INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE TCF-10 POWER LINE CARRIER FREQUENCY-SHIFT RECEIVER EQUIPMENT-TRANSFER TRIP (WITHOUT CARRIER LEVEL INDICATOR)

CAUTION: It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet and in the system instruction leaflet before energizing the system.

Printed circuit modules should not be removed or inserted when the relay is energized. Failure to observe this precaution can result in an undesired tripping output and cause component damage.

If the carrier set is mounted in a cabinet, it must be bolted down to the floor or otherwise secured before swinging out the equipment rack to prevent its tipping over.

APPLICATION

The TCF-10 frequency-shift receiver equipment as adapted for transfer-trip applications responds to carrier-frequency signals transmitted from the distant end of a power line and carried on the power line conductors. The Guard signal is transmitted continuously when conditions are normal. Its reception indicates that the channel is operative and that there is no fault in the protected equipment. The Guard frequency is 100 hertz above the center frequency of the channel. When a fault occurs within the protected equipment, protective relays switch the transmitter located there to a Trip frequency, 100 hertz below the center frequency, and also increase the power output of the transmitter (from 1 watt to 10 watts).

The reception of Trip frequency within a fixed interval after disappearance of the Guard frequency causes the energization of a high-speed electromechanical relay which closes the breaker trip circuit. If trip frequency is not received within this interval, the channel is not operating normally and a second relay closes contacts to sound an alarm. Simultaneously, the Trip relay is locked out so that a spurious Trip signal resulting later from line noise cannot cause false tripping. Other circuitry, described under OPERATION, provides security against false tripping caused by severe line noise that overrides a normal Guard signal and produces a spurious Trip signal.

CONSTRUCTION

The TCF-10 receiver unit for transfer-trip applications is mounted on a standard 19-inch wide Chassis 5 1/4 inches high (3 rack units) with edge slots for mounting on a standard relay rack. All components not mounted on Printed Circuit Modules are mounted at the rear of the panel. An input attenuator, a jack for metering the discriminator output current, and the control for the adjustable time delay in the logic circuit are accessible from the front of the Chassis See Fig. 15.

All of the circuitry that is suitable for mounting on printed circuit boards is contained on printed circuit modules that plug into the chassis from the front and are readily accessible by removing the transparent cover on the front of the chassis. The power supply components and external connectors are located at the rear of the chassis as shown in Figure 5. Reference to the internal schematic connections of Figure 1 will show the location of these components in the circuit.

All possible contingencies which may arise during installation, operation, or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding his particular installation, operation or maintenance of his equipment, the local Westinghouse Electric Corporation representative should be contacted.

through D102 to the collector of Q103 but will flow through D101 to the base of Q102 to keep it conductive. However, if Guard signal disappears and Trip signal does not appear in approximately 150 ms., C102 will charge to the breakdown point of Z105 making Q103 conductive. This will remove base input from Q104 and the alarm relay will drop out, sounding the alarm through its normally-closed contacts. (The copper slug on the alarm relay adds an additional delay of approximately 40 ms. before the alarm contacts close.) When Q103 becomes conductive, the saturation voltage at its collector is so low that any current flowing through R102 as a result of a subsequent Trip signal will be diverted through Q103 to negative instead of flowing through D101 and the base-emitter junction of Q102. If Guard signal reappears, the discriminator output at term. 15 will turn Q101 off. C101 will change and after 120 ms. it will reach the breakdown voltage of Z104 and turn Q102 on. This will allow C102 to quickly discharge through R123 and Q102 and provide the full 150 ms. time delay to be effective on any subsequent loss of guard signal.

Guard signal also produces input to transistor Q109 (block D). With base input to Q109 it has negligible voltage on its collector, but if Guard signal is lost, capacitor C104 will charge to the breakdown voltage of Z113 in a time ranging from about 2 to 20 ms., as determined by the setting of R7. This time delay also is quickly reset on reappearance of Guard signal, as C104 discharges through R114, Z113 and Q109. Transistors Q110 and Q111 are a part of logic block I. When C104 reaches the conduction voltage of Z113, Q110 conducts and removes base input from Q111. This raises the voltage on the collector of Q111 to about 15 volts, which constitutes input # 2 to block K. The purpose of logic blocks D and I is to provide an adjustable delay between the loss of Guard signal and the pickup of the Trip relay. It is possible that a noise burst might momentarily cancel the Guard signal and produce a spurious Trip signal. Provision of this adjustable delay provides a considerable degree of protection against such incorrect operations. Resistor R7 is adjustable by means of a knob on the front of the panel, and the knob can be clamped at any desired setting.

When Trip signal appears, input is fed to transistor Q106 (block E) through R119. Under this condition Q106 becomes conducting and does not supply input # 1 to Q107 (block J). If input # 2 (supplied through R115) also is lacking for Q107, the latter is non-conductive and its collector voltage is approximately 15 volts. This constitutes input # 3 to AND block K. Block K is a three-input diode-AND, with the inputs contributed by the collectors of transistors Q103, Q107 and Q111. When one or more of these transistors is conducting, input fed from the 45 volt supply through R138 cannot reach the base of Q108 to cause pickup of the Trip relay because the voltage drop across any of the three diodes plus the saturation resistance of a transistor is substantially less than the voltage drop across one diode (D110) plus the base-emitter voltage required to make Q108 conductive.

The logic blocks F and G provide further protection against incorrect tripping under noise conditions. Transistor Q105 is represented by block F; and diode D107 capacitor C103 and resistor R115 are represented by block G. Q105 receives input from either Trip or Guard signals through R101 or R106, and when either signal is present its collector voltage is a small fraction of a volt. When the transmitter is shifted from Guard to Trip by closure of a protective relay contact, the discriminator shifts its outputs very rapidly and the interval during which there is no input to Q105 is only 1.5 to 2.0 ms. Most of the charge that builds up in C103 during this interval flows to the base of Q107 and keeps it conducting after the appearance of Trip signal has removed the input through R125. However, this delay has approximately the same duration as the minimum delay obtained from block I and thus does not increase the minimum overall time for tripping following a legitimate Trip signal.

At times when severe random noise is present, such as might be produced by opening a nearby disconnect switch, the noise-produced signal may override the Guard signal and produce a discriminator output that no longer has a constant Guard output but rapidly fluctuates between Guard and Trip (and beyond). There will be relatively long periods when the discriminator has neither Guard nor Trip output. At such times capacitor C103 may approach or reach its maximum voltage, thereby keeping Q107 conducting for 40 to 50 ms. Also, because of the quick reset feature of logic block I, intermittent reappearance of Guard signal during

noise will fully reactivate the time delay for which it has been set. If a fault should occur and Trip frequency be transmitted at a time when high level noise frequencies are present, tripping may be somewhat delayed but will be accomplished before the cessation of noise unless conditions are extremely severe. The recommended 10 db. increase of transmitter output level at Trip frequency minimizes such delay.

It may appear that the function of block E in the logic diagram is duplicated by block F and could have been omitted. This is correct when the time constants are as normally supplied, but block E was retained to make the circuit adaptable to possible extreme conditions with minimum change.

In summary, the logic circuit provides the following functions:

1. Energizes alarm in case of loss of signal.
2. Prevents cancellation of an alarm by noise-produced signal.
3. Allows tripping upon reception of legitimate Trip signal.
4. Prevents tripping if channel is not operative immediately prior to reception of Trip signal.
5. Minimizes effect of noise-produced signals by utilizing noise characteristics to introduce additional Trip delay.

OUTPUT CIRCUITS

The output stage of the receiver contains the alarm relay (AL) and the tripping relay (AR). Either relay is energized from the regulated 45 volt supply when the logic circuit has determined that the existing conditions require such operation. The AL relay is a telephone type relay with a copper slug on the end of the core opposite the armature. It has two sets of Form C contacts, all points of which are connected to terminals of jack J3. The AR relay has two normally-open and two normally-closed contacts. The Four sets of contacts are connected to terminals of jack J3. The AR relay has been designed to provide very high speed operation with negligible contact bounce. While normally it is energized only briefly, it will not be damaged by continuous energization.

CARRIER LEVEL INDICATOR (WHEN SUPPLIED)

With the logic circuit connections shown on Fig. 1, the AL relay closes contacts to energize an alarm when there is absence of both Guard and Trip signal for a definite time interval. This is satisfactory when the channel fails suddenly and completely. However, the signal may weaken gradually from various causes, and it is desirable to have a means for providing a visual indication of the channel condition as well as for energizing an alarm when the signal has weakened seriously but has not reached the point of complete failure. These functions are provided if a carrier level indicator stage is included in the receiver.

The carrier level indicator is housed in the right-hand compartment of the enclosure that contains the circuit boards. Fig. 2 shows the connections of the components on this circuit board and also the external connections of the board. All other stages of the receiver are identical with those shown on Fig. 1. The same AL relay is used, but it is energized through transistor Q104 of the logic stage when the receiver does not include carrier level indication and through Q154 of the carrier level indicator when the latter is supplied. A TCF-10 receiver in which the carrier level indicator was not included at time of assembly can have this feature added later by installing the required circuit boards and making minor changes in the wiring.

The S/N detection module (carrier level indicator) has one basic function: to measure incoming in-band signal level and provide both an output to a carrier level indicating instrument and to an alarm circuit in the output module for alarming at the desired low level of signal.

This same output is also fed to an alarm circuit on the output module (contact output) for alarming at low signal levels.

The narrow-band signal of 220 hertz bandwidth called the I.F. is fed into the S/N detection board through isolation transformer T32. The amount of signal fed into the board is adjustable by means of potentiometer R111. The circuit composed of operational amplifiers IC7 and IC8 and associated components is an RMS circuit which

converts the signals into a dc voltage proportional to the r.m.s. value of the ac signals present in the IF bandwidth.

The output of the IF rms circuit is then fed to the logarithmic circuit composed of IC11A, IC12A, and IC11B which puts out a dc signal level linearly proportional to signal level in dB for feeding a microammeter calibrated with a linear dB scale with 10dB equal to 33 1/3 microamperes, is contained on the output module (contact output).

The input to the carrier level indicator is not affected by frequency variations that are within the pass band of the crystal input filter, but only by the level of the receiver input signal. When the alarm relay is energized through transistor Q104 of the logic stage (in a receiver without carrier level indicator—Fig. 1), the alarm will be activated on complete loss of signal or on loss of Guard signal if Trip signal does not appear within approximately 150 ms. After the alarm relay has dropped out and activated the alarm, the relay will not be picked up by subsequent appearance of Trip signal but only by the reappearance of Guard signal. It is desirable to retain this alarm feature when the carrier level indicator is supplied, and a single alarm relay can be caused to respond to frequency change as well as to signal level by the interconnection between the terminals of the logic and carrier level indicator circuit boards.

When Guard signal is being received, the voltage at the collector of Q103 in the logic circuit is approximately 10 volts, but this voltage is blocked from the base of (Q154) in the carrier level indicator circuit by diode D155. However, if the discriminator Guard output should fail because of a sufficient frequency shift either above or below Guard frequency, Q103 would become conductive and the collector current of (Q153) would be diverted to negative through D155 and Q103 rather than entering the base of (Q154). The latter would become nonconductive and the alarm relay would drop out, closing the alarm circuit even though the signal level is unchanged.

With Guard signal being received, the signal level just below which the discriminator Guard output drops to zero is the minimum operating level of the receiver. The AL relay should energize the alarm at a signal level somewhat above this. For usual operating conditions it should be satisfactory to set the input attenuator (R5) 15 db. above the minimum operating level and set the AL relay (by means of R156) to drop out at a signal 5 db. above the minimum operating level.

POWER SUPPLY

The regulated 20 V.D.C. and 45 V.D.C. circuits of the receiver are supplied from Zener diodes mounted on a common heat sink on the rear of the panel. Resistors (R2, R3) of suitable value are connected between the station battery supply and the 45 volt Zener to adapt the receiver for use on 48, 125 or 250 V.D.C. battery circuits. The receiver is connected to the external supply through a switch and fuses, and a pilot light indicates whether the D.C. circuits are energized. Capacitors C1 and C2 bypass r.f. or transient voltages to ground. Chokes L1 and L2 isolate the receiver from transient voltages that may appear on the D.C. supply.

CHARACTERISTICS

Frequency range	30-300 kHz
Sensitivity (noise-free channel)	0.005 volt (65 db below 1 watt for limiting)
Input Impedance	5000 ohms minimum
Bandwidth (crystal filter)	down $<$ 3 db at 220 hertz down $>$ 60 db at 1000 hertz
Discriminator	Set for 200 cycles shift from Guard to Trip frequency. Offset 25 hertz to favor Guard for all relay-output applications.
Operating time	9 ms. channel (transm. and recvr.) 2 ms. min. logic delay + 3 ms. AR relay 14 ms. minimum time +18 ms. max. added logic time (if req'd. by noise conditions) 32 ms. maximum time

Frequency spacing	
A. For two or more signals over one-way channel	500 hertz minimum
B. For two-way channel	1000 hertz, minimum between transmitter and adjacent receiver frequencies.
Ambient temperature range	−20° C to +55° C temperature around chassis.
Battery voltage variations	
Rated voltage	Allowable variation
48 V.D.C.	42 − 56 V.D.C.
125 V.D.C.	105 − 140 V.D.C.
250 V.D.C.	210 − 280 V.D.C.
Battery drain	0.20 a. at 48 V.D.C. 0.27 a. at 125 or 250 V.D.C.
Dimensions	Chasis height − 5 1/4″ or 3 r.u. Chassis width − 19″
Weight	13 lbs.

INSTALLATION

The TCF-10 receiver is generally supplied in a cabinet or on a relay rack as part of a complete carrier assembly. The location must be free from dust, excessive humidity, vibration, corrosive fumes, or heat. The maximum ambient temperature around the chassis must not exceed 55° C.

ADJUSTMENTS

All factory adjustments of the TCF-10 receiver have been carefully made and should not be altered unless there is evidence of damage or malfunctioning. Such adjustments are: frequency and output level of the oscillator and mixer; input to the amplifier and limiter; discriminator offset from center frequency; frequency spacing and magnitude of discriminator output peaks. Adjustments that must be made at time of installation are: setting of input attenuator R5; setting of the logic time delay by R7. The input attenuator and the logic time delay adjustments are made by knobs on the front of the panel.

The receiver should not be set with a greater margin of sensitivity than is needed to assure correct operation with the maximum expected variation in attenuation of the transmitter signal. In the absence of data on this, the receiver may be set to operate on a signal that is 15 db below the expected maximum signal. After installation of the receiver and the corresponding transmitter, and with a normal Guard signal being received, input attenuator R5 should be adjusted to the position at which the alarm relay drops out. R5 then should be readjusted to increase the voltage supplied to the receiver by 15 db. The scale markings for R5 permit an approximate setting to be made but it is preferable to make this setting by means of the db scales of an ac VTVM connected from ground to the sliding contact of R5.

In case the transmitter has a 1 Watt/1 Watt output and diode D56 in the discriminator is not bypassed (see discussion under OPERATION-Discriminator), the transmitter should be keyed to trip, transistor Q103 should be kept non-conducting by connecting a short clip lead across R128, and R5 should be adjusted to the position at which the trip relay just picks up. R5 then should be readjusted for a 15 db increase in receiver input, and the jumper across R128 should be removed. If D56 is bypassed the input levels at which the AL and AR relays just operate will be approximately the same, and the AL relay minimum operating point can be used as reference for arriving at the R5 setting, as described in the preceeding paragraph.

The only other adjustment which may be necessary at the time of initial installation is the adjustment of the CL1 instrument to correspond to proper variation of signal level from normal. This may be necessary if the instrument was not supplied with the receiver and was not adjusted by the factory. If this instrument was supplied and adjusted by the factory, then it could be used in adjusting R5. In this case, it would be necessary only to adjust R5 with a normal signal being received so that the instrument indicates OdB.

If the instrument was not previously adjusted by the factory, then the following procedure should

be used in adjusting the instrument. (Note: When CL1 instrument is supplied within the chassis, this is factory adjusted.)

1. Set incoming level into receiver at +10dB above normal level.
2. Adjust span adjustment, R147, so that the voltage at TP72 with respect ot TP62 (common) is +3.000 volts.
3. Reduce incoming signal into receiver by 30dB.
4. Adjust full scale adjustment, R153, so that instrument now reads −20dB. (This is approximately 0 microamperes).
5. Increase signal to +10dB level. (This is 100 microamperes).
6. Adjust slope adjustment R155 to read +10dB on instrument.
7. Reduce signal to normal level. Instrument should read OdB. If desired, instrument could be adjusted to read OdB with R155 with sacrifice in reading accuracy for +10dB.

It is recommended that R7 be set for maximum time delay (full clockwise rotation) unless field tests have shown that a shorter delay can be used without danger of false tripping under conditions of severe line noise, such as may be caused by the opening of nearby disconnect switches.

FACTORY ADJUSTMENTS

In case the factory adjustments have been altered or there is suspicion of improper adjustments or malfunctioning, then the following procedures can be used. In addition, alterations to the settings used by the factory for low signal level clamping and low signal-to-noise ratio clamping can be made using these procedures if desired.

Potentiometer R12 in the oscillator and mixer should be set for 0.3 volts, measured with a VTVM connected between TP11 and terminal 33 on the circuit board (ground terminal of voltmeter). A frequency counter can be connected to the same points for a check on the frequency which should be 20kHz above the channel center frequency. The frequency is fixed by the crystal used, except that it may be changed a few cycles by the value of capacitor C12. Reducing C12 increases the frequency, but the capacity should never be less than a value that assures reliable starting of oscillation. The frequency at room temperature is usually several cycles above the crystal nominal frequency as this reduces the frequency deviation at the temperature extremes.

The adustment of the amplifier and limiter is made by potentiometer R52. An oscilloscope should be connected from TP56 at the base of Q54 to terminal 33 of the limiter. With 5 millivolts of higher frequency on the receiver input (R5 set at zero), R52 should be adjusted to the point where the peaks of the oscilloscope trace begin to flatten. This should appear on the upper and lower peaks at approximately the same setting. (Note: Input attenuator R5 could be used to produce 5 mv of signal across input test jacks J1 and J2 if desired.)

Adjustment of the discriminator is made by capacitors C63 and C68. In order to offset the discriminator by 25 Hertz in the Trip direction, apply to the receiver input a 5 mv. signal taken from an oscillator set at fc-25 Hertz (R5 at zero.) Connect a 1.5-0-1.5 milliammeter in the circuit at J1 and a VTVM across R80. Adjust C68 for zero current in the milliammeter and C63 for maximum voltage across R80 rechecking the adjustments alternately until no further change is observed. Remove the VTVM from across R80 and observe the milliammeter reading as the oscillator frequency is varied. Postive and negative peaks should occur at fc + 75 Hertz and fc-125 Hertz, with the latter peak being 20% or 15% lower than the former because of diode D56 in the Trip output path.

In case a check is desired of any of the delay times of the reciver (such as channel time or logic delays), this can be done most conveniently by means of an oscilloscope with a calibrated triggered sweep. A two-pole toggle switch, checked to have less than 1 ms. interval between pole closures, can be used to impress the signal and trigger the sweep.

MAINTENANCE

Periodic checks of the received carrier signal and the receiver sensitivity will detect gradual deterioration and permit its correction before failure can result. The carrier level indicator, when provided, permits ready observation of the received signal level. With or without a carrier level indicator, an overall check can be made with the attenua-

tion control R5. A change in operating margin from the original setting can be detected by observing the change in the dial setting required to drop out the alarm relay. If there is a substantial reduction in margin, the signal voltage at the receiver input should be checked to see whether the reduction is due to loss of signal or loss of receiver sensitivity.

All adjustable components on the printed circuit boards are accessible when the front cover is removed. However, as described under "CONSTRUCTION", any board may be made entirely accessible while permitting electrical operation by using board extender style no. 1447C86G01. This permits attaching instrument leads to the various test points of terminals when making voltage, oscilloscope or frequency checks. It also contains switches to facilitate trouble shooting.

It is advisable to record voltage values after adjustment in order to establish reference values which will be useful when checking the apparatus. The readings will remain fairly constant over an indefinite period unless a failure occurs. However, if transistors are changed, there may be considerable difference in these readings without the overall performance being affected.

Typical voltage values are given in Table I and II. Voltages should be measured with a VTVM. Some readings may vary as much as ±20%.

TABLE I
RECEIVER D-C MEASUREMENTS

NOTE: All voltage readings taken with ground of dc VTVM on terminal 9 (neg. d.c.). Receiver adjusted for 15 db operating margin with Guard signal down 50 db from 1 watt and Trip signal down 40 db. Unless otherwise indicated, voltage will not vary appreciably whether signal is Guard, Trip or zero.

Collector Transistor	Volts (+)	
Q11	<13	
Q12	15	(Guard or Trip)
Q13	15	(Guard or Trip)
Q31	2.5	
Q32	2.5	
Q51	11.5	
Q52	12	
Q53	15.5	
Q54	2.5	
Q55	< 1	(No. sig. or Trip)
Q55	19.5	(Guard)
Q56	< 1	(No sig. or Guard)
Q56	19.5	(Trip)
Q101	< 1	(No sig. or Trip)
Q101	7	(Guard)
Q102	21	(No signal)
Q102	< 1	(Guard or keyed Trip #)
Q103	< 1	(No signal)
Q103	10	(Guard or keyed Trip)
Q104	45	(No signal)
Q104	< 1	(Guard or keyed Trip)
Q105	40	(No signal)
Q105	< 1	(Guard or Trip)
Q106	15	(No sig. or Guard)
Q106	< 1	(Trip)
Q107	< 1	(No sig. or Guard)
Q107	15	(Trip)
Q108	45	(No sig. or Guard)
Q108	< 1	(Keyed Trip)
Q109	10	(No sig. or Trip)
Q109	< 1	(Guard)
Q110	< 1	(No sig. or Trip)
Q110	15	(Guard)
Q111	15	(No sig. or Trip)
Q111	< 1	(Guard)

- "Keyed Trip" signifies minimum transition time from Guard to Trip.

TABLE II
RECEIVER RF MEASUREMENTS

NOTE: Voltmeter readings taken between receiver input and Q32 are not meaningful or feasible because of waveform or effect of instrument loading. Receiver adjusted as in Table I. Reference to +20V.

Collector of Transistor	Volts (1 watt-Guard)	Volts (10 watts-Trip)
Q32	.25	.8
Q51	.3	.9
Q52	.4	.65
Q53	2.1	2.2
Q54	4.8	4.5

RELAY MAINTENANCE AND ADJUSTMENT

The AL and AR relay contacts should

be cleaned periodically. A contact burnisher S # 182A836H01 is recommended for this purpose. The use of abrasive material for cleaning contacts is not recommended, because of the danger of embedding small particles in the face of the soft silver and thus impairing the contact. Care must be taken to avoid distorting the contact springs during burnishing, particularly in the case of the AR relay.

These relays have been properly adjusted at the factory to insure correct operation, and under normal field conditions they should not require readjustment. If, however, the adjustments are disturbed in error, or if it becomes necessary to replace some part, the following adjustment procedure should be used.

In the AL relay the armature gap should be approximately 0.004 inch with the armature closed. This adjustment is made with the armature closed. This adjustment is made with the armature stop screw and locknut. The contact leaf springs should be adjusted to obtain at least 0.015 inch gap on all contacts when fully open. There should be at least 0.010 inch follow on all normally-open contacts and 0.005 inch follow on all normally-closed contacts. The relay should pick up at approximately 35 volts.

FILTER RESPONSE MEASUREMENTS

The crystal input filter (FL1) and the IF filter (FL2) are in sealed containers and repairs can be made only by the factory. The stability of the original response characteristics is such that in normal usage no appreciable change in response will occur. However the test circuits of Dwg. 849A109 can be used in case there is reason to suspect that either of the filters has been damaged.

Fig. 4 shows the −3db and −60db check points for the crystal filters. The response curve of the IF filter shows the combined effect of the two sections, and was obtained by adding the attenuation of each section for identical frequencies. The scale of Fig. 4 was chosen to show the crystal filter response, which permitted only a portion of the IF filter curve to be shown. The check points for the pass band of each section of the latter are "down 3db maximum at 19.75 and 20.25 kHz, and for the stop band are "down 18 db minimum at 19.00 and 21.00 kHz. The signal generator voltage must be held constant throughout the entire check. A value of 20 db (7.8 volts) is suitable. The reading of VM2 at the frequency of minimum attenuation should not be more than 22db below the reading of VM1. It should be noted that a limit measured in this manner is for convenience only and does not indicate actual insertion loss of the filter. The insertion loss would be approximately 16db less than the measured difference because of the input resistor and the difference in input and output impedances of the filter.

Because of the extreme frequency sensitivity of the crystal filter, the oscillator used in its test circuit should have very good frequency stability and a close vernier control. The oscillators used for factory testing have special modifications for this use. A value of approximately 10db (2.45 volts) is suitable for the constant voltage at which to hold VM1 throughout the check. The reading of VM2 at the frequency of minimum attenuation will vary somewhat with the channel frequency but should not be more than 11db below the reading of VM1. (The filter insertion loss is approximately 6db less than the difference in readings.)

CONVERSION OF RECEIVER FOR CHANGED CHANNEL FREQUENCY

The parts required for converting a TCF-10 receiver for operating on a different channel frequency consist of a new crystal filter (FL1), a new local oscillator crystal (Y11) and probably a different feedback capacitor (C12). Because the wide range of channel frequencies precludes maintaining a factory stock of the various crystals, immediate shipment of the filter and the oscillator crystal cannot be made. After the crystals have been procured and the filter has been completed, it is recommended that the receiver be returned to the factory for the conversion and for complete test and adjustment. However, if the time that the receiver can be out of service must be kept to a minimum, the conversion may be made by customers who are equipped for this work.

RECOMMENDED TEST EQUIPMENT

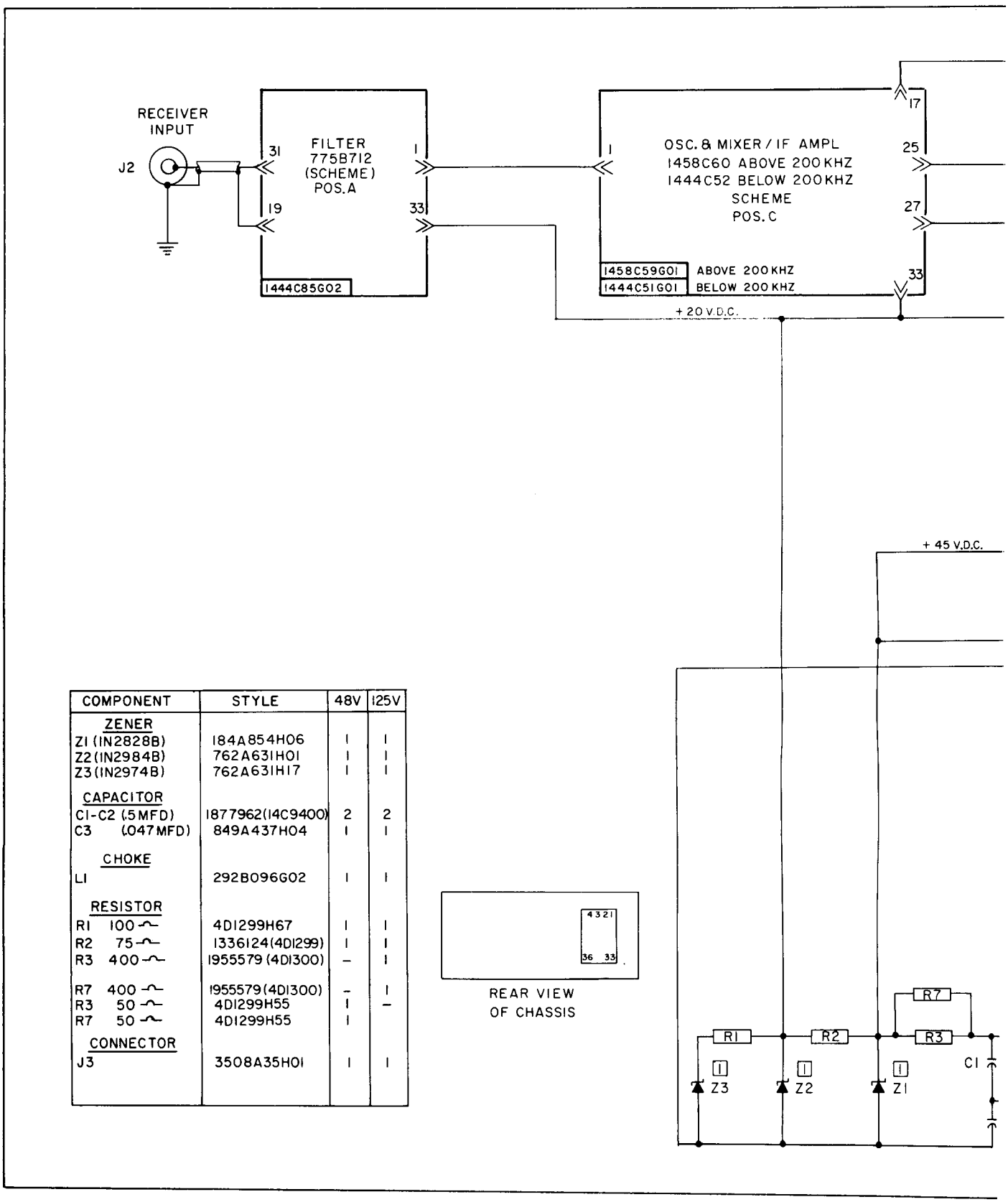
I. Minimum Test Equipment for Installation.
   a. AC vacuum Tube Voltmeter (VTVM).
      Voltage range 0.003 to 30 volts, frequency range 60 Hz to 330 kHz, input impedance 7.5 megohms.
   b. DC Vacuum Tube Voltmeter (VTVM).
      Voltage Range: 1.5 to 300 volts
      Imput Impedance: 7.5 megohms
   c. Milliammeter, 0-3 range (if receiver has carrier level indicator).

II. Desirable Test Equipment for Apparatus Maintenance
   a. All items listed in I.
   b. Signal Generator
      Output Voltage: up to 8 volts
      Frequency Range: 20-kHz to 330-kHz
   c. Oscilloscope
   d. Frequency counter
   e. Ohmmeter
   f. Capacitor checker
   g. Milliammeter, 0-1.5 or preferably 1.5-0-1.5 range, for checking discriminator.

Some of the functions of the recommended test equipment are combined in the type TCT carrier test meter unit, which is designed to mount on a standard 19″ rack but also can be removed and used as a portable unit.

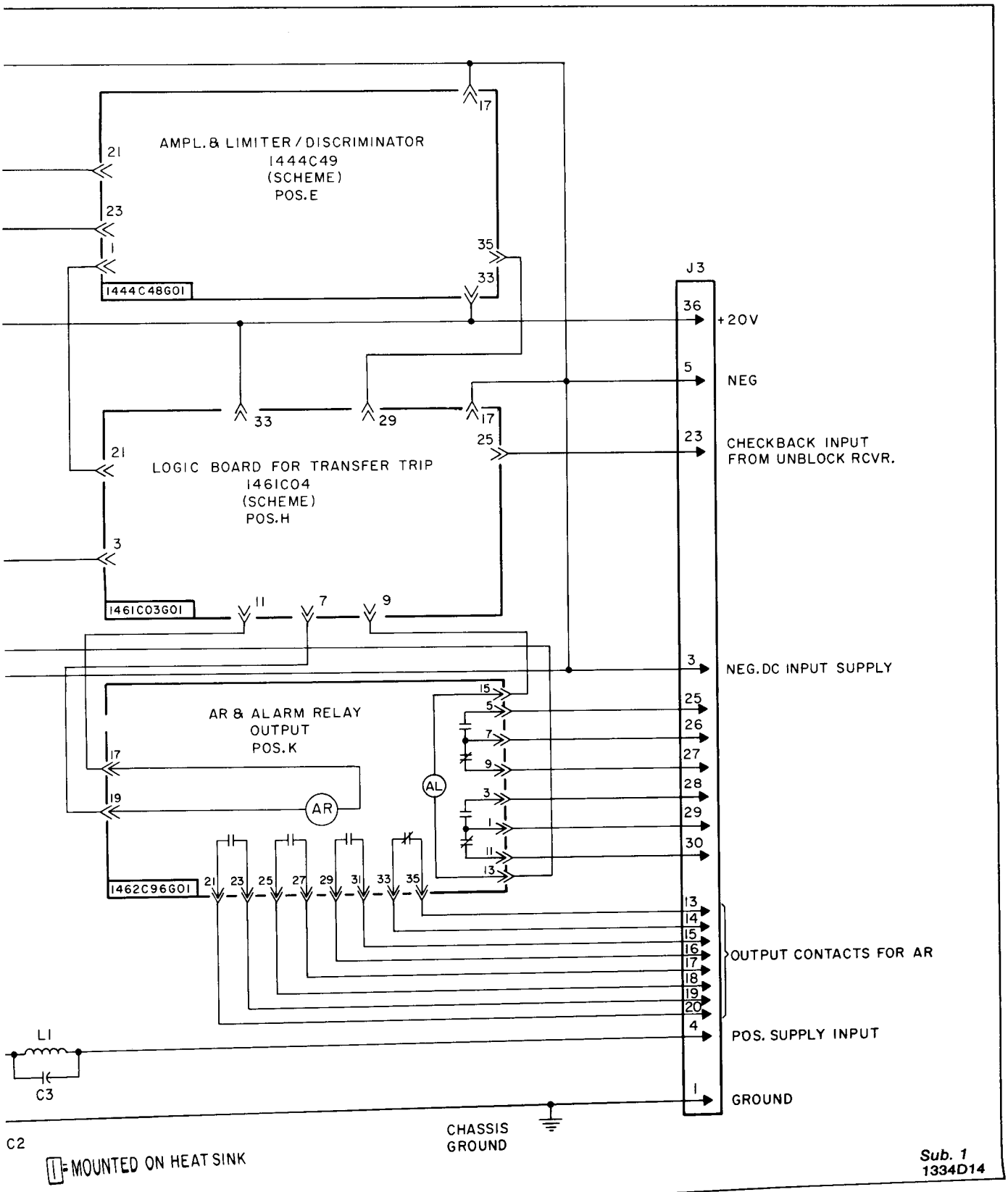
RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, replacement parts can be furnished, in most cases, to customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data, the electrical value, style number, and identify the part by its designation on the Internal Schematic drawing.



COMPONENT	STYLE	48V	125V
ZENER			
Z1 (IN2828B)	184A854H06	1	1
Z2 (IN2984B)	762A631H01	1	1
Z3 (IN2974B)	762A631H17	1	1
CAPACITOR			
C1-C2 (.5MFD)	1877962(14C9400)	2	2
C3 (.047MFD)	849A437H04	1	1
CHOKE			
L1	292B096G02	1	1
RESISTOR			
R1 100 Ω	4D1299H67	1	1
R2 75 Ω	1336124(4D1299)	1	1
R3 400 Ω	1955579 (4D1300)	–	1
R7 400 Ω	1955579(4D1300)	–	1
R3 50 Ω	4D1299H55	1	–
R7 50 Ω	4D1299H55	1	
CONNECTOR			
J3	3508A35H01	1	1

Fig. 1 Internal Schematic of Transfer Trip Recei


AMPL. & LIMITER / DISCRIMINATOR
1444C49
(SCHEME)
POS. E
1444C48G01
LOGIC BOARD FOR TRANSFER TRIP
1461C04
(SCHEME)
POS. H
1461C03G01
AR & ALARM RELAY
OUTPUT
POS. K
1462C96G01
AR
AL
J3
+20V
NEG
CHECKBACK INPUT
FROM UNBLOCK RCVR.
NEG. DC INPUT SUPPLY
OUTPUT CONTACTS FOR AR
POS. SUPPLY INPUT
GROUND
L1
C3
C2
CHASSIS
GROUND
1 = MOUNTED ON HEAT SINK
Sub. 1
1334D14

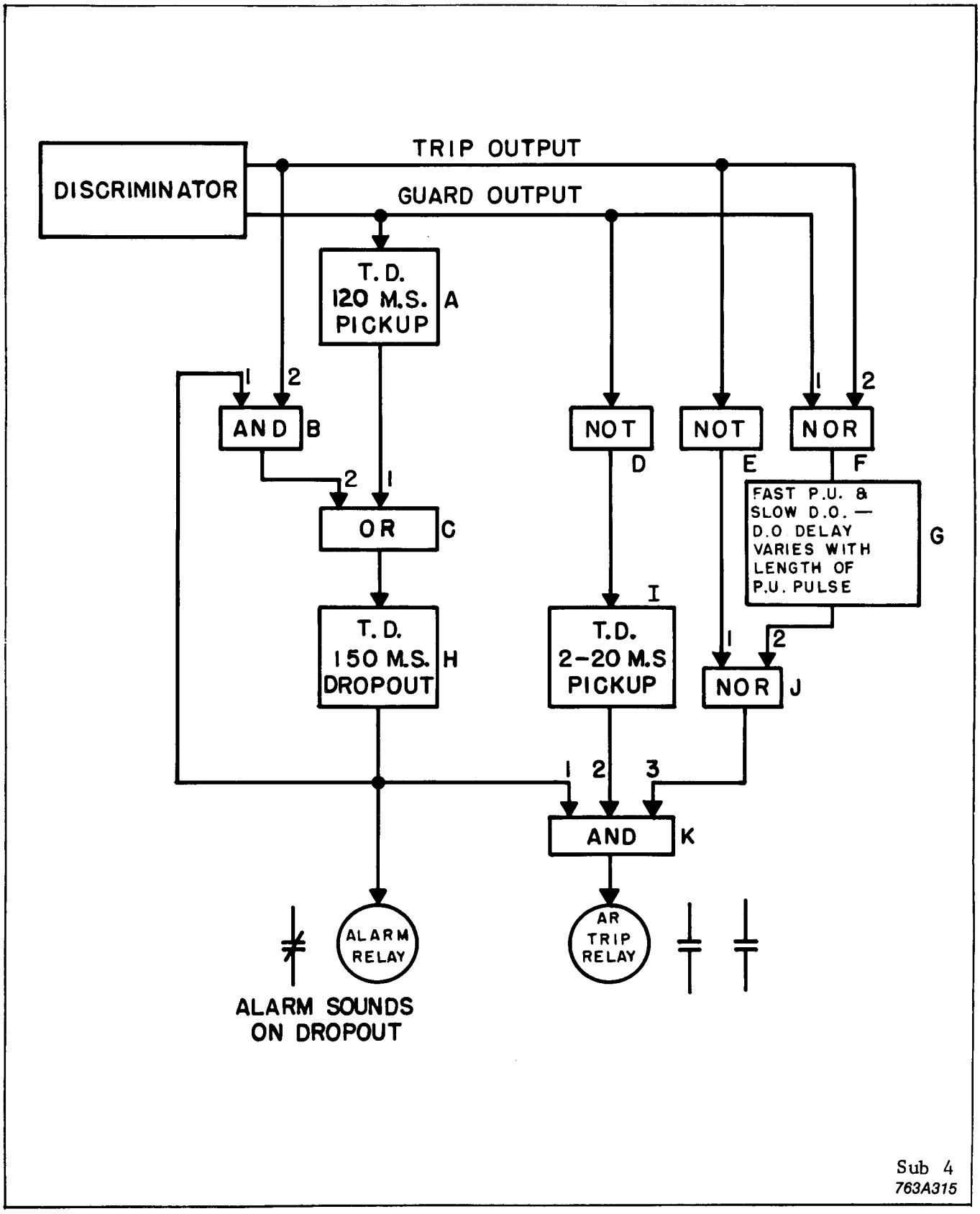


Fig. 3. Block Diagram of Output Logic Circuit

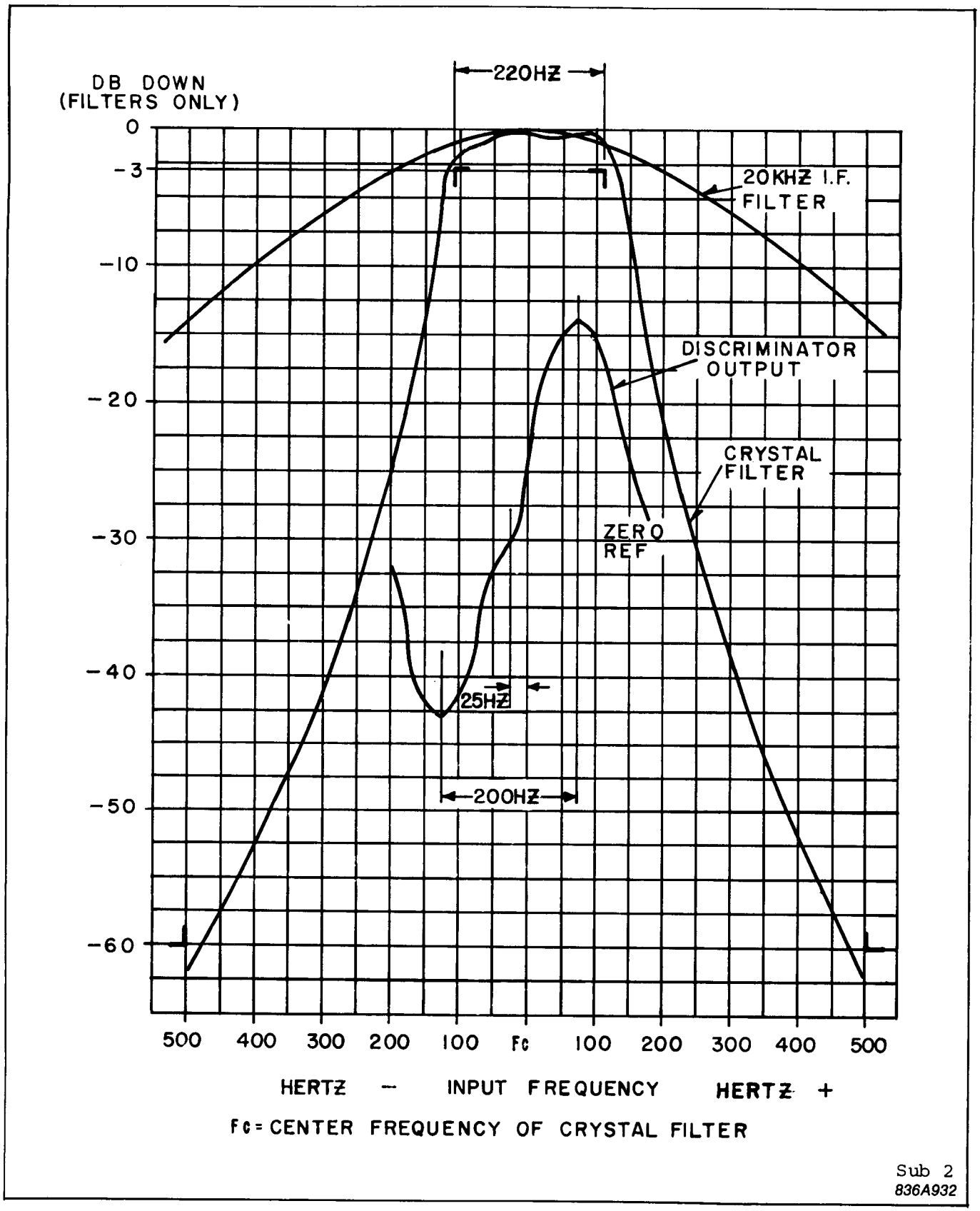


Fig. 4. Filter and Discriminator Characteristics of the Receiver

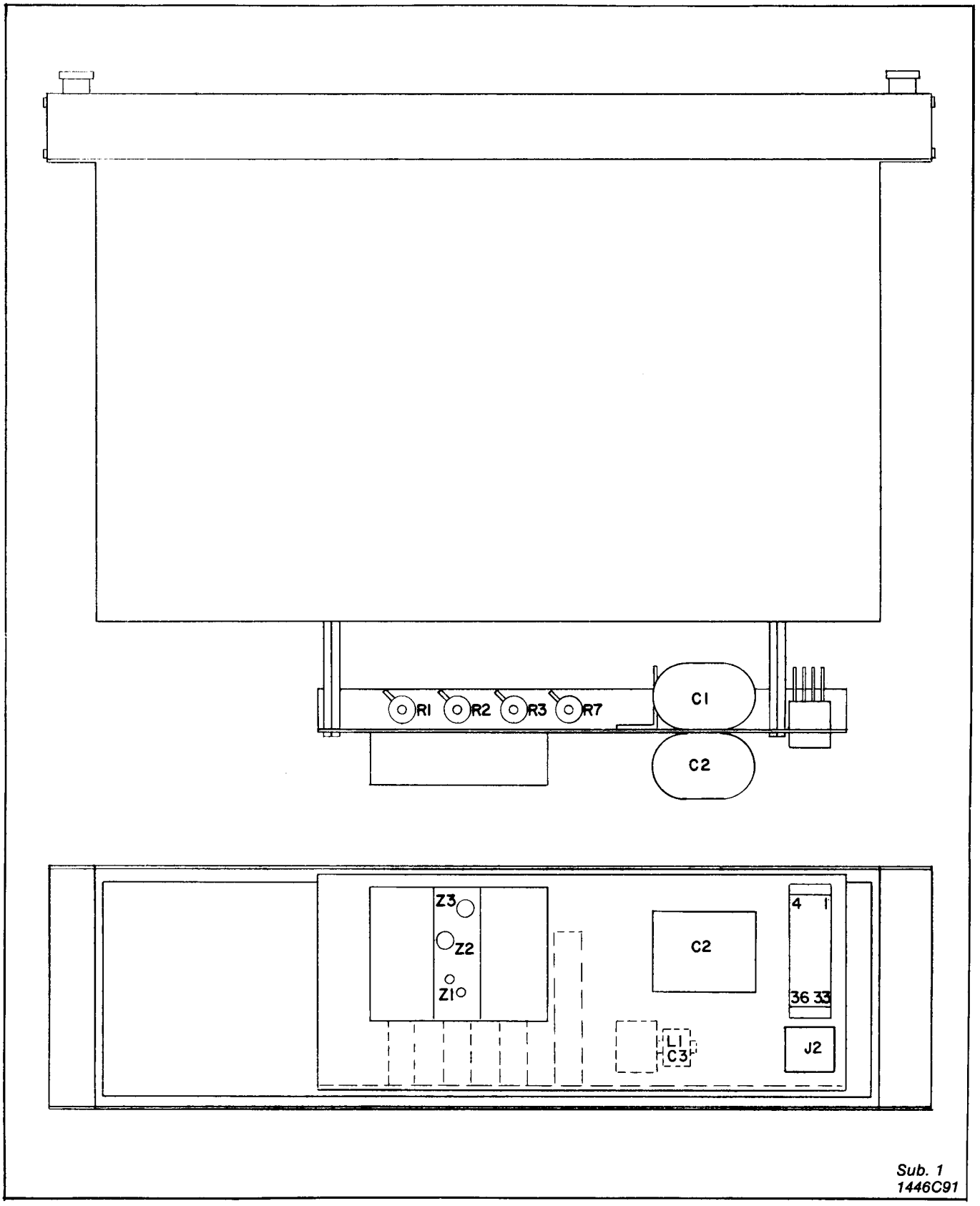


Fig. 5. Component Location of the Receiver Panel

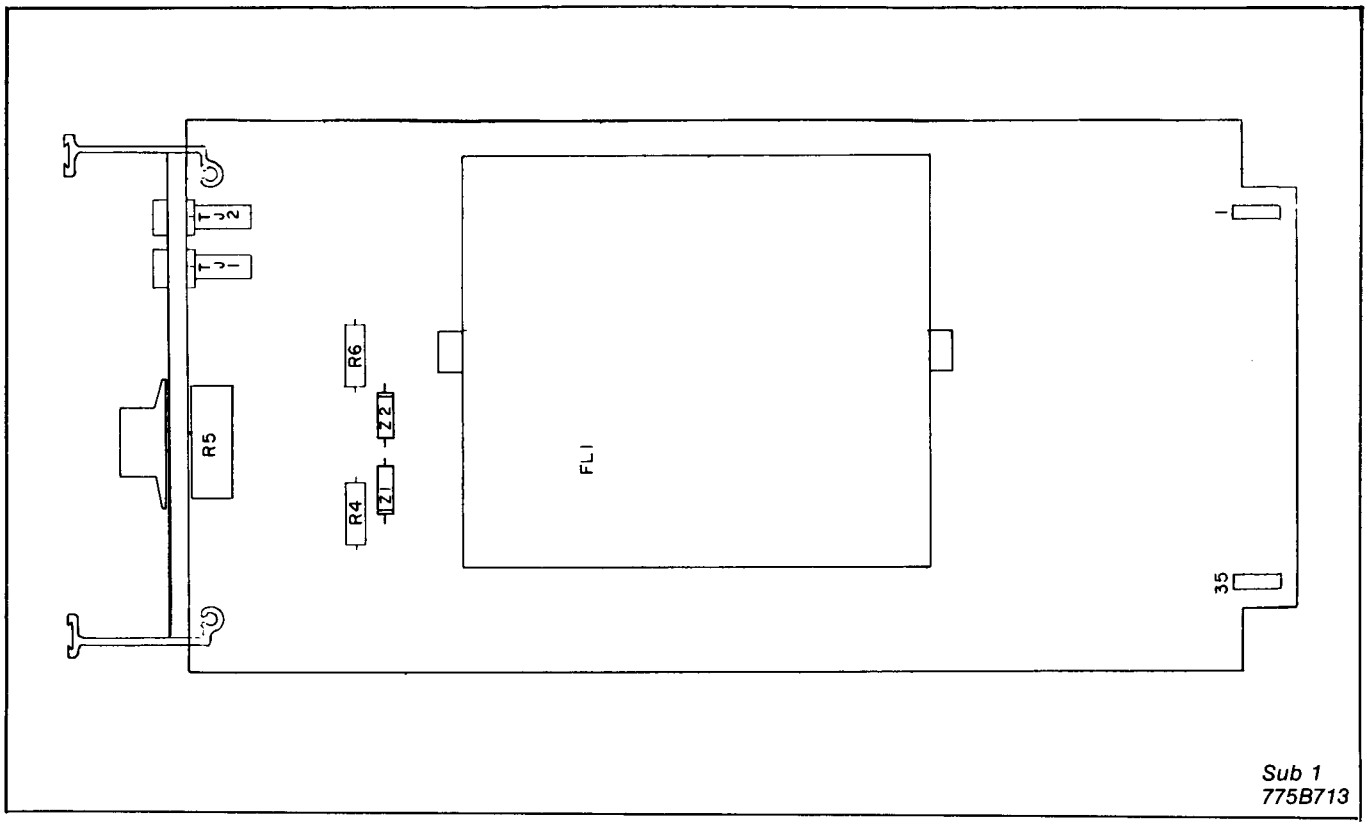


Fig. 6. Component Location of the Input Filter Module

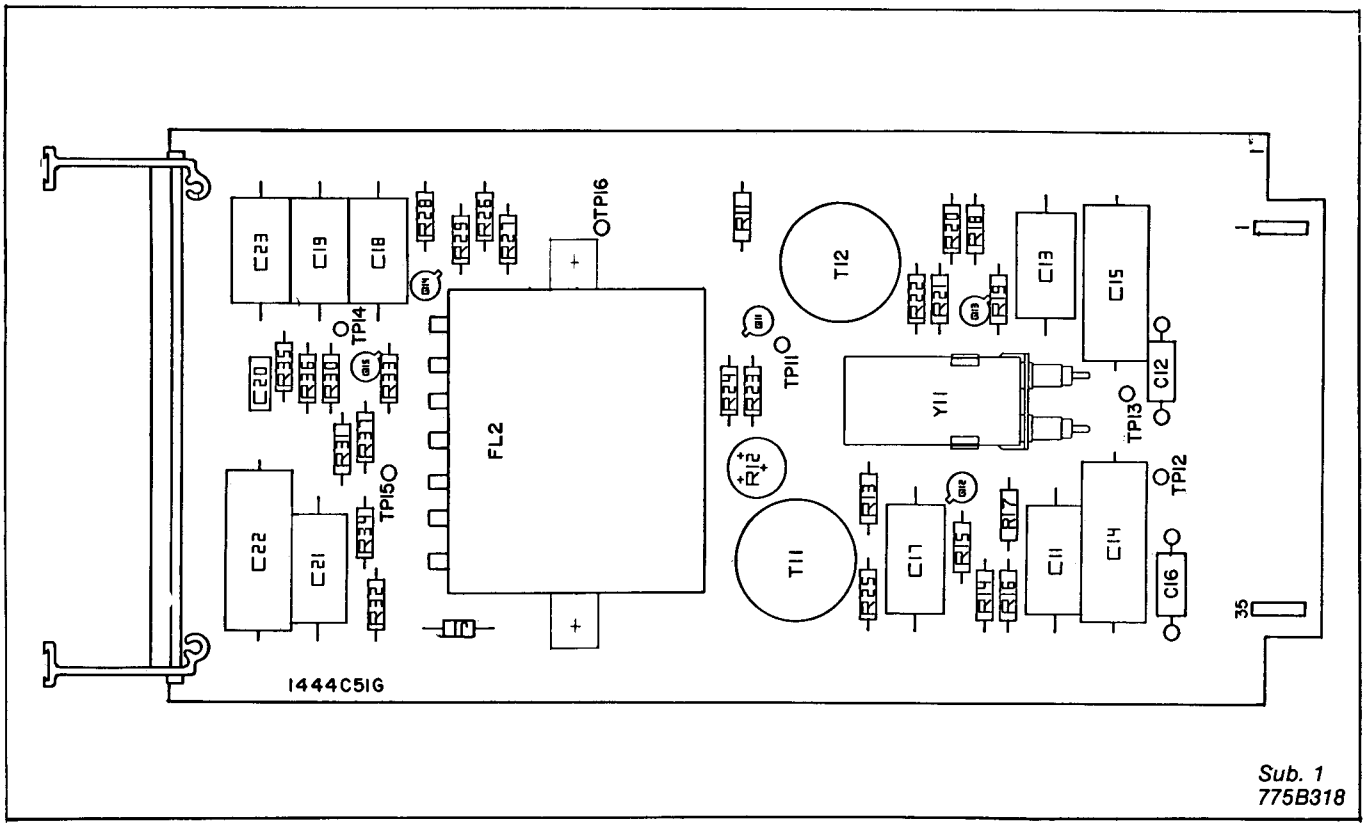


Fig. 7. Component Locations 30-200Hz. Oscillator and Mixer I.F. Amplifier

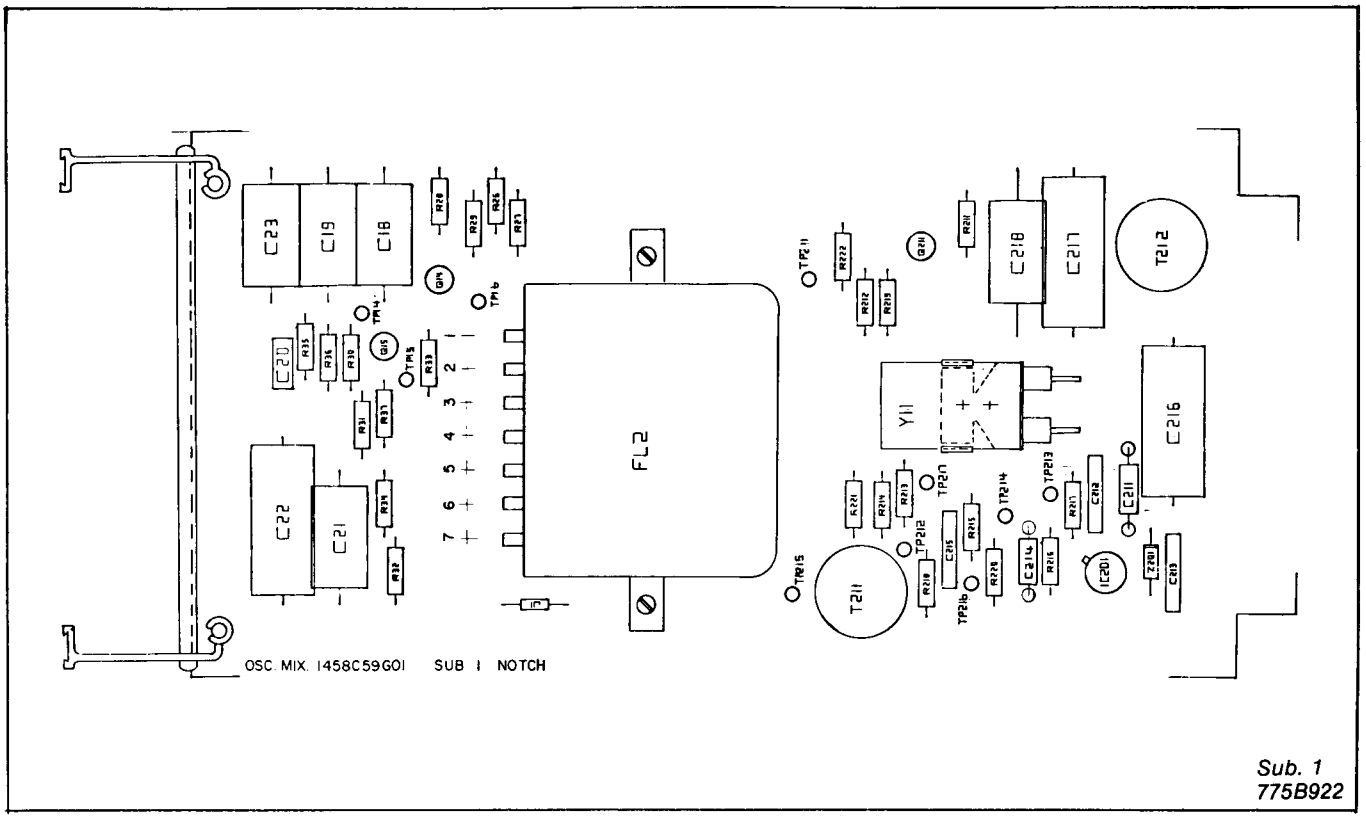


Fig. 8. Component Locations 200.5-300Hz. Oscillator and Mixer I.F. Amplifier

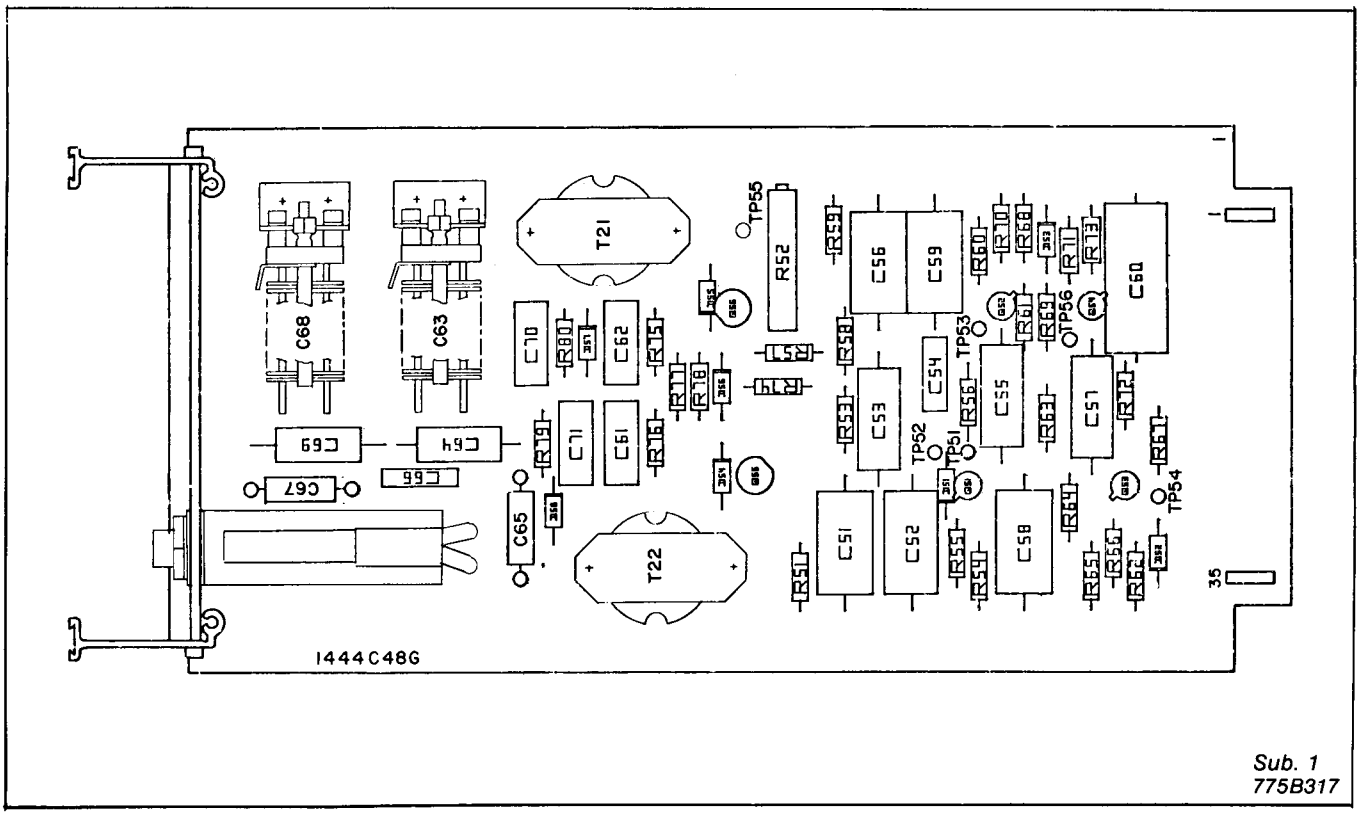


Fig. 9. Component Locations Amplifier and Limiter Discrimina tor Module

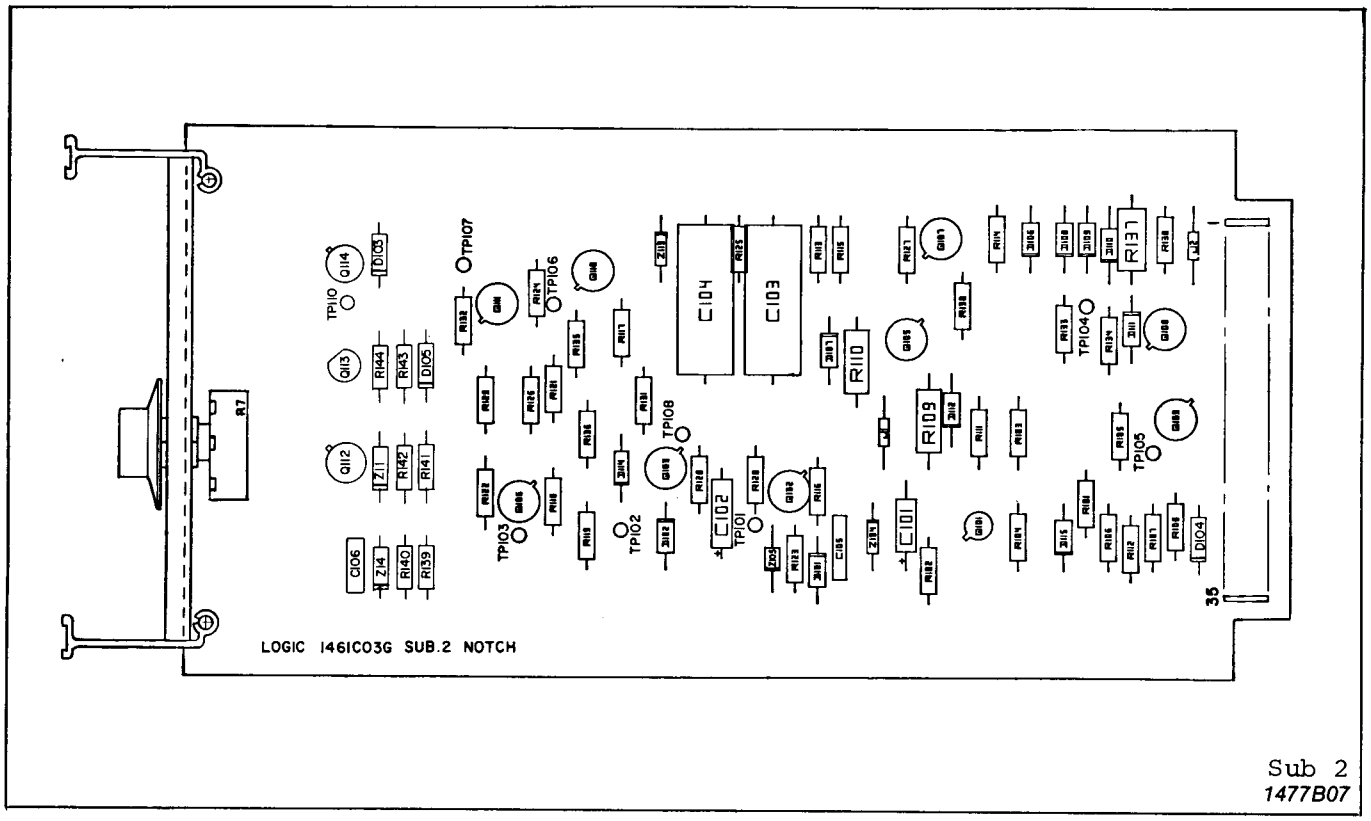


Fig. 10. Component Locations Logic Board for Transfer Trip

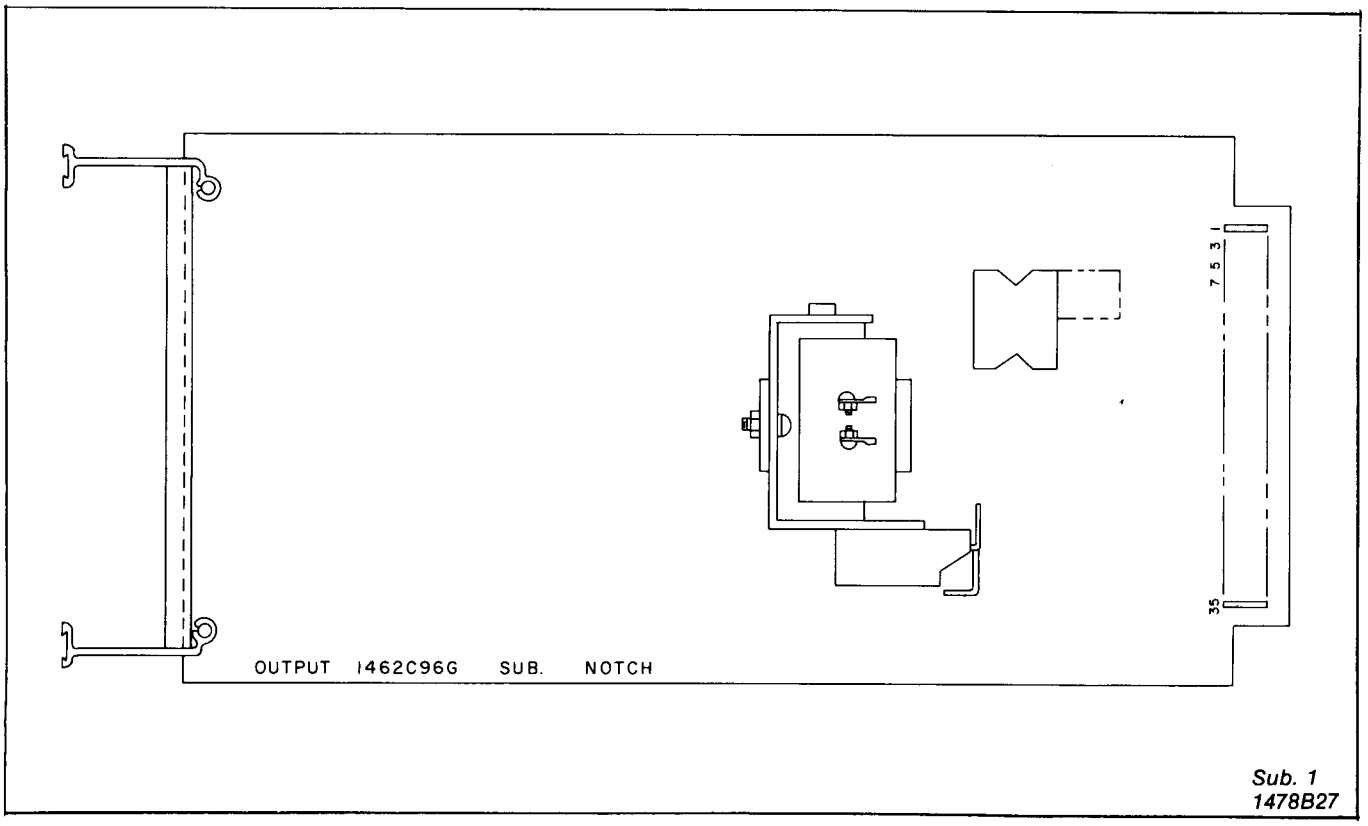


Fig. 11. Component Locations of the Output Printed Circuit Board

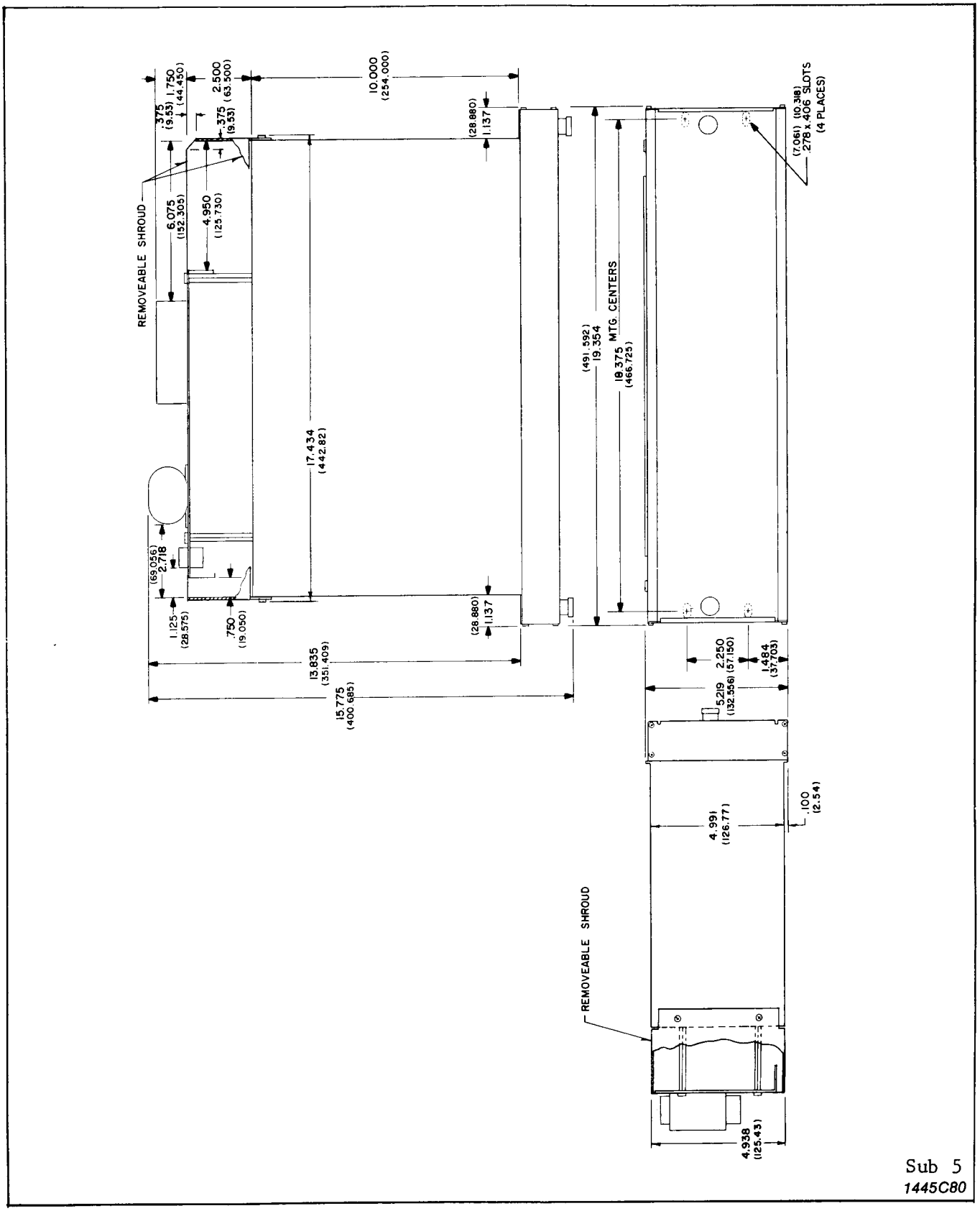
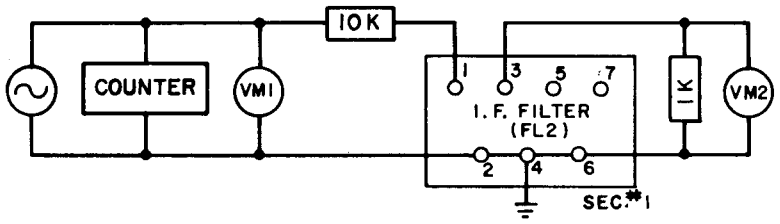
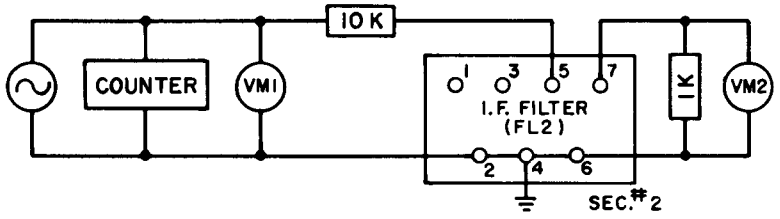
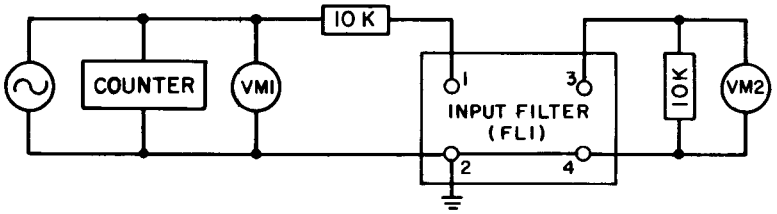


Fig. 12. Outline and Drilling for Receiver Assembly





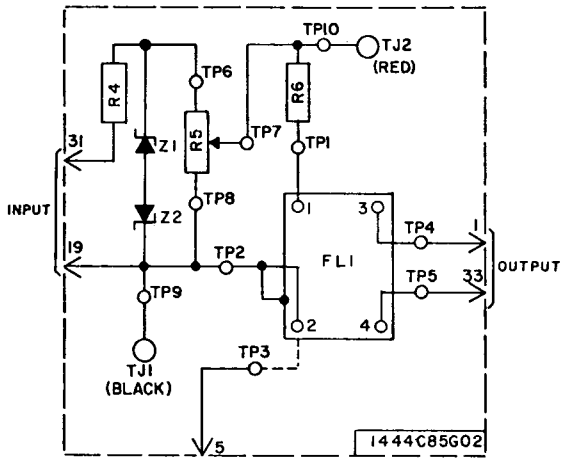
I. F. FILTER TEST CIRCUIT CONNECTIONS



INPUT FILTER TEST CIRCUIT CONNECTIONS

Sub. 1
849A109

Fig. 13. Test Currents for Frequency Shift Receiver Filters

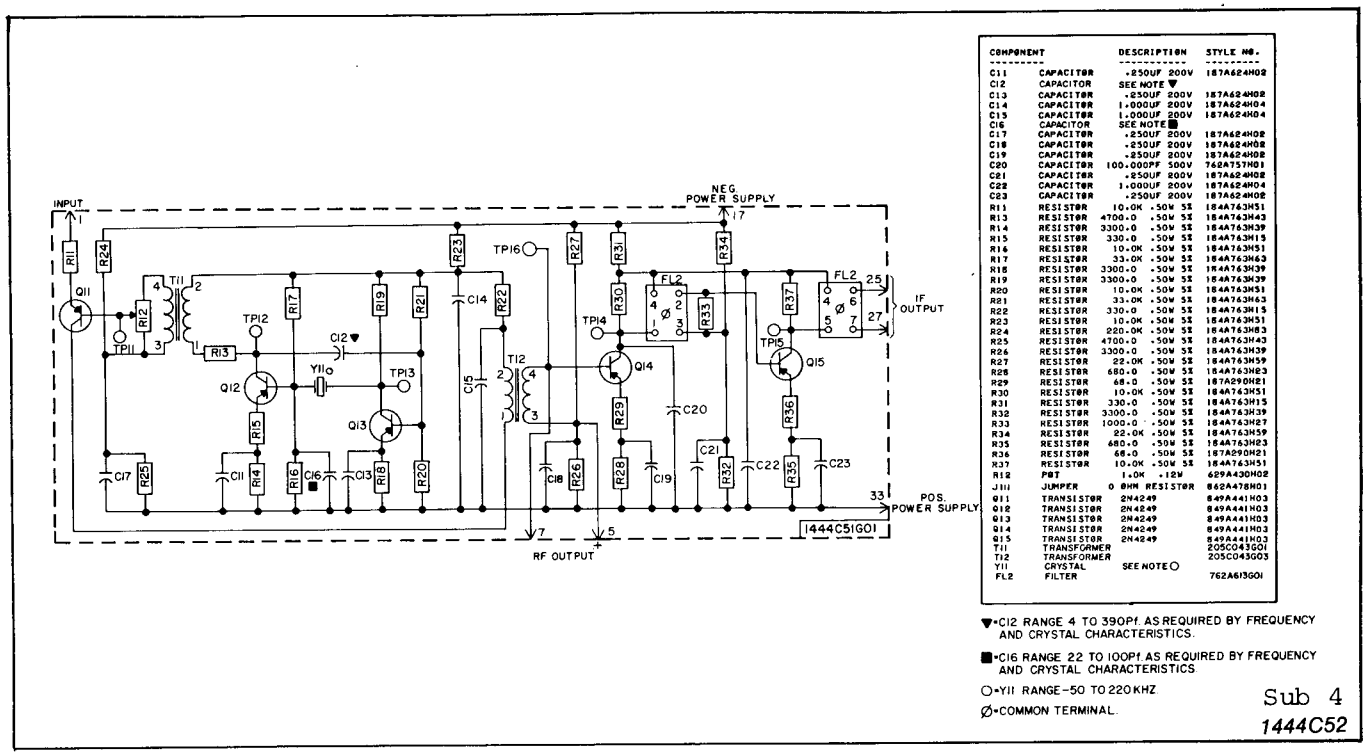


COMPONENT		DESCRIPTION	STYLE NO.
R4	RESISTOR	100.0 .50W 5%	184A763H03
R6	RESISTOR	10.0K .50W 5%	184A763H51
R5	POTENTIOMETER	10.0K 2W	185A086H10
FL1	FILTER		□
TJ1	TIP JACK	BLACK	187A332H02
TJ2	TIP JACK	RED	187A332H01
Z1	ZENER	IN3027B	188A302H07
Z2	ZENER	IN3027B	188A302H07

□ =DETERMINED BY CHANNEL FREQUENCY PER ORDER.

Sub. 1
775B712

Fig. 13 Test Circuits for Frequency Shift Receiver Filters



COMPONENT		DESCRIPTION	STYLE NO.
C11	CAPACITOR	.250UF 200V	187A624H02
C12	CAPACITOR	SEE NOTE ▼	
C13	CAPACITOR	.250UF 200V	187A624H02
C14	CAPACITOR	1.000UF 200V	187A624H04
C15	CAPACITOR	1.000UF 200V	187A624H04
C16	CAPACITOR	SEE NOTE ■	
C17	CAPACITOR	.250UF 200V	187A624H02
C18	CAPACITOR	.250UF 200V	187A624H02
C19	CAPACITOR	.250UF 200V	187A624H02
C20	CAPACITOR	100.000PF 500V	762A757H01
C21	CAPACITOR	.250UF 200V	187A624H02
C22	CAPACITOR	1.000UF 200V	187A624H04
C23	CAPACITOR	.250UF 200V	187A624H02
R11	RESISTOR	10.0K .50W 5%	184A763H51
R13	RESISTOR	4700.0 .50W 5%	184A763H43
R14	RESISTOR	3300.0 .50W 5%	184A763H39
R15	RESISTOR	330.0 .50W 5%	184A763H15
R16	RESISTOR	10.0K .50W 5%	184A763H51
R17	RESISTOR	33.0K .50W 5%	184A763H63
R18	RESISTOR	3300.0 .50W 5%	184A763H39
R19	RESISTOR	3300.0 .50W 5%	184A763H39
R20	RESISTOR	10.0K .50W 5%	184A763H51
R21	RESISTOR	33.0K .50W 5%	184A763H63
R22	RESISTOR	330.0 .50W 5%	184A763H15
R23	RESISTOR	10.0K .50W 5%	184A763H51
R24	RESISTOR	220.0K .50W 5%	184A763H83
R25	RESISTOR	4700.0 .50W 5%	184A763H43
R26	RESISTOR	3300.0 .50W 5%	184A763H39
R27	RESISTOR	22.0K .50W 5%	184A763H59
R28	RESISTOR	680.0 .50W 5%	184A763H23
R29	RESISTOR	68.0 .50W 5%	187A290H21
R30	RESISTOR	10.0K .50W 5%	184A763H51
R31	RESISTOR	330.0 .50W 5%	184A763H15
R32	RESISTOR	3300.0 .50W 5%	184A763H39
R33	RESISTOR	1000.0 .50W 5%	184A763H27
R34	RESISTOR	22.0K .50W 5%	184A763H59
R35	RESISTOR	680.0 .50W 5%	184A763H23
R36	RESISTOR	68.0 .50W 5%	187A290H21
R37	RESISTOR	10.0K .50W 5%	184A763H51
R12	POT	1.0K .12W	629A430H02
J111	JUMPER	0 OHM RESISTOR	862A478H01
Q11	TRANSISTOR	2N4249	849A441H03
Q12	TRANSISTOR	2N4249	849A441H03
Q13	TRANSISTOR	2N4249	849A441H03
Q14	TRANSISTOR	2N4249	849A441H03
Q15	TRANSISTOR	2N4249	849A441H03
T11	TRANSFORMER		205C043G01
T12	TRANSFORMER		205C043G03
Y11	CRYSTAL	SEE NOTE ○	
FL2	FILTER		762A613G01

▼-C12 RANGE 4 TO 390pf. AS REQUIRED BY FREQUENCY AND CRYSTAL CHARACTERISTICS.

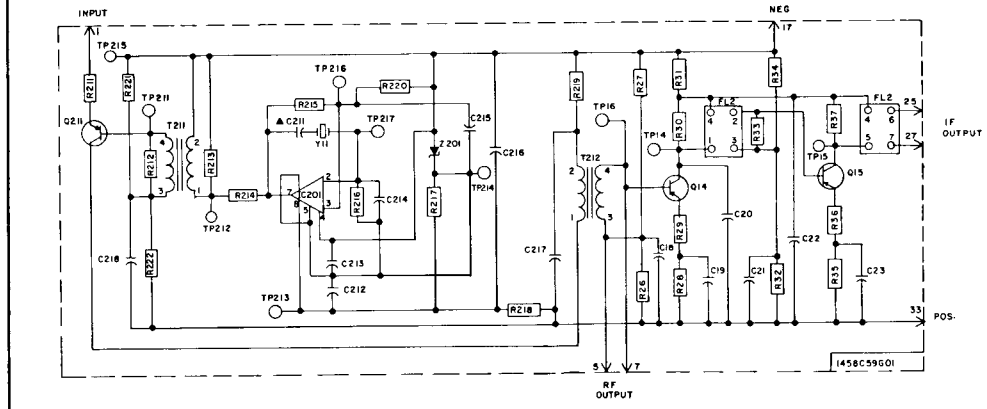
■-C16 RANGE 22 TO 100pf. AS REQUIRED BY FREQUENCY AND CRYSTAL CHARACTERISTICS

○-Y11 RANGE-50 TO 220 KHZ

Ø-COMMON TERMINAL.

Sub 4
1444C52

Fig. 15. Internal Schematic 30-200Hz. Oscillator and Mixer I.F. Amplifier Module



COMPONENT		DESCRIPTION	STYLE NO.
C18	CAPACITOR	.250UF 200V	187A624H02
C19	CAPACITOR	.250UF 200V	187A624H02
C20	CAPACITOR	100.000PF 500V	762A757H01
C21	CAPACITOR	.250UF 200V	187A624H02
C22	CAPACITOR	1.000UF 200V	187A624H04
C23	CAPACITOR	.250UF 200V	187A624H02
▲ C211	CAPACITOR	SEE NOTE ▲	
C213	CAPACITOR	.100UF 50V	149A663H04
C215	CAPACITOR	.100UF 50V	149A663H04
C216	CAPACITOR	1.000UF 200V	187A624H04
C217	CAPACITOR	1.000UF 200V	187A624H04
C218	CAPACITOR	.250UF 200V	187A624H02
○ C214	CAPACITOR	SEE NOTE ○	
IC201	INT CKT	MA710	201C624H03
J1	JUMPER	0 OHM RESISTOR	862A478H01
R26	RESISTOR	3300.0 .50W 5%	184A763H39
R27	RESISTOR	22.0K .50W 5%	184A763H59
R28	RESISTOR	680.0 .50W 5%	184A763H23
R29	RESISTOR	68.0 .50W 5%	187A290H21
R30	RESISTOR	10.0K .50W 5%	184A763H51
R31	RESISTOR	330.0 .50W 5%	184A763H15
R32	RESISTOR	3300.0 .50W 5%	184A763H39
R33	RESISTOR	1000.0 .50W 5%	184A763H27
R34	RESISTOR	22.0K .50W 5%	184A763H59
R35	RESISTOR	680.0 .50W 5%	184A763H23
R36	RESISTOR	68.0 .50W 5%	187A290H21
R37	RESISTOR	10.0K .50W 5%	184A763H51
R212	RESISTOR	1000.0 .50W 5%	184A763H27
R213	RESISTOR	10.0K .50W 5%	184A763H51
R214	RESISTOR	2700.0 .50W 5%	184A763H47
R215	RESISTOR	10.0K .50W 5%	184A763H51
R216	RESISTOR	6200.0 .50W 5%	184A763H49
R217	RESISTOR	2000.0 .50W 5%	184A763H35
R218	RESISTOR	150.0 .50W 5%	184A763H07
R219	RESISTOR	330.0 .50W 5%	184A763H15
R220	RESISTOR	47.0K .50W 5%	184A763H47
R221	RESISTOR	220.0K .50W 5%	184A763H83
R222	RESISTOR	4700.0 .50W 5%	184A763H43
Q14	TRANSISTOR	2N4249	849A441H03
Q15	TRANSISTOR	2N4249	849A441H03
Q211	TRANSISTOR	2N4249	849A441H03
Z201	ZENER	1N753A 6.2V	862A606H01
Y11	CRYSTAL	SEE NOTE □	
T211	TRANSF.		714B677G01
T212	TRANSF.		205C043G03

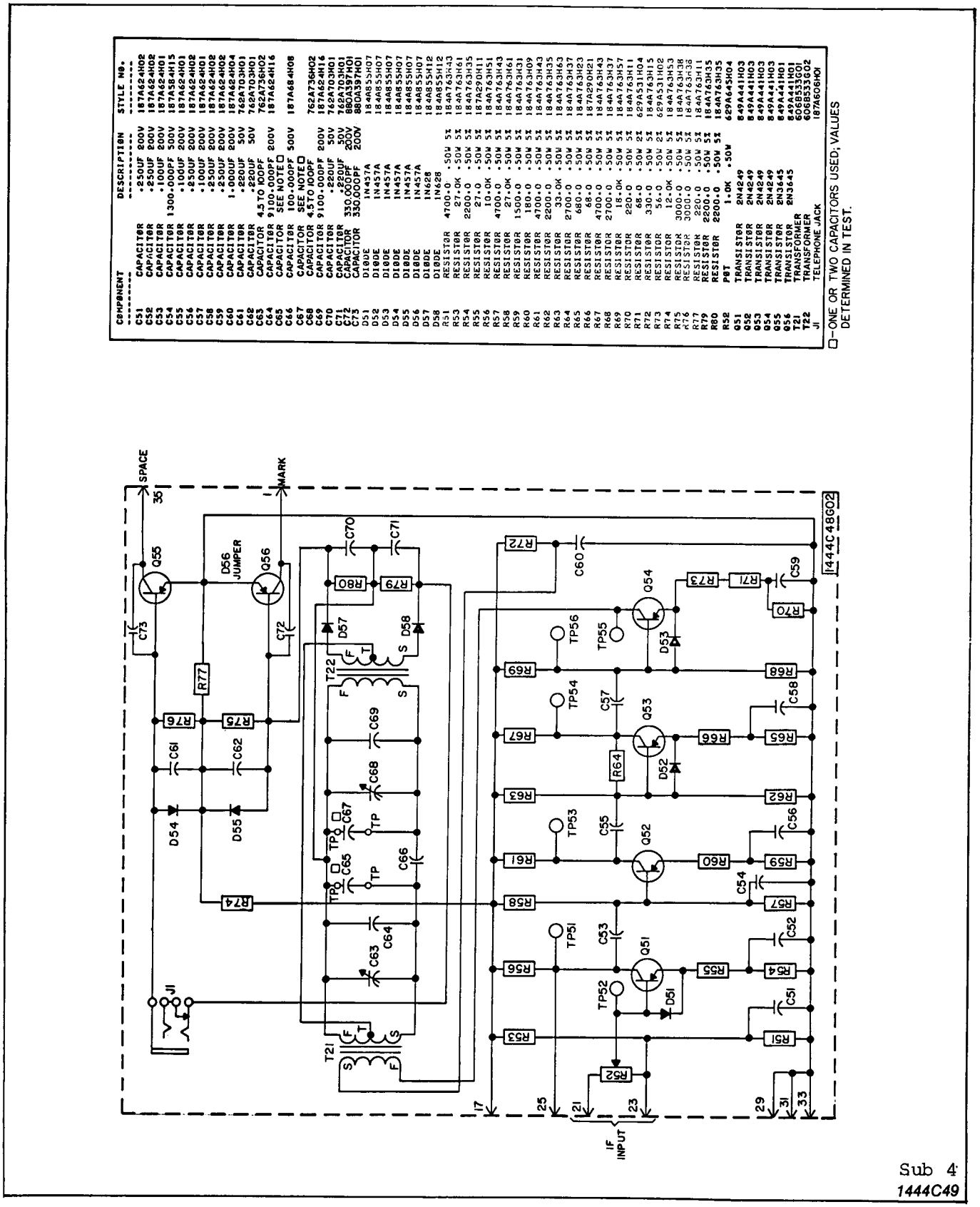
▲ C211 RANGES FROM 100PF TO 1000PF

○ C214 MAY VARY UP TO 100PF 187A695H01 THROUGH H23

□ Y11 FREQ. EQUALS RCVR (CHANNEL) FREQUENCY PLUS 20KHZ

Sub. 1
1458C60

Fig. 16. Internal Schematic 200.5-300Hz. Oscillator and Mixer I.F. Amplifier Module

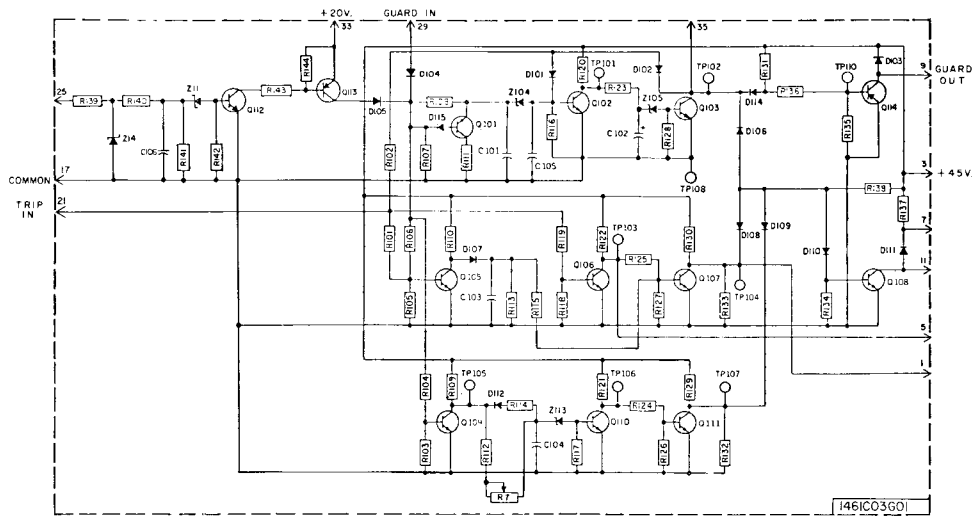


COMPONENT	DESCRIPTION	STYLE NO.
C51	CAPACITOR .250UF 200V	187A624H02
C52	CAPACITOR .250UF 200V	187A624H02
C53	CAPACITOR .100UF 200V	187A624H01
C54	CAPACITOR 1300.000PF 500V	187A584H15
C55	CAPACITOR .100UF 200V	187A624H01
C56	CAPACITOR .250UF 200V	187A624H02
C57	CAPACITOR .100UF 200V	187A624H01
C58	CAPACITOR .250UF 200V	187A624H02
C59	CAPACITOR .250UF 200V	187A624H02
C60	CAPACITOR 1.000UF 200V	187A624H04
C61	CAPACITOR .220UF 50V	762A703H01
C62	CAPACITOR .220UF 50V	762A703H01
C63	CAPACITOR 4.5 TO 100PF	762A736H02
C64	CAPACITOR 9100.000PF 200V	187A624H16
C65	CAPACITOR SEE NOTE □	
C66	CAPACITOR 100.000PF 500V	187A684H08
C67	CAPACITOR SEE NOTE □	
C68	CAPACITOR 4.5 TO 100PF	762A736H02
C69	CAPACITOR 9100.000PF 200V	187A624H16
C70	CAPACITOR .220UF 50V	762A703H01
C71	CAPACITOR 330.000PF 200V	880A397H01
C72	CAPACITOR 330.000PF 200V	880A397H01
C73	CAPACITOR .220UF 50V	762A703H01
D51	DIODE 1N457A	184A855H07
D52	DIODE 1N457A	184A855H07
D53	DIODE 1N457A	184A855H07
D54	DIODE 1N457A	184A855H07
D55	DIODE 1N457A	184A855H07
D56	DIODE 1N457A	184A855H07
D57	DIODE 1N457A	184A855H07
D58	DIODE 1N628	184A855H12
R51	RESISTOR 4700.0 .50W 5%	184A763H43
R52	RESISTOR 27.0K .50W 5%	184A763H61
R53	RESISTOR 2200.0 .50W 5%	184A763H35
R54	RESISTOR 27.0 .50W 5%	187A290H11
R55	RESISTOR 10.0K .50W 5%	184A763H51
R56	RESISTOR 4700.0 .50W 5%	184A763H43
R57	RESISTOR 27.0K .50W 5%	184A763H61
R58	RESISTOR 1500.0 .50W 5%	184A763H31
R59	RESISTOR 180.0 .50W 5%	184A763H09
R60	RESISTOR 4700.0 .50W 5%	184A763H43
R61	RESISTOR 2200.0 .50W 5%	184A763H35
R62	RESISTOR 33.0K .50W 5%	184A763H63
R63	RESISTOR 2700.0 .50W 5%	184A763H37
R64	RESISTOR 680.0 .50W 5%	184A763H23
R65	RESISTOR 68.0 .50W 5%	187A290H21
R66	RESISTOR 4700.0 .50W 5%	184A763H43
R67	RESISTOR 2700.0 .50W 5%	184A763H37
R68	RESISTOR 18.0K .50W 5%	184A763H57
R69	RESISTOR 220.0 .50W 5%	184A763H11
R70	RESISTOR 68.0 .50W 2%	629A531H04
R71	RESISTOR 330.0 .50W 5%	184A763H15
R72	RESISTOR 56.0 .50W 2%	629A531H02
R73	RESISTOR 12.0K .50W 5%	184A763H53
R74	RESISTOR 3000.0 .50W 5%	184A763H38
R75	RESISTOR 3000.0 .50W 5%	184A763H38
R76	RESISTOR 220.0 .50W 5%	184A763H11
R77	RESISTOR 2200.0 .50W 5%	184A763H35
R79	RESISTOR 2200.0 .50W 5%	184A763H35
R80	RESISTOR P8T 1.0K .50W	629A645H04
R52	TRANSISTOR 2N4249	849A441H03
Q51	TRANSISTOR 2N4249	849A441H03
Q52	TRANSISTOR 2N4249	849A441H03
Q53	TRANSISTOR 2N4249	849A441H03
Q54	TRANSISTOR 2N3645	849A441H01
Q55	TRANSISTOR 2N3645	849A441H01
Q56	TRANSFORMER	606B533G01
T21	TRANSFORMER	606B533G02
T22	TELEPHONE JACK	187A606H01
J1		

□-ONE OR TWO CAPACITORS USED; VALUES DETERMINED IN TEST.

Fig. 17. Internal Schematic Amplifier and Limiter Discriminator Module

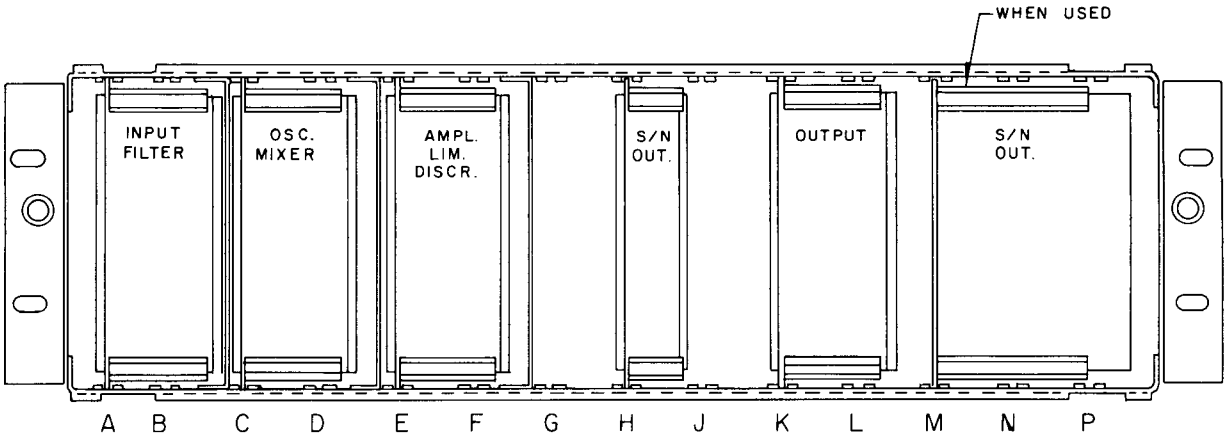
Sub 4
1444C49



COMPONENT	STYLE	REQ	REF
TRANSISTORS			
Q101	849A441H03	1	(2N3393)
Q102-106-110-111	762A585H01	4	(2N696)
Q103	184A638H18	1	(2N697)
Q107	762A585H02	1	(2N698)
Q105-108-109-112-114	184A638H19	5	(2N699)
Q113	849A441H02	1	2N4356
RESISTOR			
R109	187A643H51	1	(10K 1W ±5%)
R137	184A859H06	1	(.870 Ω 3W)
R111	184A763H19	1	(470 1/2W ±5%)
R112-R114-R123	184A763H27	3	(1K 1/2W ±5%)
R135	184A763H39	1	(3.3K 1/2W±5%)
R103-105-116TO118-135 138-126-127-128-134	184A763H51	11	(10K 1/2W ±5%)
R131	184A763H53	1	(12K 1/2W ±5%)
R107	184A763H57	1	(18K 1/2W ±5%)
R104	184A763H61	1	(27K 1/2W ±5%)
R102-124-125-132-133	184A763H63	5	(33K 1/2W ±5%)
R101-106	184A763H65	2	(39K 1/2W ±5%)
R108	184A763H69	1	(56K 1/2W ±5%)
R121-122-129-130	184A763H71	4	(82K 1/2W ±5%)
R115	184A763H73	1	(82K 1/2W ±5%)
R119	184A763H75	1	(100K 1/2W ±5%)
R113	184A763H91	1	(470K 1/2W ±5%)
R120	184A763H65	1	39K 1/2W ±5%
R7	185A086H11	1	250K 1/2W ±5%
R110	187A643H47	1	6.8K 1W ±5%
R139-R140-R144	629A53H48	3	4.7K 1/2W ±2%
R143	629A53H58	1	12K 1/2W ±2%
R141	629A53H78	1	82K 1/2W ±2%
R142	629A53H56	1	10K 1/2W ±2%
CAPACITORS			
C101	184A661H12	1	(4.7MFD 10V)
C105	184A663H02	1	(.05MFD 50V)
C102	184A661H25	1	(6.8MFD)
C103-104	187A624H11	2	(.5MFD ±10%)
C106	849A437H04	1	.047 MFD 200V
DIODES			
D114	182A881H07	1	(1N100A
D101 TO 106-107-111 108-109-110-112-115	184A855H07	13	(1N457A)
DIO-ZENER			
Z105-Z14	185A212H06	2	(1N3686B)
Z113-104, Z11	186A797H06	3	(1N957B)

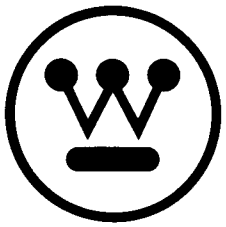
Sub 3
1461C04

Fig. 18. Internal Schematic Logic Board for Transfer Trip Module



Sub. 1
1463C18

Fig. 19. Module Location



WESTINGHOUSE ELECTRIC CORPORATION

RELAY-INSTRUMENT DIVISION

CORAL SPRINGS, FL.

Printed in U.S.A.