PMC PROCESSOR BOARD 1993A23

TABLE OF CONTENTS

EFFECTIVE DATE: DECEMBER 1981

1.0 INTRODUCTION

The PMC Processor Board is an 8086 based microcomputer board designed for general drive controller applications. This board is intended to be used in MICRO-PRODAC systems. The following functions are contained on the board.

1. 8086 CPU (Central Processing Unit)
2. Clock generator
3. Sockets for six Programmable Read Only Memories (PROM's)
4. Random Access Memory (RAM)
5. Programmable Interval Timer (PIT)
6. Programmable Peripheral Interface (PPI)
7. Programmable Interrupt Controller (PIC)

A photograph and block diagram of the PMC board are shown on Figures 1.1 and 1.2 respectively.

No attempt is made in this IL to describe the circuit details of the PMC board. Readers who are interested in the details of 8086 based systems are referred to the 8086 Family Users manual which is available from Intel Corporation.

The PMC board communicates with other boards in the MICRO-PRODAC cage on the MICRO-PRODAC Systems Bus (PSB). This bus is a subset of the IEEE 796 bus (commonly known as the Intel Multibus*).

The board is designed to be used in single master systems. There is no logic on the board for priority resolution required for multi-master systems.

The PMC uses both memory and I/O mapping. Although the 8086 processor can address up to 1 megabyte of memory, only 88K is actually allocated for use. Similarly, of the 64K available in I/O space, only 256 bytes of this space is allocated.

2.0 FUNCTIONAL DESCRIPTION AND PROGRAMMING CONSIDERATIONS

This section describes the PMC board from a functional viewpoint. In addition, programming considerations such as address definitions, initialization commands for the peripheral chips and PROM options are described.

2.1 PMC Memory Allocation

Any 8086 based system has in inherent capability to address 1 megabyte of Memory Mapped space and an additional 64K bytes of I/O Mapped space. Although the 8086 is a word (16 bit) processor, the following memory description will be based on bytes (8 bits). The reason for this is that a byte is the smallest memory unit that the 8086 can address and because the physical memory (hardware) is organized in bytes, not words. In order to simplify hardware and to take advantage of the relatively low memory requirements of a drive controller system, the MICRO-PRODAC system was designed to handle only a portion of this allowed memory space. The memory allocation in a MICRO-PRODAC system is explicitly defined by the PMC board since this board is the only bus controller, and therefore controls the PS bus addressing.

2.2 Memory Mapped Space

The memory mapped space is separated into three functions:

1. PMC on board RAM (4K bytes)
2. PMC on board PROM (24K bytes maximum)
3. PMC access to Multibus (32K bytes for slave boards which decode 16 address bits; 256K bytes for slave boards which decode 20 address bits)

Figure 2.2 shows the location of these three functions in the 1M byte space.

* Multibus is a registered trademark of Intel Corp.

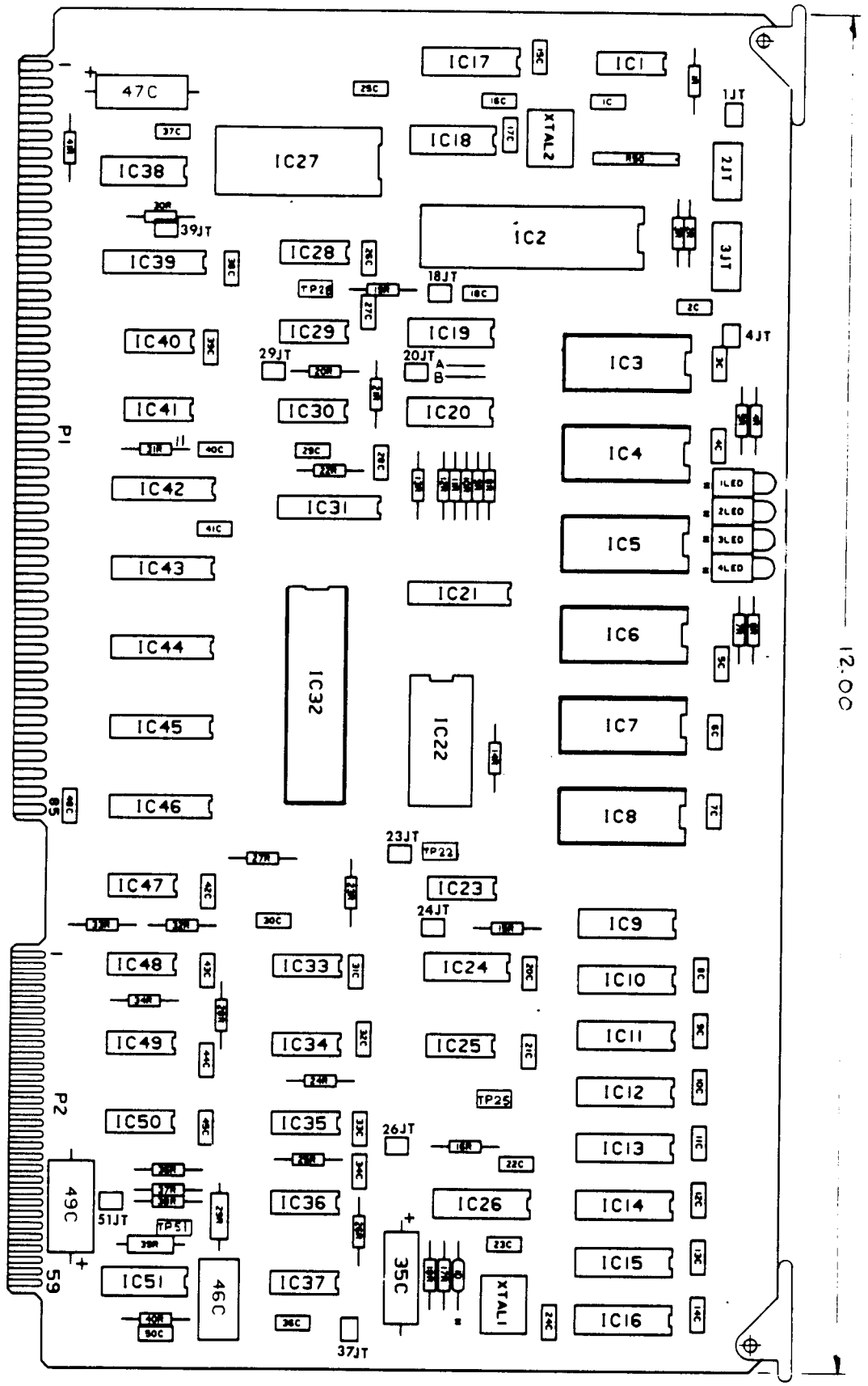

IC17
IC1
47C
IC18
XTAL2
IC27
IC38
IC2
39JT
IC39
IC28
18JT
IC29
IC19
IC40
29JT
20JT
IC3
4JT
IC41
IC30
IC20
IC4
IC42
IC31
IC5
IC43
IC21
IC6
IC44
IC32
IC22
IC45
IC7
IC46
IC8
23JT
TP22
IC47
IC23
24JT
IC9
IC48
IC33
IC24
IC10
IC49
IC34
IC25
IC11
IC12
TP25
IC50
IC35
26JT
IC13
49C
51JT
IC36
IC26
IC14
IC51
46C
IC37
35C
XTAL1
IC15
IC16
37JT
1LED
2LED
3LED
4LED
P1
P2
85
59
12.00

FIGURE 1.1

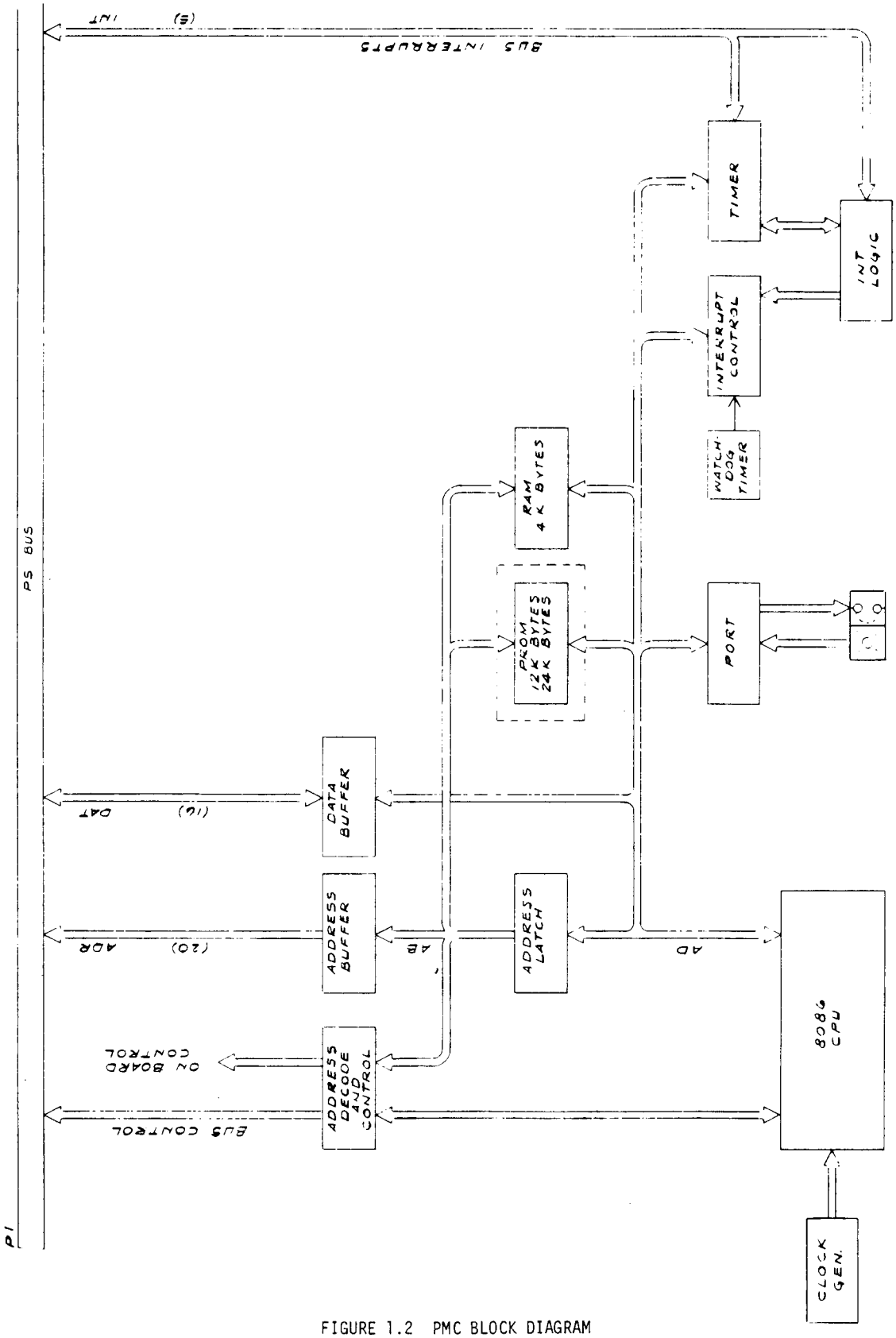


FIGURE 1.2 PMC BLOCK DIAGRAM

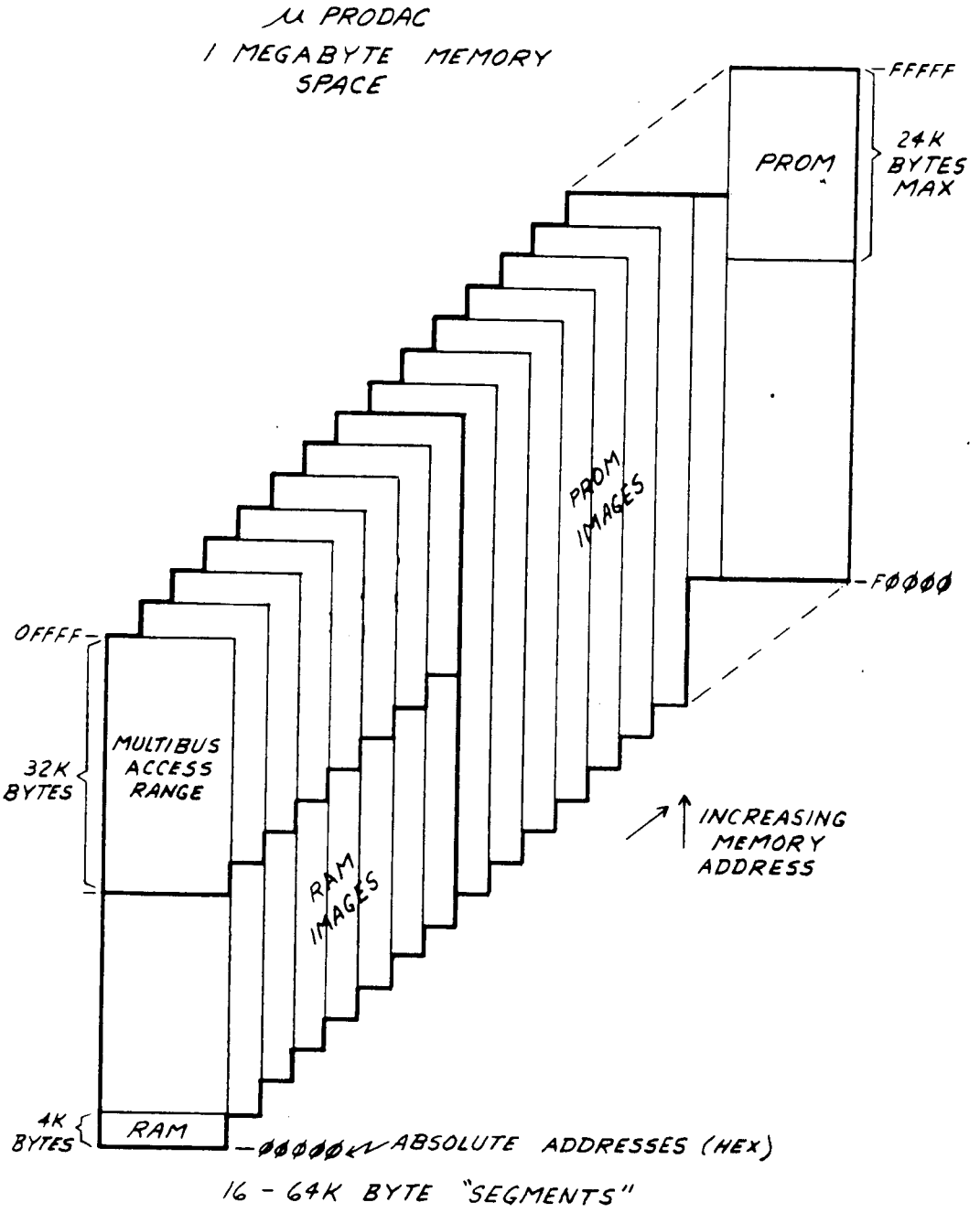

μ PRODAC
1 MEGABYTE MEMORY SPACE
FFFFF
PROM
24K BYTES MAX
PROM IMAGES
F0000
0FFFF
32K BYTES
MULTIBUS ACCESS RANGE
RAM IMAGES
INCREASING MEMORY ADDRESS
4K BYTES
RAM
00000 ABSOLUTE ADDRESSES (HEX)
16 - 64K BYTE "SEGMENTS"

FIGURE 2.2

2.2.1 RAM - Random Access Memory

The 4K bytes of on-board RAM is used for three types of storage:

1. Data Variables
2. Stack Variables
3. Interrupt Vectors

Of these, only the interrupt vectors have locations defined by hardware restrictions. The interrupt vectors must occupy the space beginning at memory location absolute 0000.

The data and stack areas can theoretically reside anywhere in RAM space as long as they do not interfere with the interrupt vectors. In order to maintain consistency, however, the locations defined in table 2.2.1 are normally used.

TABLE 2.2.1

Recommended RAM Space Usage

	Address Range (Absolute Hex)
Interrupt Vectors	00000H - 0009FH
Data Variables	000A0H - 007FFH
Stack Variables	00800H - 00FFF

Figure 2.2.1 shows the RAM space usage in graphical form.

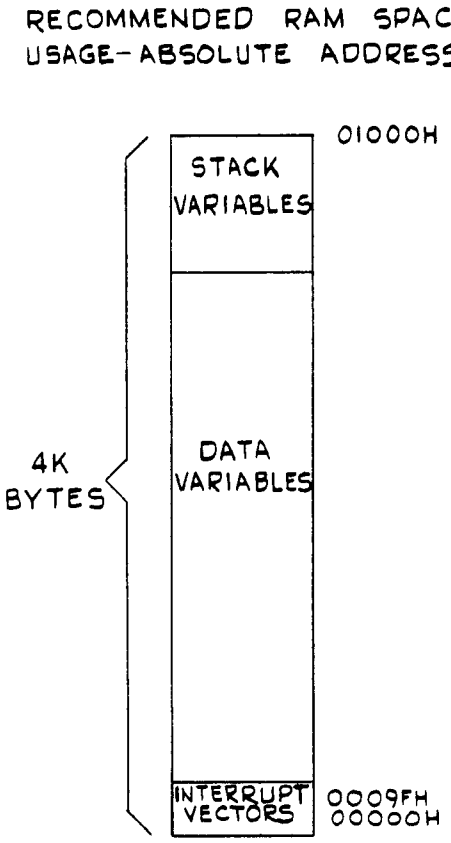


FIGURE 2.2.1

Each interrupt vector requires four bytes of RAM. Therefore, there is space for forty (40) interrupt levels in the recommended RAM allocation for interrupt vectors. The first 32 are either predefined by the hardware or reserved by Intel. Levels 32 through 39 are intended for MICRO-PRODAC interrupt vectors. Further definition of the interrupt vectors is given in section 2.3.1.

2.2.2 PROM - Programmable Read Only Memory

There are sockets for up to six PROM's on the PMC board. The PROM's can be either 2716 type on G01 boards, 2732 type on G02 boards or 2732A type on G03 boards. With 2716's, the maximum PROM space is 12K bytes; with 2732's, or 2732A's, the maximum PROM space is 24K bytes. PROM's must be installed in pairs in order to satisfy the 16 bit wide word constraint of the 8086 processor. These PROM's occupy the high end of the 1 megabyte of address space. They are located here because the starting address of the 8086 after a hardware reset is near the upper end of memory space at address OFFFFOH.

Table 2.2.2 lists the address range occupied by the PROM's. When fewer than 6 PROM's are required in a system , the PROM's should be installed in the order listed, i.e. IC5 and IC8, then IC4 and IC7 and finally IC3 and IC6. This guarantees that there is PROM at the restart address of the 8086.

TABLE 2.2.2
PROM ADDRESS RANGE

	ODD ADDRESSES	EVEN ADDRESSES	PROM TYPE	
			2716 (12K BYTES MAX)	2732 or 2732A (24K BYTES MAX)
1.	IC 5	IC 8	OFF000 - OFFFFFH	OFE000H - OFFFFFH
2.	IC 4	IC 7	OFE000H - OFEFFFH	OFC000H - OFDFFFH
3.	IC 3	IC 6	OFD000H - OFDFFFH	OFA000H - OFBFFFH

2.2.3 PS Bus Access

The PMC board drives 20 address lines onto the PS bus. A total of 256K bytes of address space is reserved for PS bus accesses, although only the first 32K (from 08000H to OFFFFH) is intended to be used for standard MICRO-PRODAC systems. (See figure 2.2).

2.3 I/O Mapped Space

I/O mapped space on the PMC card is used to interface with the on-board peripherals (Port, Timer and Interrupt Controller). All space not used for on-board I/O (or images thereof) is available for I/O mapped accesses. However, I/O mapping in general should not be used for MICRO-PRODAC systems. This capability was provided on the PMC board only to be consistent with other Multibus compatible boards.

Only 8 of the 16 I/O address bits on the PMC board are decoded and therefore only 256 bytes of I/O space can be used. Of these 256 bytes, 32 bytes are reserved for PMC on-board addresses leaving 224 bytes for PS Bus access.

Figure 2.3 shows the allocation of I/O space in a MICRO-PRODAC system. Table 2.3 lists the I/O addresses of the on-board peripheral chips.

TABLE 2.3
PMC I/O FUNCTIONS

CHIP	I/O ADDRESS*	FUNCTION
8259A PIC Programmable Interrupt Controller	00C0	Write: ICW1, OCW2 & OCW3 Read: Status and Poll
	00C2	Write: ICW2, ICW3, ICW4, OCW1 (Mask) Read: OCW1 (Mask)
8255A PPI Programmable Peripheral Interface	00C8	Write: Not Allowed Read: Port A
	00CA	Write: Port B Read: Not Allowed
	00CC	Write: Port C Read: Port C Status
	00CE	Write: Control Read: None
8253 PIT Programmable Interval Timer	00D0	Write: Counter 0 (Load Count) Read: Counter 0
	00D2	Write: Counter 1 (Load Count) Read: Counter 1
	00D4	Write: Counter 2 (Load Count) Read: Counter 2
	00D6	Write: Control Read: None

* Address between 00C0 and 00DF not listed in the table are illegal.

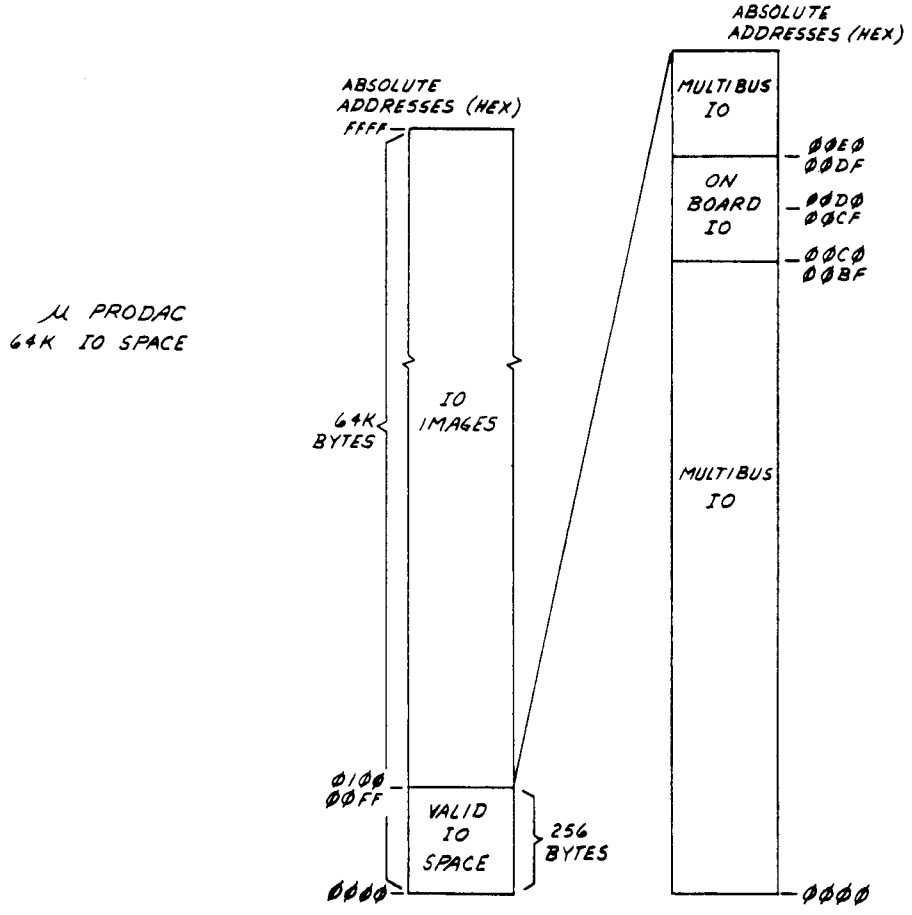


FIGURE 2.3

Printed in USA

2.3.1 Interrupt Control

The PMC board was designed to handle eight user interrupts in addition to the five interrupts built into the 8086 itself. Table 2.3.1 lists the interrupts available on the PMC board.

The five built-in interrupts (levels 0-4) are software functions, except for Power Fail Interrupt (PFI/), and programmers must make provisions for handling these interrupts.

The eight user interrupts (level 32-39) are hardware interrupts which are handled through a 8259A Programmable Interrupt Controller (PIC) chip.

Three of these interrupts have dedicated functions; five are wired to the PS Bus for general user defined application. With the standard mode control of the 8259A, the priority of the interrupts corresponds to the level, i.e. level 32 has the highest priority, level 39 has the lowest priority.

TABLE 2.3.2
PMC Interrupts

Interrupt Level	Type	Location (Hex)	Description/Source
0	8086 Internal	0000	Divide Error
1	8086 Internal	0004H	Single Step
2	Hardware	0008H	Power Fail Interrupt PFI/Nonmaskable)
3	8086 Internal	000CH	One Byte Interrupt
4	8086 Internal	0010H	Interrupt on Overflow
5-31			RESERVED BY INTEL
32	8259 PIC	0080H	Watchdog or Multibus INT0/
33		0084H	Timeout
34		0088H	Multibus INT1/
35		008CH	Multibus INT2/
36		0090H	TMR0/ from 8253 Timer Chip
37		0094H	Multibus INT3/
38		0098H	Multibus INT4/ or External Interrupt on P2
39		009CH	Multibus INT5/

2.3.1.1 PIC Programming

A complete description of the programming considerations for the 8259A PIC is given in the Intel Peripheral Design Handbook (Intel Cat. No. 9800676B). What follows is the suggested standards and definitions of PIC mode control for a MICRO-PRODAC system.

In order to set up the 8259 interrupt controller, three initialization control words (ICW1, ICW2 & ICW4) must be written in sequence to the 8259. ICW3 is not used when only a single 8259 is used, as is the case on the PMC board. The operation control words are (OCW1, OCW2 & OCW3) used to set masks, indicate end of interrupt, and set priorities. The control words to the 8259 are I/O mapped and are described in Table 2.3.1.1.

Before enabling interrupts, the three initialization control words to the PIC and the address vectors for interrupt servicing should be set up.

TABLE 2.3.1.1
8259A PIC Control Words

Control Word	I/O Address	Value	Function
ICW1	00C0H	FFH	Sets: a. 8086 mode b. Level triggered input c. Single 8259
ICW2	00C2H	20H	Sets address range of interrupt vectors at 0080H.
ICW4	00C2H	0FH	Sets: a. 8086 processor b. Buffered mode c. Automatic End of Interrupt EOI
OCW1 (Mask)	00C2H	Variable	Sets interrupt masks. Bits correspond to interrupt levels, i.e. Bit 0 (LSB) sets mask on interrupt level 32. Bit 7 (MSB) sets mask on interrupt level 39. Note: one's sets the mask, zero's clears the mask. This implies that zeros enables the corresponding interrupt.
OCW2	00C0	20H	End of Interrupt Command
OCW3	Normally not used in MICRO-PRODAC. See 8259 descriptive literature.		

2.3.2 Port Control

An 8255 Programmable Peripheral Interface (PPI) provides status and control function on the PMC board. These functions are tabulated in Table 2.3.2. Port A is for PMC board ID and configuration codes. The ID code for the PMC board is 1XH. Pullups are used on the least significant four bits of this code so the ID code is 1FH.

The 8255 PPI must be initialized by sending a control byte to I/O address 00CEH. Valid control bytes are given in Table 2.3.2. All four of these control bytes program Port A for input and Port B for output. Port C may be programmed for either all input or output or split four bits each. Control byte = 99H is the recommended value since it programs Port C in the input (safe) mode.

Port B is used for the LED indicators and control functions. The LED indicators must be enabled by writing a "0" to bit 7 of Port B. The "OK" LED is used for board "I'm OK" indication. "WD" is reserved for watchdog timer timeout indication; "T1" and "T2" are available for general test and indicating functions. All four LED's are controlled through software.

TABLE 2.3.2

PPI Functions

Port	I/O Address	Function
A	00C8	Read: Board ID & Configuration Code G01 - 01DH G02 - 01FH G03 - 01EH
B	00CA	Write: LED Indicators & Controls Bit 0 "OK" LED Bit 1 "WD" LED (Watchdog) Bit 2 "T1" LED (Test 1) Bit 3 "T2" LED (Test 2) Bit 4 Gate 1 (Counter #1) Bit 5 Reset Interrupt 36./ Bit 6 Watchdog Timer Trigger Bit 7 LEDENABLE/
C	00CC	General Purpose Port
Control	00CE	Allowed Control Bytes Port A - Input Port B - Output Control Byte — Port C Configuration 90 - PC_0 - PC_7 Output 91 - PC_0 - PC_3 In, PC_4 - PC_7 Out 98 - PC_0 - PC_7 Out, PC_4 - PC_7 In 99*- PC_0 - PC_7 In * Recommended default value

Two control functions, "Gate 1" and "Reset Interrupt 36/" are also included on Port B. "Gate 1" feeds the gate input of counter #1 on the 8253 programmable timer chip. This provides capability for operating one of the counters on the 8253 in gated mode. "Reset Interrupt 36/" clears the flip-flop which is set by counter #0 of the 8253 timer chip. This flip-flop, which feeds the 8259 interrupt controller, is used to provide interface for level triggered interrupts.

Port C is a general purpose port which is provided primarily for board production test purposes. Standard functions for this port have not been defined.

NOTE: The following software restriction must be observed when addressing the 8255. The recovery time between commands (any read or write) of the 8255 is 1 usec. This means that on the PMC board no two consecutive instructions can address the 8255. There must always be at least one instruction between any two instructions which address the 8255.

2.3.3 Programmable Interval Timer

The 8253 Programmable Interval Timer (PIT) has three programmable counter/times. On the PMC board counter #0 is connected to a flip-flop which feeds the 8259 interrupt controller. This counter is intended for basic cycle timing. Counters #1 and #2 are connected to the P2 connector. These two counters are available for general purpose timing and/or counting requirements. Counter #1 can be controlled by its gate input which is connected to the 8255 port. The other two counters have their gate inputs tied high (i.e. always enabled).

The clock (TCLK) to the 8253 operates at 1.536 MHZ (.65104 usec period). This gives a count range of 0.65104 usec to 42.666 msec.

NOTE: The following software restriction must be observed when addressing the 8253. The recovery time between commands (any read or write) of the 8253 is 1 usec. This means that on the PMC board no two consecutive instructions can address the 8253. There must always be at least one instruction between any two instructions which address the 8253.

3.0 Diagnostics and Card Replacement

3.1 Diagnostics

The software for MICRO-PRODAC systems includes software modules which are used to check the operation of the PMC (and other boards) in the system. These diagnostic software modules are automatically executed after a power on or reset condition. At the end of the execution of the diagnostic module, the software turns on the green "OK" LED on the PMC board if no failures have been detected. Otherwise the "OK" LED is left off indicating that a malfunction was detected by the diagnostic software.

3.2 Card Replacement

If the "OK" LED on the PMC card fails to come on after a power on or reset condition, then the card should be replaced with a spare card. The spare card should have exactly the same drawing number and group number suffix as the original card (i.e. 1993A23G01 for 2716 PROM's). When replacing a PMC card, one should also verify that the PROM's on the spare card are exactly the same drawing number and revision number as the original PROM's, and that the location of the PROM's is correct. This information is written on the PROM's as indicated in Figure 3.1 No adjustment or jumper changes are required when replacing a PMC board as long as the spare board has PROM's installed.

If spare PROM's are not available, then the PROM's from the original card must be transferred onto the spare card in the exact location and orientation as on the original card.

Great care should be taken when installing PROM's. Check that each lead on the chip is properly seated in the socket and make sure that the orientation is correct per Figure 3.2. PROM's which are installed backwards will be destroyed when power is applied.

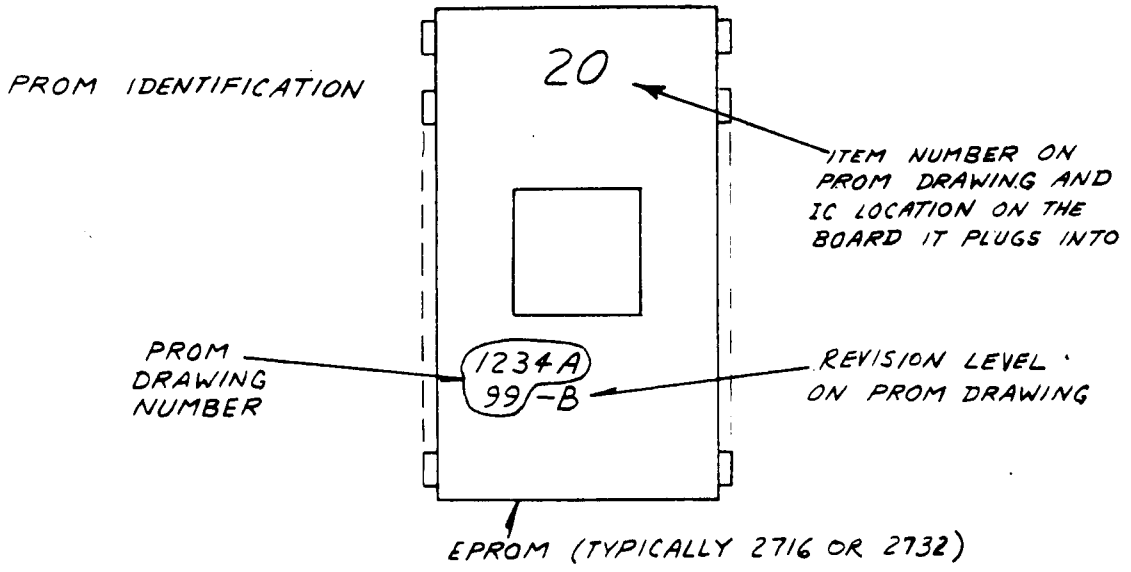
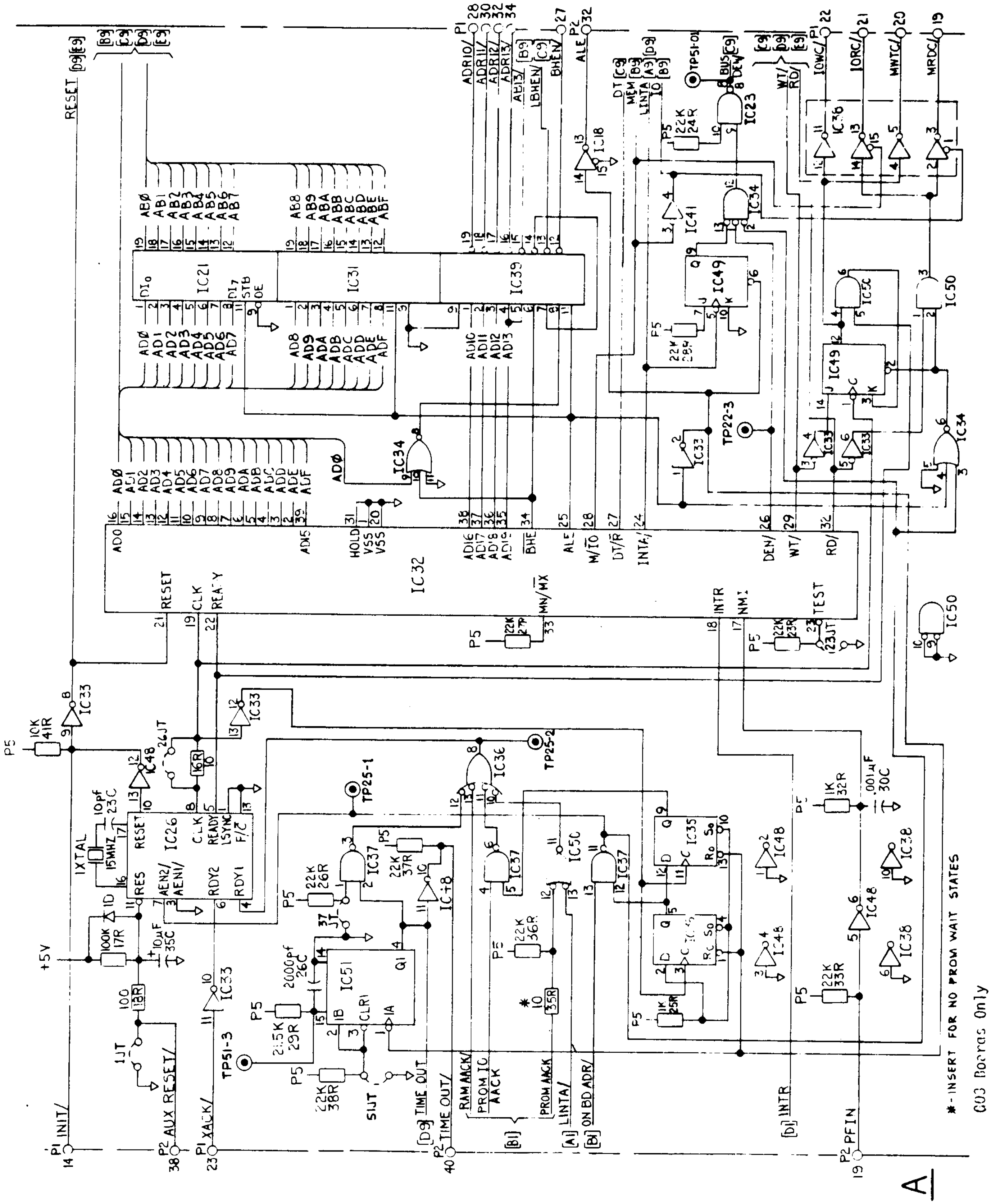
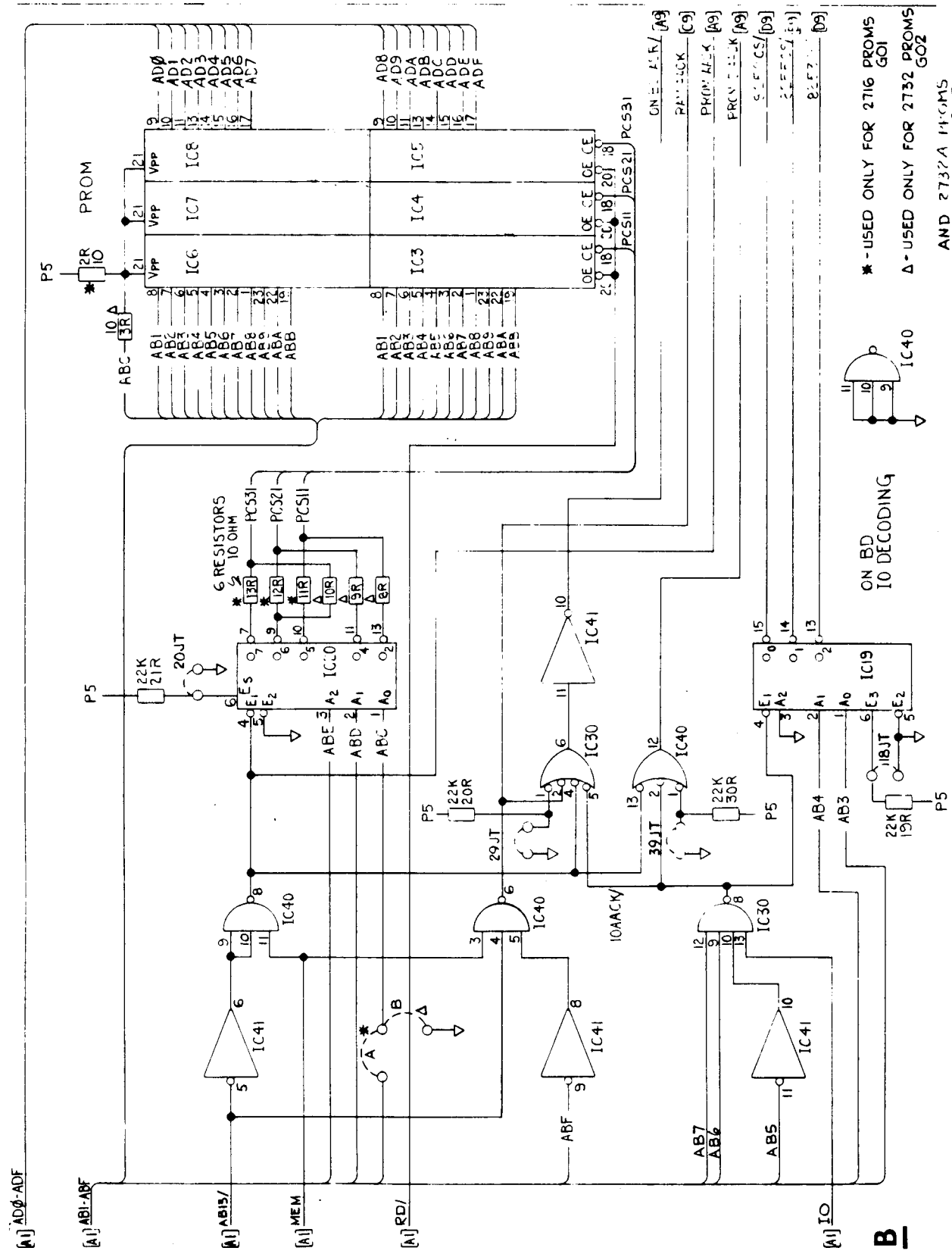
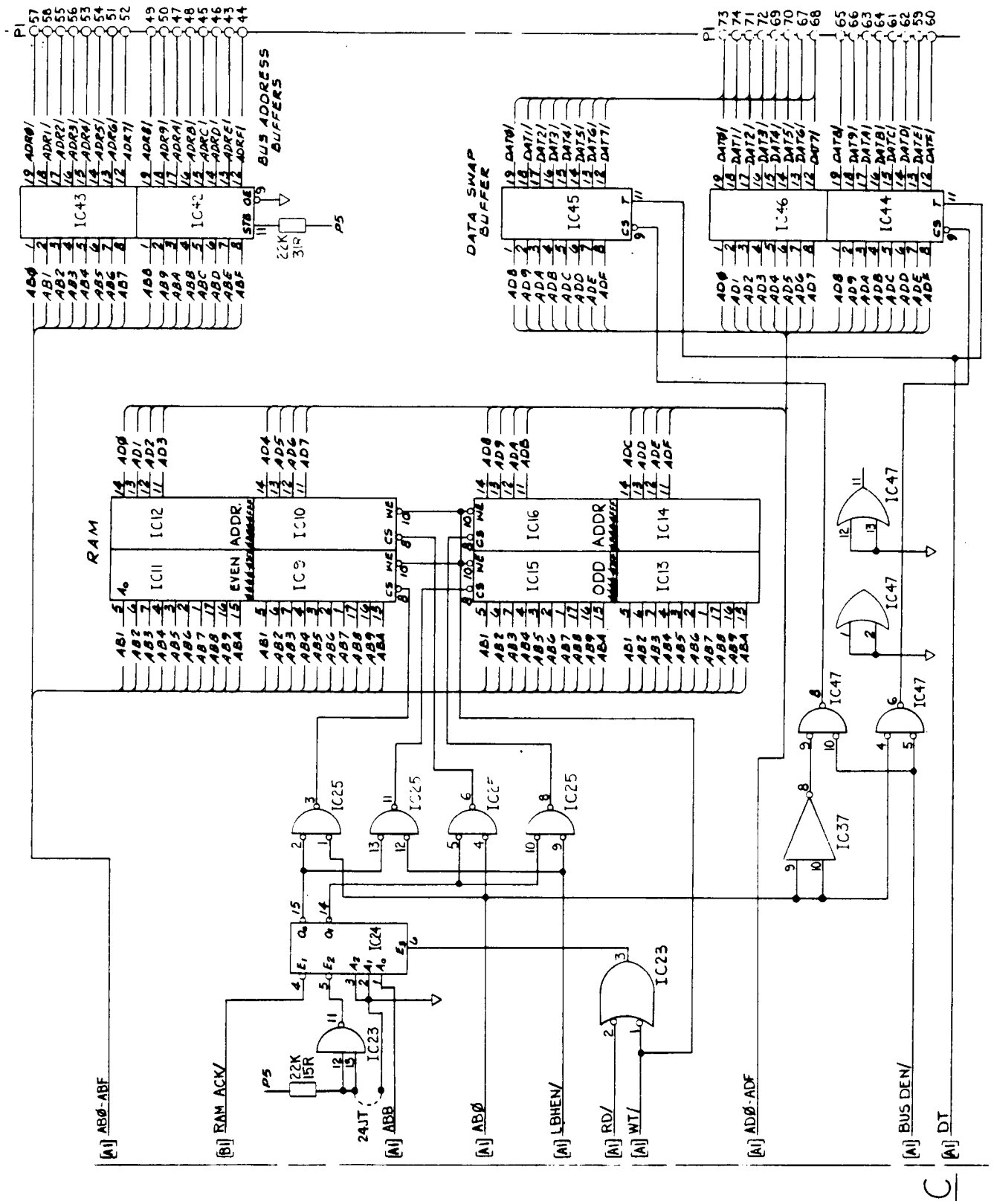
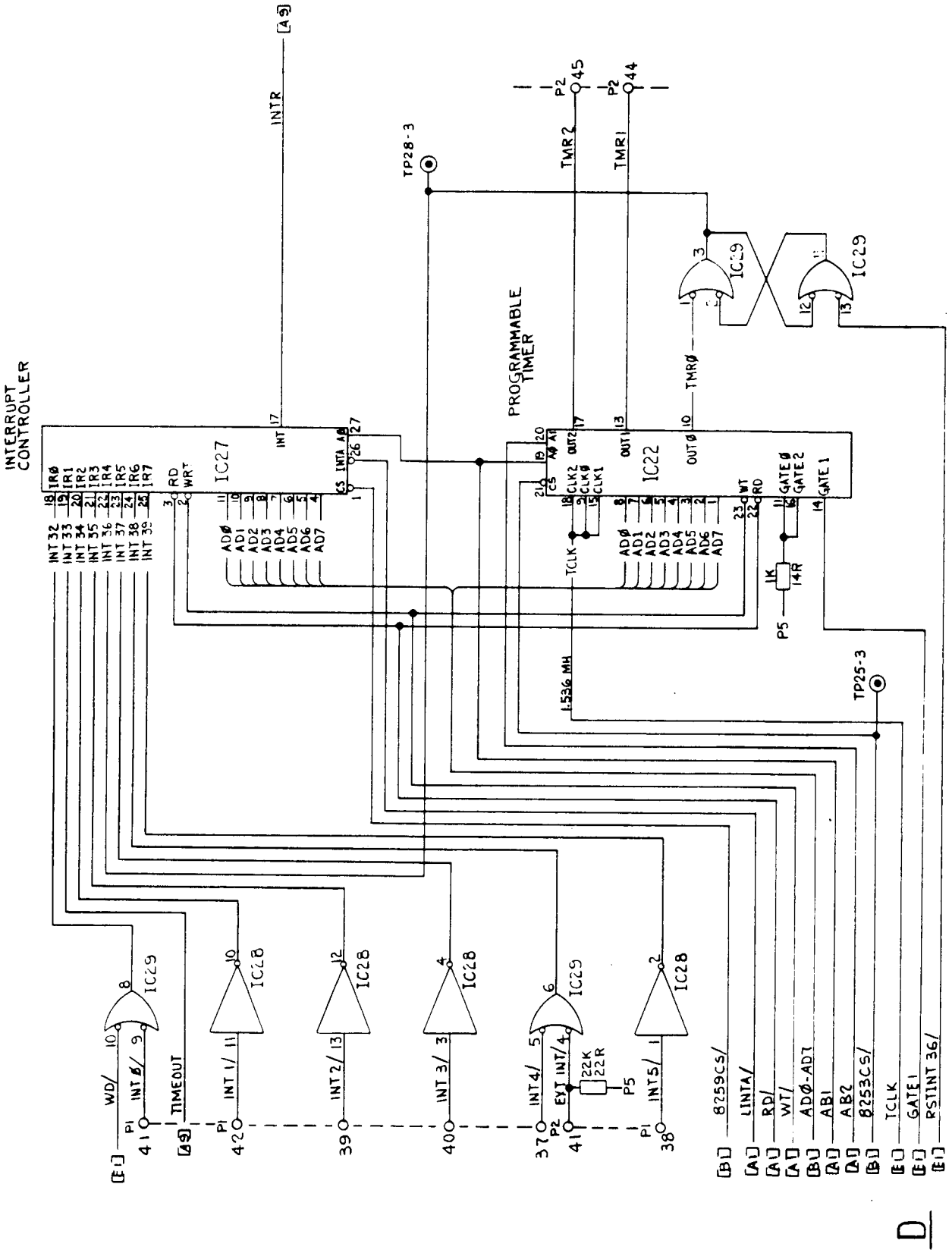


FIGURE 3.1

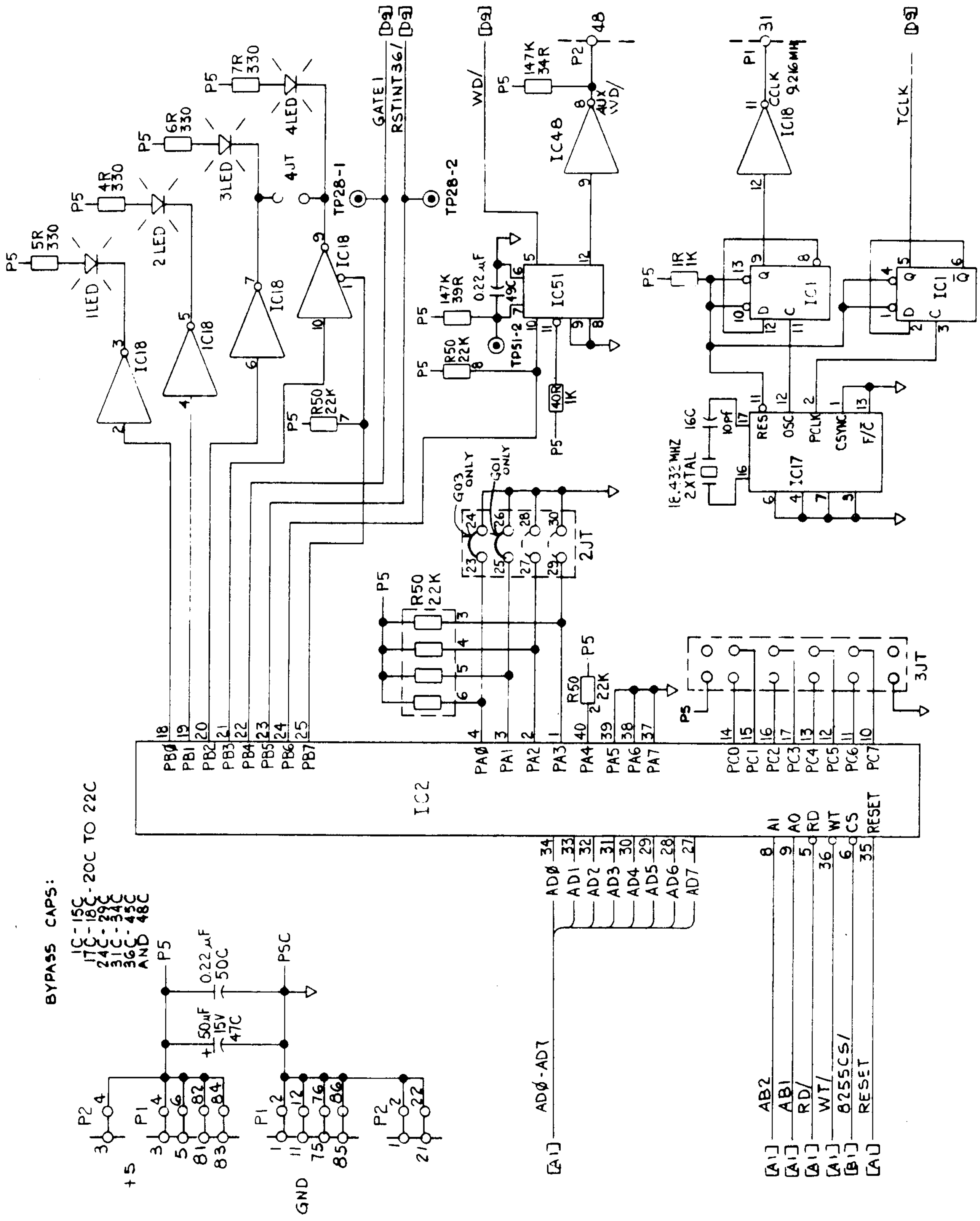

RESET
AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7
AB8 AB9 ABA ABB ABC ABD ABE ABF
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
AD8 AD9 ADA ADB ADC ADD ADE ADF
IC21
IC31
IC39
IC32
IC26
IC51
IC34
IC23
IC41
IC49
IC50
IC36
IC33
IC48
IC37
IC35
IC38
ADR10/
ADR11/
ADR12/
ADR13/
BHEN/
ALE
DT/R
M/IO
INTA/
DEN/
WT/
RD/
IOWC/
IORC/
MWTC/
MRDC/
HOLD
VSS
CLK
READY
MN/MX
INTR
NMI
TEST
1XTAL
15MHZ
TP51-3
TP25-1
TP25-2
TP22-3
TP51-01
P1 INIT/
P2 AUX RESET/
P1 XACK/
TIME OUT/
RAM AACK/
PROM IC AACK
PROM AACK
LINTA/
ON BD ADR/
INTR
P2 PFIN
*-INSERT FOR NO PROM WAIT STATES
C03 Boards Only
A


PROM
IC6
IC7
IC8
IC3
IC4
IC5
6 RESISTORS 10 OHM
IC10
IC19
IC30
IC40
IC41
ON BD IO DECODING
ADDR DECODING & PROM
* - USED ONLY FOR 2716 PROMS G01
Δ - USED ONLY FOR 2732 PROMS G02
AND 2732A PROMS G03
B1


BUS ADDRESS BUFFERS
DATA SWAP BUFFER
RAM
ADDR. EVEN
ADDR. ODD
IC43
IC42
IC45
IC46
IC44
IC12
IC11
IC10
IC9
IC16
IC15
IC14
IC13
IC25
IC24
IC23
IC47
IC37
22K 15R
22K 3R
P5
P1
ABØ-ABF
RAM ACK/
ABB
ABØ
LBHEN/
RD/
WT/
ADØ-ADF
BUS DEN/
DT


INTERRUPT CONTROLLER
IC27
INTR
PROGRAMMABLE TIMER
IC22
TP28-3
TP25-3
TMR2
TMR1
TMR0
P2
45
44
IC29
IC28
INT 32
INT 33
INT 34
INT 35
INT 36
INT 37
INT 38
INT 39
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
TCLK
1.536 MH
1K
14R
P5
22K
22R
WD/
INT 0
TIMEOUT
INT 1/
INT 2/
INT 3/
INT4/
EXT INT/
INT5/
8259CS/
LINTA/
RD/
WT/
AD0-AD1
AB1
AB2
8253CS/
TCLK
GATE1
RSTINT 36/

D


BYPASS CAPS:
1C-15C, 17C-18C-20C TO 22C
24C-29C
31C-34C
36C-45C
AND 48C
P5
PSC
0.22 µF
50C
50µF
15V
47C
+5
GND
P1
P2
AD0-AD7
AB2
AB1
RD/
WT/
8255CS/
RESET
IC2
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
A1
A0
RD
WT
CS
RESET
IC18
1LED
2LED
3LED
4LED
5R 330
4R 330
6R 330
7R 330
4JT
TP28-1
TP28-2
GATE1
RSTINT36/
WD/
IC51
IC48
AUX WD/
147K 34R
147K 39R
0.22 µF
49C
TP51-2
R50 22K
40R 1K
G03 ONLY
G01 ONLY
2JT
3JT
IC17
RES
OSC
PCLK
CSYNC
F/C
16.432 MHZ
2XTAL
16C
10pF
IC1
1R 1K
CCLK 9.216MHZ
TCLK

IC POWER SUPPLY TABLE			
IC	TYPE	P5 (+5)	PSC
1, 35	LS74	14	7
2	8255A	26	7
3 TO 8	2716/2732	24	12
9 TO 16	2114	18	9
17, 26	8284	18	9
18, 38	8098	16	8
19, 20, 24	8205	16	8
21, 31	8282	20	10
22	8253	24	12
23, 29, 37	LS00	14	7
25, 47	LS32	14	7
28, 33, 41	LS04	14	7
30, 36	LS20	14	7
50	LS08	14	7
40	LS10	14	7
34	LS27	14	7
49	LS73A	4	11
51	LS123	16	8
27	8259A	28	14
32	8086	40	1,20
39, 42, 43	8283	20	10
44, 45, 46	8287	20	10
48	TTLØ6	14	7

APPENDIX B

PMC Board Specifications

1.	Memory Capacity	
	On-Board RAM	4K Bytes Static
	On-Board PROM	Sockets for six PROM's 12K bytes max on G01 boards (2716 PROM's) 24K bytes max on G02 boards (2732 PROM's)
2.	CPU Clock Frequency	5 MHZ
3.	PS Bus CCLK Frequency	9.21 MHZ
4.	Interval Timer (8253) Input Frequency	1.536 MHZ
5.	Interrupts	Eight levels of hardware interrupt. Defined per Table 2.3.1.
6.	Memory Timing	
	On-Board RAM Cycle Time	800 usec max.
	On-Board PROM Cycle Time	1200 usec max. - G01 or G02 (2716 or 2732 EPROMS) 800 usec - G03 (2732A EPROMS)
7.	Watchdog Timeout Time	14.5 msec ±25%
8.	Timeout Timer Time	22 usec ±10%
9.	Power Supply Requirements	5 VDC ±5% 2.0A Typical 3.28A Max.