INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE STU-12 TRANSFER TRIP RELAY FOR A WEAK FEED TERMINAL

CAUTION: It is recommended that the user of this equipment become acquainted with the information in either these instructions or the system instruction leaflet 40-205.1 before energizing this relay. Failure to observe this precaution may result in damage to the equipment. Before putting the relay into service, operate the relay to check the electrical connections.

Do not remove or insert printed circuit boards while the STU-12 relay is energized.

APPLICATION

The type STU-12 relay is a solid state directional comparison permissive overreaching transfer trip auxiliary relay for use with solid state or electromechanical distance relays, and a frequency shift type TCF carrier or TA-3 tone channel. This relay will prevent tripping for faults external to the protected line section to which it is applied and permit high speed simultaneous tripping for internal faults. The relay will respond to indications of fault direction and distance provided by the phase and ground distance relays thereby, controlling the transmission of a trip signal and the initiation of high speed tripping for internal faults.

The relay described in this instruction may be applied to two or three terminal lines to provide high-speed simultaneous clearing of all line terminals, even though one or more of these fails to deliver a meaningful amount of fault current. A forward reaching relay of at least one terminal must operate for the internal fault.

CONSTRUCTION

The STU-12 relay is mounted on a standard 19" wide panel 5-¼" high (3 rack units) with edge slots for mounting on a standard relay rack or panel. For the outline and drilling plan refer to Fig. 43.

A hinged and removable door on the front of the chassis covers the printed circuit boards. The photograph in Fig. 1 shows the front view of the relay with the door open. A sealing post at the top center in front may be used to lock and seal the relay when in service.

The rear panel consists of a hinged door which may be opened to expose various components mounted inside. Mounted on the hinged door are two AR type auxiliary relays and, when used, two AL telephone type relays. The AR relay is a small high-speed attracted armature type of unit. An insulated member, fastened to the free end of the armature, draws down four moving contact springs to close or open the contacts when the relay coil is energized. This relay is available for inspection by removing the locking screw and swinging the hinged door outward. In the AL relays, an electromagnet attracts a right-angle iron bracket which in turn operates a set of make or break contacts.

Four power supply resistors are mounted in the rear housing of the chassis. In addition, one 32 terminal connector, J1, and two, (4) terminal, terminal blocks are mounted on the rear of the panel. The photo in Fig. 2 shows the rear view of the STU-12 relay with the top cover off and rear door open.

All of the circuitry suitable for mounting on printed circuit boards is contained in an enclosure behind the front door. The printed circuit boards slide into position in slotted guides at the top and bottom of the enclosure, and engage a terminal block at the rear of the compartment. Each board and terminal block are keyed so that they cannot be accidently inserted into the wrong slot location. A handle mounted on the front end of the board is used for identification, and for removing and inserting the circuit. In addition the handles also serve as a bumper with the front door to prevent the board from becoming disconnected from its terminal block. The boards may be removed for replacement purposes or for use in conjunction with a board extender (Style No. 849A534G01) which permits access to the boards test points and terminals for making measurements while the relay is energized

SUPERSEDES I.L. 41-959.71
*Denotes change from superseded issue.

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Fifteen (15) printed circuit boards are used in the STU-12 chassis. The location and title of the printed circuit boards are shown on the relay component location drawing, Fig. 3.

Printed Circuit Boards

Following is a description of all the printed circuit boards used in the STU-12 relay. Refer to the functional relay logic shown in Fig. 4, 5, 6, and 7. The internal schematics associated with the printed circuit boards contain a detailed NOR/NAND logic diagram to simplify understanding of the transistor logic.

For those users not generally acquainted with logic circuit notation or with device symbols of those components used in the STU-12 drawings, it is recommended that a copy of Westinghouse instruction leaflet. I.L. 41-000-1 entitled SYMBOLS FOR SOLID STATE PROTECTIVE RELAYING be consulted.

Power Supply Board

The Power Supply board located in slot A contains two 20 volt transistor regulators: These voltage regulators will operate from a nominal battery supply of 48 or 125 volts dc by varying resistors RA, RB, RC and RD mounted in the rear of the chassis. The location of components on this board is shown in Fig. 8, and the internal schematic is Fig. 9.

Weak Feed Logic 1 Board

The Weak Feed (W.F.) Logic-1 board located in slot B contains logic to provide tripping and keying by the forward reaching relays (21NP(67N) or 21P and to provide indication of loss of ac potential if either 21S or 21NS(67NS) inadvertantly operates for a sustained period of greater than 500 milliseconds.

In relays for use with electromechanical systems a relay driver is provided on this board to energize the Loss of Potential AL telephone relay mounted in the rear of the chassis. A contact bounce circuit is also provided to override bounce in the contacts of 21P or 21NP(67N).

Location of components on this board is shown in Fig. 10. Two internal schematics are used: Fig. 11-for use with electro-mechanical systems and Fig. 12 for use with solid state systems.

Weak Feed Logic-2 Board

The Weak Feed (W.F.) Logic-2 board located in slot C contains some of the logic to control echo keying. This board provides interface with the undervoltage relay (27). There are two buffered inputs, one for IA/IC, another for 21S- which work into an AND circuit, whose output will block echo keying and trip. A memory circuit on this board provides echo-key blocking after the 10/0 timer operates even if 21S and IA/IC reset.

Location of components on this board is shown in Fig. 13, and the internal schematic in Fig. 14.

Weak Feed Logic-3 Board

The Weak Feed (W.F.) Logic-3 board located in slot D contains some of the logic to set up breaker tripping at the weak source terminal. An output from the 4 input AND on this board is one of the conditions required for trip. Other logic, including the 0/50 millisecond timer, is used to supervise tripping.

A contact bounce circuit is required for electromechanical systems to override bounce which could delay tripping.

Location of components on this board is shown in Fig. 15. Two internal schematics are used: Fig. 16-for electromechanical systems and Fig. 17-for solid state systems.

Weak Feed Locic-4 Board

The Weak Feed (W.F.) Logic 4 board located in slot E contains logic to both provide or block echo keying. An output from the 3 input AND on this board will start echo keying, but if an output is received from the 4 input OR, the 4/80 millisecond timer will pickup and block echo keying.

The memory circuit comprised of an AND and OR is used to block echo keying when the breaker is open and the undervoltage relay (27) operates.

Location of components for this board is shown in Fig. 18, and the internal schematic is in Fig. 19.

Channel Interface Boards

The Channel Interface boards located in Slot F

(Channel 1) and Slot G (Channel 2-when used) contain the buffered interface logic for connection with the channel equipment and provide the outputs to work into the Channel Trip and Supv. boards. In addition, the TA-3 Channel Interface board contains buffered outputs.

An interlock feature is also included in order to convert from a 2 to 3 terminal line relay and conversely. CHANNEL TWO INTERFACE board in slot G must be used in the relay for THREE TERMINAL applications, but MUST BE REMOVED for TWO TERMINAL LINE systems.

A conversion kit may be ordered to change a 2 TERM LINE relay to 3 TERM LINE. This kit includes instructions, nameplate and a CHANNEL INTERFACE BOARD.

The location of components for both the TA-3 and TCF-CHANNEL INTERFACE boards is shown in Fig. 20. Internal schematics are shown in Fig. 21 for the TA-3 CHANNEL and Fig. 22 for the TCF CHANNEL.

Channel Trip Boards

The CHANNEL TRIP board located in slot H contains the connecting logic between the channel trip signals and the remainder of the relay logic. A buffered output for channel 1 and 2 trip is included on this board.

The TONE CHANNEL TRIP board also has additional logic comprised of two AND's and an OR for a guard return function. This logic is inherent to the TCF channel equipment, therefore it is not required in this relay.

Location of components on this board is shown in Fig. 23. Two internal schematics are used; TONE CHANNEL TRIP BOARD - Fig. 24, TCF CHANNEL TRIP BOARD - Fig. 25.

Channel Supervision Board - TCF Channel

The Channel Supervision board for a TCF Channel is located in slot I and contains the connecting logic between the supervisory functions of the channel equipment and the remainder of the relay logic. Both LOW SIGNAL CLAMP outputs work into an OR, as do both CHECK TRIP outputs.

For electromechanical systems, a relay driver is used for energizing a loss of channel AL telephone relay.

The location of components for this board is shown in Fig. 29, and the internal schematic in Fig. 30.

Channel Supervision Board - Tone Channel

The Channel Supervision board for a TONE channel is located in slot I and contains the connecting logic between the supervisory functions of the channel equipment and the remainder of the relay logic. A 150/100 millisecond time delay and associated logic is used to monitor the LOW SIGNAL CLAMP outputs for loss of channel. For electromechanical systems, a relay driver is used for energizing a Loss of Channel AL telephone relay. the NOISE outputs work into OR logic on this board.

Location of components for this board is shown in Fig. 26. Two internal schematics are used; Fig. 27 for electromechanical systems and Fig. 28 for solid state systems.

Transmitter Key Board

The Transmitter Key board located in slot J contains OR logic to combine all inputs required to key the transmitter, and interface circuitry to key the particular channel equipment. A relay driver circuit is connected to the output of the OR in order to operate an AR relay mounted in the rear of the chassis.

For use with the TCP channel, interface with the transmitter is a positive going (0 to 20 volt) buffered output represented by transistors Q4 and Q5 is shown on the internal schematic, Fig. 32. When the relay is used with tone channels, the transmitter interface is a negative going output similar to the relay driver and is shown by transistor Q6 on internal schematic, Fig. 33.

Location of components for the XMTR KEY board is shown in Fig. 31.

Checkback Board

The Checkback board located in slot K contains logic used to functionally test the channel in both directions. The circuit consists of two AND circuits and a 2500/2500 millisecond time delay and is operated from the CHANNEL SUPV board. This logic is required as part of the channel checkback scheme.

The location of components for this board is shown in Fig. 34, and the internal schematic in Fig. 35.

Timing Board

The timing board located in slot L contains logic, a buffered input, and three time delays used in conjunction with the remainder of the relay.

After a pilot trip operation, the 0/30 millisecond timer maintains the transmitter keying for 30 milliseconds. The 180/0 millisecond timer delays keying of the transmitter for 180 milliseconds after opening of the local breaker. Input to this timer is a 48/125 V DC buffer circuit.

The 2500/0 millisecond timer and associated logic is used to permit transient blocking for 2.5 seconds if a trip output is obtained from the channel receiver. This circuit is also controlled by the 52b contact input.

The location of components on this board is shown in Fig. 36, and the internal schematic in Fig. 37.

Arming Board

The Arming Board located in slot M contains the connecting logic between the Channel, Protective Relay, Elec-Mech and Timing boards for the OUTPUT board. Logic on this board interfaces with and sets up arming of the trip AND, the transient blocking and unblocking timers and the 4/0 millisecond trip timer.

In addition, two time delays, 0/1000 and 0/100 milliseconds, are included on this board. The 0/1000 MStimer holds transient blocking on for an additional 1000 MS to protect against fault power reversals due to unequal breaker reclosing times into a permanent external fault. After a pilot trip operation, the 0/100 MS timer picks up and immediately resets the 0/1000 MS timer to de-energize the transient blocking timer. The 100 MS dropout time is greater than the time it takes to reset the distance relays, remove the input to the 0/1000 MS timer, therefore transient blocking will remain off, after the pilot trip signal is removed.

The location of components for this board is shown in Fig. 38 and the internal schematic in Fig. 39.

Output Board

The Output board located in slot N contains the final logic of the relay. This board utilizes the intelligence supplied by the Arming board to set up either a pilot trip output for internal faults, transient blocking on external faults or transient unblocking for sequential faults.

Three timers are used on this board: a 4/0 millisecond timer to delay the pilot trip output and two 18/0 millisecond timers for transient blocking and unblocking. NOTE: Relays may be supplied with the transient blocking time calibrated for 25 milliseconds instead of 18 MS to coordinate with the time delay of the channel equipment. The pilot trip output is comprised of and AND circuit whose output works into a logic inverting amplifier. There are two final pilot trip output: a buffered positive going (0 to 20 volt) output and a relay driver to activate an AR relay mounted in the rear of the chassis. Fig. 40 shows location of components on this board, and Fig. 41 shows the internal schematic and detailed logic.

Test Board

The Test board located in slot 0 is used for facilitating test measurements and routine checks of the relay. This board consists of 10 test terminals mounted on a panel attached to a printed circuit board.

OPERATION

The type STU-12 transfer trip relay for a weak feed terminal is used in a directional comparison permissive overreaching transfer trip relay system for power line protection. High speed tripping is obtained for two or three terminal line application where line terminals may be weak or strong, providing one of the terminals is a strong source.

System Operation

In a directional comparison transfer trip system, a continuous guard signal is normally transmitted from each line terminal and received at all other terminals. The channel transmitters are keyed to the trip frequency by the STU-12 to remove blocking at the remote terminals during an internal fault. At the weak feed terminal, the STU-12 operates on the "echo-trip" principle; that is, a trip request must be received from one of the remote terminals before the local transmitter can key a trip signal back to the remote terminal. In addition to receiving a remote trip request at the weak source terminal, either voltage relay (27 or 59N) and neither reverse-reaching relay must operate to key the local transmitter. Pilot tripping is initiated at the weak terminal if either voltage relay operates and neither reverse reaching phase or ground relay operates and a trip request is received from all remote terminals.

If a weak source terminal can be become a strong source then forward reaching phase and ground relays can be applied to the system as in the transfer trip normal system.

Some features included in the system are a functional test channel checkback scheme, loss of A-C potential circuit for reverse reaching relays, channel logic to force a guard return, and coordination for bus fault tripping, breaker failure and fault power reversal. The description of the preceding features and some special weak feed coordination is further explained under the Relay Operation section.

Refer to system I.L. 40-205.1 on the transfer trip system for further system operation.

Relay Operation

Refer to the logic diagrams shown in Fig. 4, 5, 6, and 7 to understand the operation of the STU-12 transfer trip relay.

1. Normal Condition

   In Fig. 4,5,6, and 7 the logic voltage "0" and "1" states shown refer to the normal operating condition of the STU-12 relay.

2. Internal Fault

   For an internal fault, providing the terminal is weak feed, one of the voltage relays (27 or 59N) Will operate and cause the input that is not negated on the 4 input AND on WEAK FEED LOGIC-3 board to become a logic "1". This will satisfy this AND and course a logic "1" output from the line driver which does the following:

   a. Produce a logic "1" at Test Term 3 (Protective Relay.)

   b. Pickup the 0/1000 MS timer on the ARMING BD. and produce a logic "0" at terminal 5 of the OUTPUT BD. This will start the transient blocking timer.

   c. Arm the trip AND on the OUTPUT BD through the one input OR on the ARMING BD.

   d. Satisfy one input of the trip AND on the ARMING BD.

   Both of the channel transmitters will be keyed at the remote terminals, thus causing both of the receiver trip outputs of the local channel 1 and 2 receivers to become a logic "1". This make TEST TERM 4 (CHANNEL TRIP) a logic "1" signal through logic on the CHANNEL INTERFACE and CHANNEL TRIP BDS. This "1" output will satisfy the trip AND on the ARMING BD. causing energization of the 4/0 MS timer on the OUTPUT BD. Four milliseconds later the trip AND on the OUTPUT BD. will be satisfied and produce a PILOT TRIP.

In addition, a voltage relay operation will cause drop out the 0/6 MS timer on the WEAK FEED LOGIC 4 board and satisfy one of the inputs on the three input AND on the board. Since a trip request will be received from the remote terminal (s); that is, then the receiver trip outputs become a logic "1"; to satisfy the three input AND to key the local transmitter.

Also, when a receiver trip output (logic "1") is received as an input to the STU-12 the 2500/0 MS timer on the TIMING BD. will be energized to start transient blocking. This will not affect the initial pilot trip, since it is an internal fault, and once the local breaker opens, then the 52b contact will block the output of this AND on the TIMING BD.

The 52b contact of the breaker provides an input to the 0/50 timer on the WEAK FEED LOGIC-3 board. The output of this timer blocks tripping when the breaker is open. Tripping will remain blocked 50 milliseconds after closing the breaker at the Weak Feed terminal to allow time for the undervoltage relay (27) to reset

If the STU-12 is applied at a terminal that can be a strong feed terminal, then distance relays 21P or 21NP (67N) would respond to the internal fault.

Operation of either of these relays would cause the STU-12 to key the transmitter to the trip frequency and also to set up trip. Logic for strong feed operation is on WEAK FEED LOGIC-1 board.

Once a pilot trip signal is obtained for an internal fault, the 0/100 MS timer on the ARMING BD. will rapidily reset the 1000 millisecond dropout timer of the 0/1000 MS timer. Therefore; when reclosing into a permanent internal fault, the only time delay will be the 4/0 MS timer.

3. External Fault

For an external fault forward from the weak source terminal but behind the remote terminals, one of the forward reaching relays of the remote terminal of a three terminal line will not see the fault. As a result, no receiver trip signal will be received from that remote terminal. At the local terminal, if either voltage relay (27 or 59N) operates, then, through logic on WEAK FEED LOGIC 3 board, the four input AND is satisfied to produce a logic "1" at TEST TERM 3 (Protective Relay). The trip AND on the ARMING BD will not be satisfied because both receiver trip signals were not received. However, the 0/1000 MS timer will pickup to cause the 18/0 MS transient blocking timer on the OUTPUT BD to start timing. IN 18 milliseconds, TEST TERM 2 (TRANSIENT BLOCKING) will become a negative logic "1" to block the trip AND of the OUTPUT BD. thereby preventing possible undersirable tripping during transients occuring at the clearing of an external fault.

If an external fault occurs behind the weak feed terminal of the protected line, then either the undervoltage (27) or overvoltage relay (59N) will operate. Also, either reverse reaching relay (21S or 21NS) will also see this fault and operate to block the 4 input AND on the WEAK FEED LOGIC 3 board. The forward reaching relays at the remote terminal (s) may also see this fault and key to the trip frequency. Therefore a trip request (received receiver trip signal) would be received at the weak feed terminal. This would satisfy one input of the trip AND on the ARMING BD. and also start the 2500/0 ms. timer on the TIMING BD. Since the other input to the trip AND is not satisfied, the output of the 2500/0 ms. timer will activate the 0/1000 ms. timer on the ARMING BD. and set up transient blocking 18 milliseconds latter to block trip. No tripping will occur at the remote terminals since operation of 21S or 21NS at weak feed terminal will prevent echo keying by pickingup the 4/80 ms. timer on WEAK FEED LOGIC 4 board.

The 0/6 MS timer on WEAK FEED LOGIC 4 board is used to delay echo keying for 6 milliseconds to allow adequate time for 21S or 21NS to operate for an external fault. The overcurrent fault detector (IA/IC) supervices 21S and must operate along with 21S to block keying and trip.

If the terminal was strong rather than weak feed, then for a forward external fault, the forward reaching relay 21P or 21NP (67N) would operate to set up transient blocking. For a reverse fault, these relays would not see the fault, but transient blocking would be set up with the received trip signals.

Transient blocking is also established to insure against any misoperation due to fault power reversals caused by unequal circuit breakers clearing time on a parallel line. The 1000 millisecond reset time of the 0/1000 MS timer on the ARMING BD. prevents misoperations when reclosing into an external fault where fault power flow reversals occur. In addition, the 1000 millisecond reset time also prevents transient, blocking from resetting when short holes appears in the input.

4. Sequential Fault

Occasionally an external fault will be followed by an internal fault before the former is cleared. In order to prevent a long delay in clearing a sequential fault a transient unblocking 18/0 MS timer is included. Although transient blocking has been initiated by the external fault, the presence of an internal fault will produce a negative logic "1" signal from the trip AND on the ARMING BD., since a trip request will be received from the remote terminal. This "1" signal will energize the 4/0 MS timer and satisfy the AND to energize the 18/0 MS transient unblocking timer on the OUTPUT BD. In 18 milliseconds the transient blocking timer will reset the transient blocking timer thus satisfying the TRIP AND on the OUTPUT BD. and causing a pilot trip output.

5. Loss of Potential

Distance relays may tend to operate if the input from the potential device is momentarily interrupted. Since tripping of circuit breakers is undesirable for this loss of ac potential the STU-12 relay will lockout tripping and provide alarm. This is accomplished by the 500/500 MS timer on WEAK FEED LOGIC-1 board. In 500 milliseconds after a reverse reaching relay (21NS-67NS or 21S) operation, providing both receiver trip signals are not present, a logic "1" signal will be produced at TEST TERM 7 (Loss of Potential). This "1" signal will lockout the three input AND on W.F. Logic 1 board, thereby simulating "not" distance relay (21P or 21NP-67N) operation. Output of the 500/500 MS timer will also provide a buffered "1" signal at the J1 connector.

For electromechanical systems, an AL telephone relay will drop out for indication purposes.

6. Channel Transmitter Control

The transmitter may be keyed to the trip frequency by any one of the following six inputs:

a. 0/30 MS timer after pilot trip.

b. 180/0 MS timer from 52b contact.

c. 21P or 21NP (67N) forward reaching relay operation — strong feed keying

d. 27 or 59N — voltage relay operation — weak feed keying.

e. Check back circuit from channel logic.

f. Contact bounce for 21P or 21NP (67N) operation — electromechanical systems only.

When the transmitter is keyed, TEST TERM 5 (XMTR KEY) becomes a logic "1" signal, the keying AR picks up, and the interface with the transmitter becomes a logic "1" as described under the operation of the XMTR KEYING BD.

The weak feed keying control logic is contained primarily on WEAK FEED LOGIC BDS. 2 and 4. Keying at the weak terminal will take place when either voltage relay (27N and 59N) and neither reverse reaching relay (21NS or 21S) operates and a trip request is received from either remote terminal. There is a 6 millisecond delay (0/6 MS timer) on echo keying to allow time for blocking to become effective for an external fault, thereby preventing false keying.

Operation of 21S and its supervising overcurrent fault detector IA/IC will satisfy the two input AND on WEAK FEED LOGIC 2 BD. If the undervoltage relay 27 has operated and the breaker is not open then an output will be obtained from the three input AND. This output will start the 10/0 MS timer and also satisfy the four input OR on WEAK FEED LOGIC 4 BD. to block echo keying. After 10 milliseconds, the output of the 10/0 timer will seal in the three input AND to provide continuous echo key block when 21S resets after memory action subsides for a zero voltage fault. This AND can only be reset by the undervoltage relay (27) or by the opening of the breaker. The purpose of the breaker resetting this is to break the 21S seal in for bus faults, where bus side pots are used.

If 21NS or 67NS operates, it also will block echo keying by applying an input to the four input OR on WEAK FEED LOGIC 4 board. Also, echo keying is blocked by the 2 input OR and AND memory circuit on the same board. This circuit will cause blocking when the breaker is open (52b closed) and the undervoltage relay (27) operates. The purpose of this is to prevent tripping of the remote terminals when closing the line into a fault on the weak-terminal bus, when using bus-side pots. Relay 21S could not operate for this case since their was no voltage prior to the fault.

To block echo keying, an output must be received from the four input OR an WEAK FEED LOGIC 4 board for 4 milliseconds to pickup the the 4/80 timer and block the echo keying three input AND. The 4 ms time delay will prevent blocking for transient 21S operation on an internal fault. There is an 80 millisecond delay on removal of blocking to insure that the fault detectors at the remote terminal have reset.

Strong feed keying control is obtained through logic on WEAK FEED LOGIC 1 board. Operation of 21P or 21NP (67N) will satisfy the three input AND on this board providing loss of potential has not occurred and echo keying is not blocked. A A logic "1" output from this AND will cause transmitter keying.

After a pilot trip operation the 0/30 MS timer on the TIMING BD. will maintain keying of the trip frequency for 30 milliseconds in order to insure that the remote breaker has tripped before the transmitter returns to normal condition.

After the local circuit breaker opens, the 52b contact will energize the 180/0 MS timer on the TIMING BD. and initiate trip frequency transmission after 180 milliseconds and until such time as the circuit breaker is reclosed. This 180 millisecond delay allows coordination for bus fault tripping of the local breaker, where tripping of the remote breaker would be incorrect and might cause undesired interruption to tapped transformer terminals. Transmission of the trip frequency is necessary to permit tripping of the remote terminal should the remote circuit breaker be closed into a fault, or should a fault develop in the protected line while while the local circuit breaker is open.

7. Channel Logic

   a. TCF frequency shift carrier channel
   Refer to CAHNNEL-INTERFACE, TRIP, and SUPERVISION BDS. in logic drawings Fig. 4 and 5.

Two TCF CHANNEL INTERFACE boards are shown: Both boards must be used for three terminal line systems utilizing two receivers. However, for two terminal line applications, the interface board in board slot G must not be used in the relay. An interlock shown on the Channel 2 interface board connects the Channel 2 trip output as one output to the Channel trip AND on the CHANNEL TRIP BD.

For three terminal line applications, both receiver trips signals are required to produce a logic "1" signal at TEST TERMINAL 4. This output will satisfy one input of the ARMING BD. trip AND, block operation of the 500/500 MS loss of potential timer, and produce a buffered "1" output. Either receiver trip signal will produce a "1" signal at terminal 12 of the CHANNEL TRIP BD. to start transient blocking.

For two terminal line applications, the one receiver trip signal will produce a "1" output at TEST TERMINAL 4 (CHANNEL TRIP), and terminal 12 of the CHANNEL TRIP BD.

Operation of either or both low signal clamp inputs ("1" to "0") will cause a "1" signal at TEST TERMINAL 6 (LOSS OF CHANNEL) for use in the channel checkback scheme. For electromechanical systems, an AL telephone relay will dropout for indication of loss of channel. In addition, operation of either Check Trip output will produce a "1" output at terminal 7 of the CHANNEL SUPERVISION BD. This signal is used for the channel checkback scheme.

   b. Frequency shift tone channel
   Refer to CHANNEL INTERFACE, TRIP and SUPERVISION BDS. in logic drawings Fig. 6 and 7.

Two TONE CHANNEL INTERFACE boards are shown; Both boards must be used for three terminal line systems utilizing two receivers. However, for two terminal line applications, the interface board in board slot G must not be used in the relay. An interlock shown on the channel 2 interface board connects the channel 2 trip output as one input to three input channel trip AND on the CHANNEL TRIP BD.

For three terminal line applications, both receiver trip signals and no low signal clamps are required to produce a logic "1" signal at TEST TERMINAL 4 (CHANNEL TRIP). This output will satisfy one input of the ARMING BD. trip AND, block operation of the 500/500 MS loss of potential timer, and produce a buffered output. Either receiver trip signal will produce a "1" signal at terminal 12 of the CHANNEL TRIP BD. to start transient blocking and to energize an AND circuit on the CHANNEL SUPERVISION BD.

For two terminal line applications, the one receiver trip signal will produce a "1" output at TEST TERMINAL 4, and terminal 12 of the CHANNEL TRIP BD.

When a Tone Channel is used with the STU-12 transfer trip relay, the Tone receiver must be internally strapped to clamp to no trip output when a low signal condition occurs. Therefore, tripping will not be allowed under loss of channel.

Either LOW signal clamp operation ("1" to "0") will pickup the 150/100 MS timer and produce a "1" signal at TEST TERMINAL 6 (LOSS OF CHANNEL) for use in channel checkback as well as blocking Channel Trip. For electromechanical systems, an AL telephone relay will dropout for indication of loss of channel. Both low signal clamp outputs on the CHANNEL INTERFACE BDS. are buffered and separately brought out to the J1 connector.

One AND circuit on the CHANNEL SUPERVISION BD. is used for channel checkback. When a receiver trip signal from either channel is received, a logic "1" will be produced at terminal 3 of the CHANNEL SUPERVISION BD. providing both low signal clamps have not operated.

When the noise output operates on either one or both channel receivers, a logic "1" output is produced from the noise OR on the CHANNEL SUPERVISION BD. to block the trip AND of the ARMING BD. Therefore, the STU-12 relay will not trip on receipt of the channel noise. Both noise outputs on the CHANNEL INTERFACE BD. are buffered, connected together, and brought out to the J1 connector.

A guard return circuit is included on the CHANNEL TRIP BD. and is comprised of two AND's and an OR. The principle of guard return, is to insure that after a loss of channel condition is cleared up, the receiver trip signal will return in the "0" logic state, not "1". When a low signal clamp operation ("1" to "0") is received from the tone channel, then the 150/100 MS timer picks up and applies a "1" signal to one input of each of the two guard AND's on the CHANNEL TRIP BD. Now, if either or both receiver trip signals are "1" or become a "1" within the 100 millisecond dropout time of the 150/100 MS timer, then a "1" output will be produced at the output of the guard return AND and the OR it works into. Terminal 5 of the CHANNEL TRIP BD. will become a "1" and hold the 150/100 MS timer picked up by applying a "1" input to the 3 input loss of channel OR on the CHANNEL SUPERVISION BD. By inspecting the logic it can be seen that both receiver trip signals (one for two terminal applications) must return to guard, logic "0" to, make the channel operative after a loss of channel condition.

8. Channel Checkback Test

A. TCF frequency shift carrier channel
Refer to logic drawings, Fig. 4 and 5. Information in this section does not cover the the complete test, but only that portion concerning the STU-12 relays.

At the local terminal, the carrier transmitter will be disconnected from the line thus causing a loss of channel condition at the remote terminal. This will cause the loss of channel OR on the CHANNEL SUPERVISION BD. (Remote Terminal) to assume a "1", and satisfy the two input AND (preceding the 2500/2500 MS timer) and in 2500 milliseconds pickup the 2500/2500 MS timer on the CHECKBACK BD. The "1" output of the 2500/2500 MS timer will satisfy one input of the AND following it. Next, a test switch will be operated at the local terminal and the following will happen: a protective relay signal (for example, 21P) will be simulated, the transmitter will be reconnected to the line to restore the channel, and the local transmitter will be keyed to the trip frequency. At the remote terminal the TCF receiver logic will not give a trip output since the channel was not restored to the guard frequency. However, there will be a "1" signal obtained from the CHECK TRIP output of the receiver. This check trip output will satisfy the other input to the AND on the CHECKBACK BD. causing the transmitter to be keyed to the trip frequency. Since the check trip signal also applies a "1" input to the negated input of the AND energizing the 2500/2500 MS timer, it will no longer be satisfied and the timer will dropout causing keying to stop in 2.5 seconds. However, within the 2.5 seconds of keying, the STU-12 relay at the local terminal will trip because of reception of both a received trip signal and a simulated protective relay signal.

b. Frequency shift tone channel
Refer to logic drawings, Fig. 6 and 7
Information in this section does not cover the complete test, but only that portion concerning the STU-12 relay.

At the local terminal, the tone transmitter will be disconnected from the line thus causing a loss of channel condition at the remote terminal. This will cause the loss of channel OR on the CHANNEL SUPERVISION BD. (remote terminal) to assure a "1" output to pickup the 150/100 MS timer. This satisfies the two input AND on the Check Back Bd. and in 2500 milliseconds the 2500/2500 MS timer will pick up. The "1" output of the 2500/2500 MS timer will satisfy one input of the AND following it. Next, a test switch will be operated at the local terminal and the following will happen: a protective relay signal (for example, 21P) will be simulated, the transmitter will be reconnected to the line to restore the channel, and the local transmitter will be keyed to trip frequency. At the remote terminal, the tone receiver trip signal will be a "1" thus causing the three input AND on the CHANNEL SUPERVISION BD. to operate and produce a "1" at terminal 3 of this board. This "1" will satisfy the other input to the AND on the CHECKBACK BD. causing the transmitter to be keyed to the trip frequency. Since at the same time, the input to the 2500/2500 MS timer is lost, then the keying signal to local terminal will only last 2.5 seconds. However, within this time of keying, the STU-12 relay will trip because of the reception of both a received trip signal and a simulated protective relay signal.

9. Electromechanical Systems

When the STU-12 relay is used with electromechanical protective relays, two contact bounce circuits are used. The contact bounce circuit will produce a logic "1" output immediately upon reception of an input logic "1" signal. This output will last for approximately 20 milliseconds. The contact bounce circuits on the W.F. Logic 1 and 3 boards permit transmitter keying and an input to set up tripping respectively. These circuits prevent additional delay in tripping due to a bouncing elecmech protective relay contact.

Two telephone alarm relays are mounted in the rear of the chassis — one for indication of loss of a-c potential, another for indication of loss of channel. Both of these AL's are normally picked up.

CHARACTERISTICS

Control Voltage: 48 V DC (42 to 56 volts)
125 V DC (105 to 140 volts)

Current Drain:
SOLID STATE SYSTEMS
Normal — 160 MA
Pilot Trip - 270 MA
Maximum - 310 MA

ELEC-MECH SYSTEMS
Normal - 200 MA
Pilot Trip - 310 MA
Maximum - 350 MA

Temperature Range: -20 C to +55 C around chassis

Inputs:
52b Contact - 48/125 Control Voltage Buffered
48V - 1.5 MA MAX CURRENT
125V - 2.5 MA MAX CURRENT

Protective Relays:
21NS(67NS), 21S, 21NP(67N), 21P, 59N, 27, IA/IC
SOLID STATE SYSTEMS
15 to 20 V DC Buffered
2 MA MAC CURRENT
ELEC-MECH SYSTEMS
48/125 Control Voltage Buffered
48 V - 1.5 MA MAX CURRENT
125 V - 2.5 MA MAX CURRENT

All Other Inputs are: 15 to 20 V DC, buffered and require 2 MA MAX CURRENT

Outputs:

Transmitter Key:

TCF Frequency Shift Carrier Channel: 15 to 20 V DC Buffered
10 MA MAX CURRENT

Frequency Shift Tone: "0" State - Open Circuit
"1" State - Short Circuit to Battery Neg.
140 V DC MAX Voltage
40 MA MAX CURRENT

All Other Outputs are 15 to 20 V DC Buffered and provide 10 MA MAX CURRENT.

Time:

Trip Time (4/0): 4.0 to 4.5 Milliseconds (adjustable from 2.0 to 6.0 MS)

Transient Block and Transient Unblock Time (18/0): 17 to 20 milliseconds (adjustable from 12 to 30 MS) (Relays may be ordered with a transient blocking time of 24 to 27 milliseconds)

Low Signal Lock-out Time: 130 to 180 Milliseconds

Loss of Potential Time (500/500): 400 to 600 Milliseconds

Dimensions: relay height-5.25"(3 rack units)
relay width - 19"
relay depth - 14"

Weight: approximately 15 lbs.

SETTINGS

No setting is required on the STU-12 relay.

INSTALLATION

The STU-12 relay is generally supplied in a cabinet or on a relay rack as part of a complete system. The location must be free from dust, excessive humidity, vibration, corrosive fumes or heat. The maximum temperature around the chassis must not exceed 55 C.

The outline and drilling plan of the STU-12 relay is shown in Fig. 43.

ADJUSTMENTS & MAINTENANCE

Acceptance Check

It is recommended that an acceptance check be applied to the STU-12 relay to verify that the circuits are functioning properly. The following procedure can be used for this purpose.

Connect the STU-12 relay to the test circuit of Fig. 42. Apply rated dc to J1 terminals 3 and 4 as shown, and use an auxiliary 20 volt regulator or the internal 20 volts of the STU-12 relay for the inputs to the switches. On STU-12 relays for use with the electro-mechanical protective relays, rated positive dc must be applied to the protective relay switches.

Note that the low signal switches for channel 1 and 2 are normally closed and all other switches are open.

Since the STU-12 relay varies in logic depending on the channel equipment, insure that it is checked per the proper channel. When reference is made to AL relay, this refers to STU-12 relays for use only with electro-mechanical systems utilizing elec-mech protective relays.

When reference is made to TEST TERMINAL, this means one of the 10 test terminals on the TEST BD. in board slot O. All voltages are to be measured with respect to negative, TEST TERMINAL 10. Voltage measurements may vary by +10%. Information in this acceptance test applies to a relay with a transient blocking time of 18 MS. For relays with a transient blocking time of 25 MS., limits are 24 to 27 milliseconds.

A. Normal Condition

TEST	TERMINAL	1:	0 Volts
,,	,,	2:	20 Volts
,,	,,	3:	0 Volts
,,	,,	4:	0 Volts
,,	,,	5:	0 Volts
,,	,,	6:	0 Volts
,,	,,	7:	0 Volts
,,	,,	8:	20 Volts
,,	,,	9:	20 Volts

Keying AR — Not picked up
Trip AR — Not picked up
Loss of Channel AL — Picked up (Elec-Mech System)
Loss of Potential AL—Picked up (Elec-Mech System)

B. Channel Logic - 2 Term Line Relay Only (For 3 Term Line relays, disregard this section and continue on section C)

1. TCF Carrier Channel

a. Channel Trip-2500/0 MS timer (TIMING BD.), 0/1000 MS timer

Close Trip-1 switch

Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds, then rise from 0 to 20 volts in 3100 to 4100 milliseconds.

Test Term 4: Voltage rise from 0 to 20 volts

Open Trip - 1 switch

b. Loss of Channel

Open LOW SIGNAL - 1 switch

Test Term 6: Voltage rise from 0 to 20 volts

Loss of Channel AL will drop out

Close LOW SIGNAL - 1 switch

2. Tone Channel

a. Channel Trip - 2500/0 MS timer (TIMING BD.) 0/1000 MS timer (ARMING BD.), transient blocking timer

Close Trip-1 switch

Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds, then rise from 0 to 20 volts in 3100 to 4100 milliseconds.

Test Term 4: Voltage rise from 0 to 20 volts

Open Trip-1 switch

b. Loss of channel-150/100 MS timer (CHANNEL SUPERVISION BD.)

Open LOW SIGNAL-1 switch

Test Term 6: Voltage rise from 0 to 20 volts in 130 to 180 milliseconds

Loss of Channel AL will drop out

Close LOW SIGNAL - 1 switch

Test Term 6: Voltage drop from 20 to 0 volts in 75 to 125 milliseconds.

c. Guard Return

Open LOW SIGNAL-1 switch, then close Trip-1 switch

Test Term 4: Voltage must remain at zero

Close LOW SIGNAL - 1 switch

Test Term 6: Voltage must remain at 20 zero

Open Trip-1 switch

Test Term 6: Voltage must drop from 20 to 0 volts

C. Channel Logic - 3 Term Line Relays Only (For 2 Term Line relays, the preceding section was used and this part may be disregarded)

1. TCF Carrier Channel

a. Channel 1 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer

Close Trip - 1 switch

Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds

Test Term 4: Voltage remains at zero

Open Trip-1 switch

b. Channel 2 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD,), transient blocking timer

Close Trip - 2 switch

Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds

Test Term 4: Voltage must remain at zero

Open Trip - 2 switch

c. Channel 1 and 2 Loss of Channel

Open LOW SIGNAL - 1 switch

Test Term 6: Voltage rise from 0 to 20 volts

Loss of Channel AL must drop out

Close LOW SIGNAL - 1 switch, then open LOW SIGNAL - 2 switch

Test Term 6: Voltage rise from 0 to 20 volts

Loss of Channel AL must drop out

Close LOW SIGNAL - 2 switch

d. Channel 1 and 2 switches

Test Term 4: Voltage rise from 0 to 20 volts

Open Trip-1 and Trip-2 switches

2. Tone Channel

a. Channel 1 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer

Close Trip - 1 switch

Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds

Test Term 4: Voltage remains at zero

Open Trip - 1 switch

b. Channel 2 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.) transient blocking timer

Close trip - 2 switch

Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds

Test Term 4: Voltage remains at zero

Open Trip - 2 switch

c. Guard Return - Channel 1 - Trip and Low Signal - 150/100 MS timer

Open LOW SIGNAL - 1 switch

Test Term 6: Voltage rise from 0 to 20 volts in 130 to 180 milliseconds

Loss of Channel AL must drop out

Close Trip - 1 switch, then close LOW SIGNAL - 1 switch

Test Term 6: Voltage must remain at 20 volts

Open Trip -1 switch

Test Term 6: Voltage must drop from 20 to 0 volts in 75 to 125 milliseconds

d. Guard Return - Channel 2 - Trip and Low Signal - 150/100 MS timer

Open LOW SIGNAL -2 switch

Test Term 6: Voltage rise from 0 to 20 volts in 130 to 180 milliseconds

Loss of Channel AL must drop out

Close Trip - 1 switch, then close LOW SIGNAL - 1 switch

Test Term 6: Voltage must remain at 20 volts

Open Trip - 1 switch

Test Term 6: Voltage must drop from 20 to 0 volts in 75 to 125 milliseconds

e. Channel 1 and 2 - Trip and Low Signal

Close Trip-1 and Trip-2 switches

Test Term 4: Voltage rise from 0 to 20 volts

Open LOW SIGNAL-1 switch

Test Term 4: Voltage drop from 20 to 0 volts

Open Trip-1 and Trip-2 switches, then close LOW SIGNAL-1 switch

D. Weak Feed Logic Operation

1. Weak Feed Trip

a. Voltage relay operation

Close 27 switch

Test Term 3: Voltage rise from 0 to 20 volts

Open 27 switch, then repeat above using 59N switch

b. Block of weak feed trip (W.F.Logic 3 BD.) 21NS, 21S and IA/IC, and 52b (0/50 timer)

Close 59N switch

Close 21NS switch

Test Term 3: Voltage drop from 20 to 0 volts

Open 21NS switch

Close 21S and IA/IC switches

Test Term 3: Voltage drop from 20 to 0 volts

Open 21S and IA/IC switches

Close 52b switch

Test Term 3: Voltage drop from 20 to 0 volts

Open 52b switch

Test Term 3: Voltage rise from 0 to 20 volts in 38 to 62 milliseconds (0/50 timer)

Open 59N switch

2. Weak Feed Keying (For 2 Term line relays, remove the output BD. (Slot N) for these tests to prevent a Pilot Trip operation)

a. Voltage Relay operation

Close 27 Switch

Test Term 5: Voltage remains at zero

Close Trip-1 switch

Test Term 5: Voltage rise from 0 to 20 volts

Open 27 switch, then close 59N switch

Test Term 5: Voltage rise from 0 to 20 volts in 6 to 10 milliseconds (0/6 timer)

Open 59N and Trip-1 switch

b. Block of weak feed keying (W.F.Logic 2 & 4 BDS.) 21NS. 21S and IA/IC, 52b, 10/0 timer, 4/80 timer, 0/6 timer

Close Trip-1 switch

Close 59N switch

Test Term 5: Voltage rise from 0 to 20 volts

Close 21NS switch

Test Term 5: Voltage drop from 20 to 0 volts in 2.4 to 4.0 milliseconds (4/80 timer)

Open 21S switch

Test Term 5: Voltage rise, from 0 to 20 volts in 60 to 100 milliseconds (4/80 timer)

Open 59N switch, then close 27 switch

Close 21D switch, then IA/IC switch

Terminal 3 (W.F. Logic 2 BD.): Voltage rise from 0 to approx. 7 volts in 6 to 10 milliseconds (10/0 timer)

Test Term 5: Voltage drop from 20 to 0 volts

Open 21S and IA/IC switches

Test Term 5: Voltage must remain at zero.

Close 52b switch

Terminal 3 (W.F. Logic 2 BD.): Voltage must drop from 7 to 0 volts

Test Term 5: Voltage will rise from 0 to 20 volts

Open 52b switch

Test Term 5: Voltage must drop from 20 to 0 volts

Open 27 switch

(Re insert OUTPUT BD. into Slot N)

E. Strong Feed Operation

1. 21P or 21NP (67N) Keying and trip

Close 21P switch

Test Term 3 & 5: Voltage rise from 0 to 20 volts

Open 21P switch and repeat above fro 21NP switch

2. Loss of potential (500/500 timer - W.F. Logic 1 BD.)

Close 21S switch

Test Term 7: Voltage rise from 0 to 20 volts in 400 to 600 milliseconds (500/500 timer)

Repeat above for 21NS switch

3. Block of Loss of Potential

Close Trip-1 and Trip-2 switches (Trip-2 switch not required for 2 Term Line relays)

Then close either 21S or 21NS switch

Test Term 7: Voltage must remain at zero

Open 21S (or 21NS,) Trip-1 and Trip-2 switches

4. Block of 21P (21NP) Keying and Trip

Close 21P switch

Then close 21S switch

Test Term 3: Voltage must drop from 20 to 0 volts in 0.5 sec.

Close 52b switch and 27 switch

Open 21S switch

Test Term 3: Voltage must remain at zero

Open 27 switch

Test Term 3: Voltage must rise from 0 to 20 volts

Open 52b and 21P switches

F. 52b Contact Operation - 180/0 MS timer (TIMING BD.)

Close 52b switch

Test Term 5: Voltage must rise from 0 to 20 volts in 180 to 230 milliseconds

Open 52b switch

G. Channel Checkback Operation

1. TCF Carrier Channel 2500/2500 MS timer (CHECKBACK BD.), check trip inputs

Open LOW SIGNAL - 1 switch

TP4 on CHECKBACK BD. voltage must drop from 8 to 0 volts in 2000 to 3000 milliseconds

Close CK-Trip-1 switch

Test Term 5: Voltage must rise from 0 to 20 volts immediately then drop from 20 to 0 volts in 2000 to 3000 milliseconds

XMTR KEY AR must pickup for 2 to 3 seconds

Close LOW SIGNAL-1 switch, then open CK Trip-1 switch

For relay used for 3 Term Line, also do the following:

Open LOW SIGNAL-2 switch and wait for 3 seconds, then close CK Trip-2 switch

Test Term 5: Voltage must rise from 0 to 20 immediately then drop from 20 to 0 volts in 2 to 3 seconds.

Close LOW SIGNAL-2 switch, then open CK Trip-2 switch

2. Tone Channel 2500/2500 MS timer (CHECKBACK BD.)

Open LOW SIGNAL-1 switch

TP4 on CHECKBACK BD.: Voltage must drop from 8 to 0 volts in 2000 to 3000 milliseconds

Close Trip-1 switch, then close LOW SIGNAL -1 switch

Test Term 5: Voltage must rise from 0 to 20 volts immediately then drop from 20 to 0 volts in 2000 to 3000 milliseconds

XMTR KEY AR must pick up for 2 to 3 seconds

Open Trip-1 switch

For relays used for 3 Term Line, also do the following:

Open both LOW SIGNAL-1 and LOW SIGNAL-2 switches then close Trip-2 switch. Wait for 3 seconds then close both LOW SIGNAL-1 and 2 switches

Test Term 5: Voltage must rise from 0 to 20 volts immediately after closing both the LOW SIGNAL switches then drop from 20 to 0 volts in 2 to 3 seconds

Open Trip-2 switch

H. Pilot Trip - 4/0 MS Timer (OUTPUT BD.)

Close 52b switch in order to prevent the 2500/0 MS timer from starting transient blocking

Close Trip-1 switch, and also, for 3 Term Line relays, close Trip-2 switch

Then, close 21P Switch

Test Term 1: Voltage must rise from 0 to 20 volts in 4.0 to 4.5 milliseconds

Trip AR must pickup

Open Trip-1 and Trip-2 switches

Test Term 1: Voltage must remain at 20 volts

Open 21P switch and Trip AR must drop out

Open 52b switch

I. Pilot Trip After Transient Unblocking 18/0 MS Timer (OUTPUT BD.)

Close 21P switch

Then, close Trip-1 switch, and also for 3 Term Line relays, close Trip-2 switch

Test Term 1: Voltage drop from 20 to 0 volts 18 to 20 milliseconds

Open 21P switch

Test Term 1: Voltage drop from 20 to 0 volts.

Open Trip-1 and Trip-2 switches

Repeat above tests except use switch 27 or 59N in place of 21P switch

J. Continue Key after pilot trip - 0/30 MS Timer

Close 21P switch

Close Trip-1 switch and for 3 Term Line relays, also close Trip-2 switch

As soon as the voltage on Test Term 1 rises from 0 to 20 volts then the 0/30 MS timer will pickup

Then open 21P switch

Test Term 5: Voltage must drop from 20 to 0 volts in 24 to 30 milliseconds

Open Trip-1 and Trip-2 switches

K. Fast Reset of 0/1000 MS timer after pilot trip .0/100 MS timer (ARMING BD.)

For checking this 0/1000 MS timer, it will be necessary to use a jumper

Close 21P switch, then close Trip-1 switch and also for 3 Term Line relays close Trip-2 switch

Terminal 4 (ARMING BD.): Voltage must rise from 0 to 16 volts in less than 2 milliseconds after the voltage at Test Term 1 rises from 0 to 20 volts

In order to check the 100 millisecond reset time, it is necessary to connect a jumper from TP-8 to terminal 14 on the ARMING BD.

Open 21P switch

Terminal 4 (ARMING BD.): Voltage must drop from 16 to 0 volts in 70 to 170 milliseconds

Open Trip-1 and Trip-2 switches, and remove the jumper

L. Contact Bounce Circuits (Weak Feed (W.F.) Logic 1 and 3 BDS.)

This section is to be used only for those STU-12 relays which are for use with electromechanical protective relays

Close 21P switch

Terminal 2 (W.F. Logic 1 and 3 Bds.): Voltage must rise from 0 to 20 volts immediatly then drop back to zero in approximately 20 milliseconds

Open 21P switch

M. Noise Operation (tones only)

This section is to be used only for those STU-12 relays which are for use with a frequency shift tone channel.

Close NOISE-1 switch

Then close 21P switch and Trip-1 switch, and also for 3 Term Line relays close Trip-2 switch

Test Term 1: Voltage must remain at zero

Open Noise-1 switch

Test Term 1: Voltage must rise from 0 to 20 volts

Trip AR must pickup

Open 21P, Trip-1 and Trip-2 switches

For 3 Term Line relays, repeat above test using Noise-2 switch instead by Noise-1 switch.

Recommended Routine Maintenance

Periodic checks of the relaying system are desirable to indicate impeding failure so that the equipment can be taken out of service for correction. Any accumulated dust should be removed at regular maintenance intervals.

All contacts should be periodically cleaned. A contact burnisher, Style No. 182A836H01, is recommended. The use of abrassive material is not recommended because of the danger of embedding small particles in the face of the soft silver and thus imparing the contact.

CALIBRATION

The proper adjustments to insure correct operation of the relay have been made at the factory and should not be disturbed after receipt by the customer. However, if the adjustments or if the components or printed circuit boards which affect calibration have have changed, then the STU-12 relay should be rechecked per the acceptance check information.

All time delays are fixed except for the three timers on the OUTPUT BD.: 18/0 (25/0) MS transient blocking timer. These adjustable timers can be recalibrated as follows using an auxiliary timer or oscilloscope.

Transient Block 18/0 MS Timer – OUTPUT BD.

(NOTE: For relays having a transient blocking timer of 25/0 MS limits are 24 to 27 milliseconds.

Start timer on 21P switch (positive pulse)
End timer on Test Term 2 (negative pulse)

Close 21P switch and the voltage on Test Term 2 must drop from 20 to 0 volts in 18 to 20 milliseconds (24 to 27 MS)

This time can be adjusted by turning potentiometer R14 on the OUTPUT clockwise for more time or counter clockwise for less time. (After recalibrating this timer also recheck the calibration of the 4/0 MS timer.)

Pilot Trip 4/0 MS Timer – OUTPUT BD.

Start Timer on 21P switch (positive pulse)
End timer on Test Term 1 (positive pulse)

For this calibration, close 52b switch

Close Trip-1 switch, and also Trip-2 switch for 3 Term Line relays

Then close 21P switch and the voltage on Test Term 1 must rise from 0 to 20 volts in 4.0 to 4.5 milliseconds

This timer can be adjusted by turning potentiometer R20 on the OUTPUT BD.clockwise for more time and counter-clockwise for less time.

(After recalibrating this timer, also recheck calibration of the 18/0 MS transient block timer.)

Transient Unblocking 18/0 MS Timer-OUTPUT BD.

Start timer on Trip-1 switch (positive pulse)

End timer on Test Term 1 (positive pulse)

Close 21P switch, and also close Trip-2 switch for 3 Term Line relays.

Then close Trip-1 switch and the voltage on Test Term 1 must rise from 0 to 20 volts in 18 to 20 milliseconds.

This time can be adjusted by turning potentiometer R1 on the OUTPUT BD. clockwise for more time and counter-clockwise for less time.

Tripping Relay (AR)

The type AR tripping relay unit has been properly adjusted at the factory to insure correct operation and should not be disturbed after receipt by the customer. If, however, the adjustments are disturbed in error, or it becomes necessary to replace some part in the field, use the following adjustment procedure. This procedure should not be used until it is apparent that the AR unit is not in proper working order, and then only if suitable tools are available for checking the adjustments.

a. Adjust the set screw at the top of the frame to obtain a 0.009 inch gap at the rear end of the armature air gap.

b. Adjust each contact spring to obtain 4 grams pressure at the very end of the spring. This pressure is measured when the spring moves away from the edge of the slot in the insulated crosspiece.

c. Adjust each stationary contact screw to obtain a contact gap of 0.020 inch. This will give 15-30 grams contact pressure.

Trouble Shooting

The components of the STU-12 relay are operated well within their ratings and normally will give long and trouble-free service. However, if a relay has given an indication of trouble in service or during routine check, then using "0" and "1" logic notation, the faulty printed circuit board can be traced to using the diagrams in Fig. 4, 5, 6, or 7. In turn, the faculty, component or circuit can be found using the individual schematic of the printed circuit boards which show the detailed transistor NOR/NAND logic-

Each NOR/NAND logic block represents a transistor on the schematic. The output of each individual logic block is the collector of the transistor which represents that block. The collector of each transistor is either connected to a test point or printed circuit terminal. A box around the transistor indicates that it is conducting for the normal condition of the relay.

Following is an explanation of the voltage levels for the "0" and "1" logic notation as shown for the normal relay condition in Figs. 4, 5, 6, and 7. This logic notation will also apply to the detailed logic on the printed circuit board internal schematics.

For positive logic – represented by logic blocks, with no arrows. "0" is equivalent to less than 0.5 volts with respect to negative, Test Term 10.

"1" is equivalent to 8 to 20 volts with respect to negative, Test Term 10)

For negative logic - represented by logic blocks with open arrow heads, "0" is equivalent to 8 to 20 volts with respect to negative, Test Term 10, except for the output of the relay driver, where a "0" is rated positive dc.

"1" is equivalent to less than 0.5 volts with respect to negative, Test·Term 10.

A board extender, Style No. 849A534G01, is available for facilitating circuit voltage measurements. After withdrawing anyone of the circuit boards, the extender is inserted into that slot. The board is then inserted into the terminal block on the front of the extender to restore all circuit connections.

The Test Terminals on the Test Bd. in the board position to the extreme right are helpful in checking the overall relay operation. Following are the voltages that will occur at these Test Terminals under various conditions:

NOTE: All voltages referred to are taken with respect to negative, Test Terminal 10.

Test Terminal 1: Pilot Trip

Normal Condition – 0 volts
Internal Fault – 20 volts

For an internal fault, either a forward reaching relay (21P or 21NP(67N)) or a voltage relay (27 or 59N) operation and both receiver trip signals (one receiver trip signal for 2 Term Line relays are required.

Test Terminal 2: Transient Blocking & Unblocking

Normal Condition – 20 volts
External Fault – 0 volts

The following will simulate an external fault:
21P or 21NP (67N) operation
27 or 59N operation
either channel receiver trip operation

Test Terminal 3: Protective Relay

Normal Operation – 0 volts
21P or 21NP(67N) Operation - 20 volts
27 or 59N Operation - 20 volts

Test Terminal 4: Channel Trip

Normal Condition - 0 volts

Operation of Channel 1 and 2 receiver trip outputs-(for 2 Term Line relays, only 1 channel required) - 20 volts

Test Terminal 5: XMTR Key

Normal Condition - 0 volts
21P or 21NP(67N) Operation - 20 volts
52b contact operation - 20 volts
Internal Fault (pilot trip signal) / 20 volts
27 or 59N and received trip signal 1 or 2 – 20 volts
Channel Checkback scheme–20 volts for 2.5 seconds

Test Terminal 6: Loss of Chennel

Normal Condition - 0 volts
Operation of either channel 1 or 2 Low signal clamp-20 volts.

Test Terminal 7: Loss of Potential

Normal Condition - 0 volts

21NS(67NS) or 21S operation–20 volts after 500 MS time delay

21NS(67NS) or 21S and both receiver trip signal operation (one receiver trip signal for 2 Term Line relays) - 0 volts

Test Terminal 8 and 9: Pos. 20 V DC

Normal Condition - 0 volts

Test Terminal 10: Negative DC

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing the repair work. When ordering parts, always give the complete nameplate data, and the component Style No. given in the Electrical Parts List.

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	REFERENCE	STYLE
POWER SUPPLY BOARD – S#202C465G01		
Capacitors		
C1, C2	6.8 MFD, 35 V, ±20%	184A661H10
Diodes		
D1, D2	1N645A	837A692H03
Resistors		
None on PCB	None	
Transistors		
Q1, Q2	2N3589	837A617H01
Zener Diodes		
Z1, Z3	1N3050A (180 V - 1W)	187A936H16
Z2, Z4	1N4747A (20 V - 1W)	849A487H01
Heat Sink for A1 & Q2		849A517H01
WEAK FEED – S#6262D69G01 – ELEC. MECH. SYSTEM **LOGIC 1 BOARD – S#6262D69G02 – SOLID STATE SYSTEM**		
Capacitors		
C1, C2	.047 mfd, 200 VDC	849A437H04
C3, C4	22 mfd, 35 V DC	184A661H16
C5	.27 mfd, 200 V DC	188A669H05
C6	.47 mfd, 35 V DC	837A241H21
Diodes		
D1, D2, D3, D4, D5	1N645A	837A692H03
Resistors		
R1, R2, R7, R8 △	4.7 K, ½ W, ±2%	629A531H48
R1, R2, R7, R8 *	47 K, ½ W, ±2%	629A531H72
R3, R9	4.7K, ½ W, ±2%	629A531H48
R4, R10, R27, R45	82K, ½ W, ±2%	629A531H78
R5, R11, R15, R18, R21, R24, R26, R30, R33, R37, R40, R43, R44	10 K, ½ W, ±2%	629A531H56
R6, R12, R16, R25, R31, R38	6.8K, ½ W, ±2%	629A531H52
R13, R14, R17, R29, R34, R35, R36, R39, R41	27K, ½ W, ±2%	629A531H66
R19	39K, ½ W, ±2%	629A531H70
R20, R23	470 ohms, ½ W, ±2%	629A531H24
R22	47K, ½ W, ±2%	629A531H72
R28	150 Ohms, 3 W, ±5%	762A679H01
R32	1K, ½ W, ±2%	629A531H32
Transistors		
Q1, Q2, Q3, Q4, Q5, Q6, Q8, Q10, Q11	2N3417	848A851H02
Q7, Q12	2N3645	849A441H01
Q9	2N3589	837A617H01

△ – Solid State Systems # – Elec. Mech Systems

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	REFERENCE	STYLE
WEAK FEED LOGIC 1 BOARD (continued)		
Zener Diodes		
Z1, Z2, Z5, Z6, Z11	IN3688A	862A288H01
Z3, Z7	IN3686B	185A212H06
Z4, Z8, Z9, Z10	IN957B	186A797H06
Z12	IN3050B	187A936H17
WEAK FEED LOGIC 2 BOARD S#6262D57G01 – SOLID STATE SYSTEMS; S#6262D57G02 – ELEC. MECH. SYSTEMS		
Capacitors		
C1, C2, C3	.047 mfd, 200 VDC	849A437H04
C4	.15 mfd, 35 VDC	837A241H13
Diodes		
D1, D2, D3, D4, D5	IN645A	837A692H03
Resistors		
R1, R6, R12 Δ	4.7K, ½W, ± 2%	629A531H48
R1, R6, R12 #	47K, ½W, ± 2%	629A531H72
R2, R7, R13	4.7K, ½W, ± 2%	629A531H48
R3, R8, R14	82K, ½W, ± 2%	629A531H78
R4, R9, R15, R20, R23, R28, R30, R33, R36	10K, ½W, ± 2%	629A531H56
R5, R11, R17, R21, R24, R29, R34, R37	6.8K, ½W, ± 2%	629A531H52
R10, R16, R18, R19, R22, R25, R26, R27, R35	27K, ½W, ± 2%	629A531H39
R31	2K, ½W, ± 2%	629A531H60
R32	15K, ½W, ± 2%	
Transistors		
Q1, Q2, Q3, Q4, Q5, Q6, Q8, Q9	2N3417	848A851H02
Q7	2N3645	849A441H01
Zener Diodes		
Z1, Z3, Z5	IN3686B	185A212H06
Z2, Z4, Z6	IN957B	186A797H06
WEAK FEED LOGIC 3 BOARD S#6262D65G01 – SOLID STATE SYSTEMS; S#6262D65D02 – ELEC. MECH. SYSTEMS		
Capacitors		
C1	3.3 mfd, 35 VDC	862A530H01
C2, C3	.047 mfd, 200 VDC	849A437H04
C4	.47 mfd, 35 VDC	837A241H21
Diodes		
D1, D2, D3, D4, D5	IN645A	837A692H03

Δ – Solid State Systems # – Elec. Mech. Systems

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	REFERENCE	STYLE
WEAK FEED LOGIC 3 BOARD (continued)		
Resistors		
R1, R7, R14, R20, R21, R22, R24, R25, R30, R32	27K, ½W, ± 2%	629A531H66
R2, R5, R8, R13, R17, R26, R28, R31, R33, R35	10K, ½W, ± 2%	629A531H56
R3	30K, ½W, ± 2%	629A531H67
R4	470 ohm, ½W, ± 2%	629A531H24
R6, R9, R15, R23, R27	6.8K, ½W, ± 2%	629A531H52
R10, R16 Δ	4.7K, ½W, ± 2%	629A531H48
R10, R16 #	47K, ½W, ± 2%	629A531H72
R11, R17	4.7K, ½W, ± 2%	629A531H48
R12, R18, R29, R36	82 K, ½W, ± 2%	629A531H78
R34	15K, ½W, ± 2%	629A531H60
Transistors		
Q1, Q2, Q3, Q4, Q5, Q6, Q8	2N3417	848A851H02
Q7, Q9	2N3645	849A441H01
Zener Diodes		
Z1, Z3, Z5	IN957B	186A797H06
Z2, Z4	IN3686B	185A212H06
WEAK FEED S#6262D74G01 – SOLID STATE SYSTEM LOGIC 4 BOARD S#6262D74G02 – ELEC. MECH. SYSTEM		
Capacitors		
C1	.047 mfd, 200 VDC	849A437H04
C2	4.7 mfd, 35 VDC	184A661H12
C3	.47 mfd, 35 VDC	837A241H21
Diodes		
D1, D3, D4, D5, D6	IN645A	837A692H03
Resistors		
R1, R2, R5, R6, R12, R14, R15, R22, R29, R31, R32, R33	27K, ½W, ± 2%	629A531H66
R3, R7, R13, R20, R23, R26, R28, R34	10K, ½W, ± 2%	629A531H56
R4, R8, R16, R19, R21, R27, R30, R35	6.8K, ½W, ± 2%	629A531H52
R9 Δ	4.7K, ½W, ± 2%	629A531H48
R9 #	47K, ½W, ± 2%	629A531H72
R10	4.7K, ½W, ± 2%	629A531H48
R11	82K, ½W, ± 2%	629A531H78
R17	22K, ½W, ± 2%	629A531H64
R18	2.7K, ½W, ± 2%	629A531H42
R24	33K, ½W, ± 2%	629A531H68
R25	470 ohms, ½W, ± 2%	629A531H24
Transistors		
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	2N3417	848A851H02
Zener Diodes		
Z1	IN3686B	185A212H06
Z2, Z3, Z4	IN957B	186A797H06

Δ – Solid State System

– Elec. Mech. System

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	REFERENCE	STYLE
CHANNEL – S#202C530G01 – TCT INT. **INTERFACE BOARD – S#202C469G01 – TA3 INT.**		
Capacitors		
C1, C3, C5	.047 mfd, 200 V DC	849A437H04
C4, C6	.27 mfd, 200 V DC	188A669H05
Diodes		
D2, D3	1N645A	837A692H03
Resistors		
R1, R2, R9, R10, R17, R18	4.7 K, ½W, ± 2%	629A531H48
R3, R7, R11, R15, R19, R23	82 K, ½W, ± 2%	629A531H78
R4, R5, R12, R13, R20, R21, R26	10 K, ½W, ± 2%	629A531H56
R6, R14, R22, R27	6.8 K, ½W, ± 2%	629A531H52
R16, R24	150 ohm, 3W, ± 5%	762A679H01
R25	27 K, ½W, ± 2%	629A531H66
Transistors		
Q1, Q3, Q5, Q7	2N3417	848A851H02
Q2, Q4, Q6	2N3645	849A441H01
Zener Diodes		
Z1, Z4, Z7	1N3686B, 20 V, ± 5%	185A212H06
Z2, Z5, Z8	1N957B, 6.8 V, ± 5%	186A797H06
Z6, Z9, Z10	1N3688A, 24 V, ± 20%	862A288H01
CHANNEL – S#202C471G01 – TCF **TRIP BOARD – S#202C472G01 – TONE**		
Capacitors		
C1	0.27 mfd, 200 V	188A669H05
Diodes		
D1	1N645A	837A692H03
Resistors		
R1, R2, R5, R8, R11, R14, R17, R18, R21, R22, R25, R26, R29, R32, R33, R34, R37, R43	27 K, ½W, ± 2%	629A531H66
R3, R6, R9, R12, R15, R19, R23, R27, R30, R35, R38, R39	10K, ½W, ± 2%	629A531H56
R4, R7, R10, R13, R16, R20, R24, R28, R31, R36, R40	6.8 K, ½W ± 2%	629A531H52
R41	82 K, ½W, ± 2%	629A531H78
R42	150 ohm, 3 W, ± 5%	762A679H01

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	REFERENCE	STYLE
CHANNEL TRIP BOARD (continued)		
Transistors		
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11	2N3417	848A851H02
Zener Diodes		
Z1	1N3688A, 24 V, ± 10%	862A288H01
TCF CHANNEL SUPERVISION BOARD – S#202C532G01		
Resistors		
R1, R2, R9, R22, R23, R26	27 K, ½W, ± 2%	629A531H66
R3, R4, R10, R13, R24, R27	10 K, ½W, ± 2%	629A531H56
R5, R11, R25, R28	6.8 K, ½W, ± 2%	629A531H52
R12	1 K, ½W, ± 2%	629A531H32
Transistors		
Q1, Q4, Q8, Q9	2N3417	848A851H02
Q2	2N3645	849A441H01
Q5	2N3589	837A617H01
Zener Diodes		
Z1	1N3050B, 180 V	187A936H17
TONE CHANNEL – S#202C474G01 – ELEC. MECH. SYSTEMS SUPERVISION BOARD – S#202C533G01 – SOLID STATE SYSTEMS		
Capacitors		
C1	12 mfd, 35 V, ± 10%	862A530H05
Diodes		
D1, D2, D3	1N645A	837A692H03
Resistors		
R1, R2, R3, R6, R15, R20, R23, R24, R25, R28, R29, R32	27 K, ½W ± 2%	629A531H66
R4, R7, R12, R13, R16, R19, R21, R26, R30, R33	10 K, ½W, ± 2%	629A531H56
R5, R8, R14, R17, R22, R27, R31, R34	6.8 K, ½W, ± 2%	629A531H52
R9 Δ	22 K, ½W, ± 2%	629A531H64
R10 Δ	10K, ½W, ± 2%	629A531H56
R11	15 K, ½W, ± 2%	629A531H60
R18	1 K, ½W, ± 2%	629A531H32
Transistors		
Q1, Q2, Q3, Q5, Q7, Q8, Q9, Q10	2N3417	848A851H02
Q4	2N3645	849A441H01
Q6	2N3589	837A617H01
Zener Diodes		
Z1	1N957B, 6.8 V, ± 5%	186A797H06
Z2	1N3050B, 180 V	187A936H17

Δ – Indicates typical value

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	REFERENCE	STYLE
TRANSMITTER – S#202C634G01 – TCF CH. KEY BOARD – S#202C535G01 – TONE CH.		
Capacitors		
C1, C2	0.27 mfd, 200 V DC	188A699H05
Diodes		
D1, D2, D3, D4, D5, D6, D7	1N645A	837A692H03
Resistors		
R1, R2, R3, R4, R5, R6, R7, R13	27 K, ½W, ± 2%	629A531H66
R8, R9, R12, R14, R15, R20	10 K, ½W, ± 2%	629A531H56
R10, R11, R16	6.8 K, ½W, ± 2%	629A531H52
R17	82 K, ½W, ± 2%	629A531H78
R18	150 ohm, 3 W, ± 5%	762A679H01
R19	4.7 K, ½W, ± 2%	629A531H48
Transistors		
Q1, Q4	2N3417	848A851H02
Q2, Q5	2N3645	849A441H01
Q3, Q6	2N3589	837A617H01
Zener Diodes		
Z1, Z3	1N3688A, 24 V, ± 10%	862A288H01
Z2, Z4	1N3050B, 180V	187A936H17
CHECKBACK BOARD – S#6263D17G01		
Capacitors		
C1, C2	150 mfd, 35 V	849A007H01
Diodes		
D1, D2, D3	1N645A	837A692H03
Resistors		
R1, R4, R7, R8, R15	27 K, ½W, ± 2%	629A531H66
R2, R5, R9, R12, R16	10 K, ½W, ± 2%	629A531H56
R3, R6, R17	6.8 K, ½W, ± 2%	629A531H52
R10 Δ, R13 Δ	33 K, ½W, ± 2%	629A531H68
R11, R14	470 ohm, ½W, ± 2%	629A531H24
Transistors		
Q1, Q2, Q3, Q4, Q5	2N3417	848A851H02
Zener Diodes		
Z1, Z2	1N957B, 6.8 V, ± 5%	186A797H06

Δ – Indicates typical value

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	REFERENCE	STYLE
TIMING BOARD – S#202C477G01		
Capacitors		
C1	.047 mfd, 200 V	849A437H04
C2	12 mfd, 35 V, ± 10%	862A530H05
C3	1.5 mfd, 35 V, ± 5%	187A508H18
C4	150 mfd, 30 V, ± 10%	849A007H01
C5	1.0 mfd, 35 V, ± 10%	837A241H15
Diodes		
D1, D2, D3, D4, D5	1N645A	837A692H03
Resistors		
R1	47 K, ½W, ± 2%	629A531H72
R2	4.7K, ½W, ± 2%	629A531H48
R3	82 K, ½W, ± 2%	629A531H78
R4, R7, R10, R13, R16, R19, R22, R25, R28, R33	10 K, ½W, ± 2%	629A531H56
R5, R8, R14, R17, R23, R26, R34	6.8 K, ½W, ± 2%	629A531H52
R6, R9, R15, R18, R24, R27, R31, R32, R35	27 K, ½W, ± 2%	629A531H66
R11 Δ	30 K, ½W, ± 2%	629A531H67
R12, R21, R30	470 ohm, ½W, ± 2%	629A531H24
R20 Δ, R29 Δ	33 K, ½W, ± 2%	629A531H68
Transistors		
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10	2N3417	848A851H02
Zener Diodes		
Z1	1N368B, 20 V, ± 5%	185A212H06
Z2, Z3, Z4, Z5	1N957B, 6.8 V, ± 5%	186A797H06
ARMING BOARD – S#202C478G01		
Capacitors		
C1	22 mfd, 35 V, ± 10%	184A661H16
C2	3.3 mfd, 35 V, ± 5%	862A530H01
Diodes		
D1, S2, D3, D4, D5	1N645A	837A692H03
Resistors		
R1, R2, R5, R9, R10, R16, R20, R23, R24, R25	27 K, ½W, ± 2%	629A531H66
R3, R6, R11, R12, R18, R21, R26, R27, R32, R36	10 K, ½W, ± 2%	629A531H56
R4, R7, R13, R19, R22, R28, R33	6.8 K, ½W, ± 2%	629A531H52
R14	82 K, ½W, ± 2%	629A531H78
R15	20 K, ½W, ± 2%	629A531H63
R29, R34	1K, ½W, ± 2%	629A531H32
R30	100 ohm, ½W, ± 2%	629A531H08
R31 Δ	15 K, ½W, ± 2%	629A531H60
R35	12K, ½W, ± 2%	629A531H58
Transistors		
Q1, Q2, Q3, Q5, Q6, Q7, Q9, Q10	2N3417	848A851H02
Q4, Q8	2N3645	849A441H01

Δ – Indicates typical value

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	REFERENCE	STYLE
OUTPUT BOARD S#202C479G01		
Capacitors		
C1	1.5 mfd, 35 V, ± 10%	187A508H18
C2, C4, C7	0.22 mfd, 100 V	763A219H21
C3	3.3 mfd, 35 V, ± 10%	862A530H01
C6	0.047 mfd, 200 V	849A437H04
C8, C9	0.1 mfd, 200 V	188A669H03
C10	0.27 mfd, 200V	188A669H05
Diodes		
D1, D2, D3, D4, D5, D6, D7, D8	1N645A	837A692H03
Potentiometers		
R1	50 K, ¼W, ± 20%	629A430H01
R14	15 K, ¼W, ± 20%	629A430H08
R20	1 K, ¼W, ± 20%	629A430H02
Resistors		
R2, R7, R9, R12, R18, R21, R23, R24, R25, R26, R30 R31, R34, R36, R37	10 K, ½W, ± 2%	629A531H56
R3	150 K, ½W, ± 5%	629A531H84
R6	47 ohm, ½W, ± 5%	187A290H17
R8, R35	27 K, ½W, ± 2%	629A531H66
R10, R15	470 ohm, ½W, ± 2%	629A531H24
R11	470 K, ½W, ± 5%	184A763H91
R16, R28	4.7 K, ½W, ± 2%	629A531H48
R4, R17, R19, R22, R29	22 K, ½W, ± 2%	629A531H64
R5, R27, R32, R33, R38	6.8 K, ½W, ± 2%	629A531H52
R39	82 K, ½W, ± 2%	629A531H78
R40	150 ohm, 3W, ± 5%	762A679H01
R13	15K, ½W, ± 2%	629A531H60
Transistors		
Q1, Q4, Q5, Q6, Q8, Q11	2N3645	849A441H01
Q2, Q3, Q7, Q10	2N3417	848A851H02
Q9	2N3589	837A617H01
Zener Diodes		
Z1, Z7	1N3688A, 24 V, ± 10%	862A288H01
Z2, Z3, Z4, Z5	1N957B, 6.8 V, ± 5%	186A797H06
Z6	1N3050B, 180 V	187A936H17
TEST BOARD – S#5490D87G01		
Tip Jacks (Red) 1, 2, 3, 4, 5, 6, 7, 8, 9		187A332H01
Tip Jacks (Black) 10		187A332H02

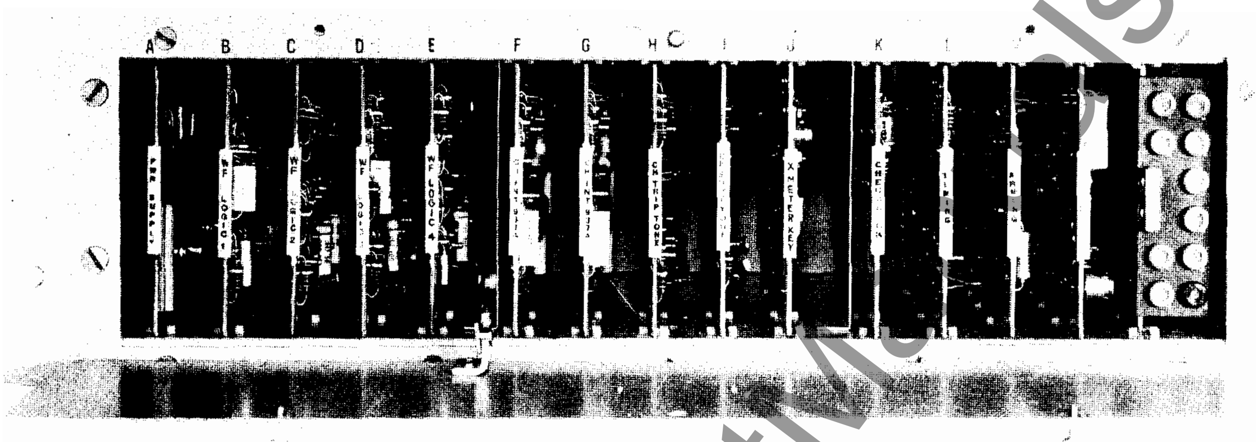


Fig. 1. Photograph (Front view with door open)

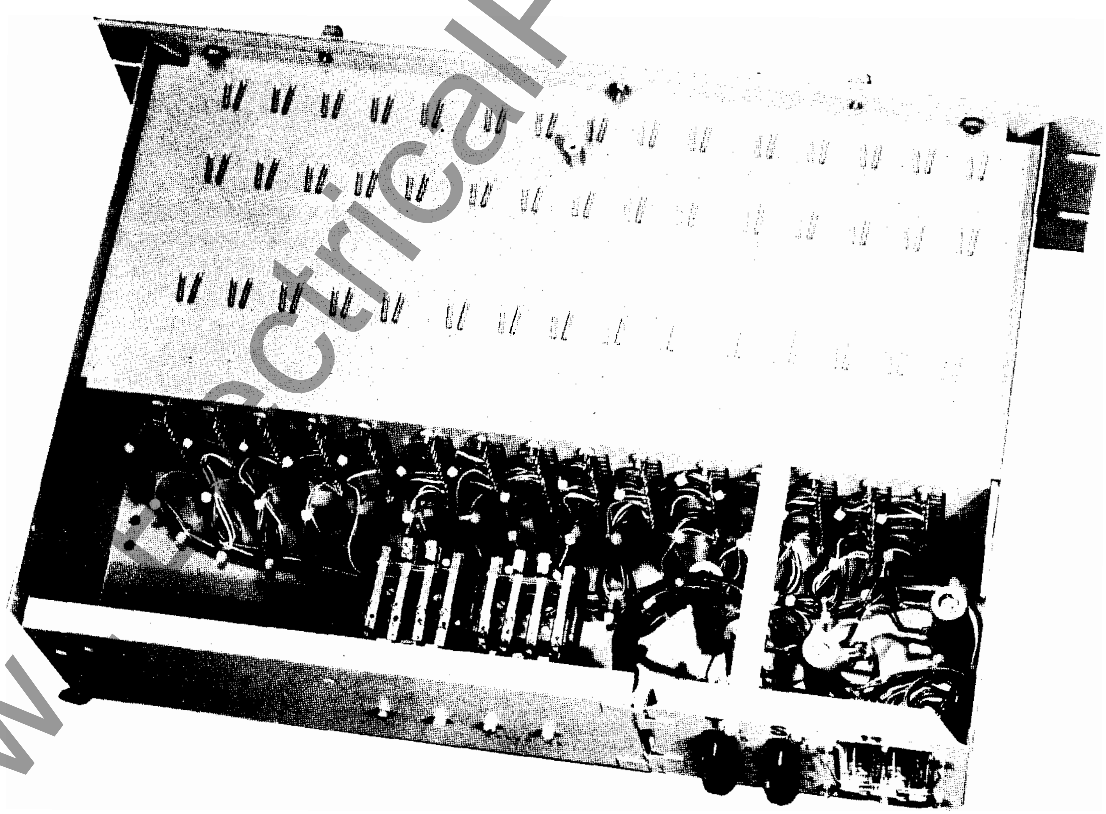
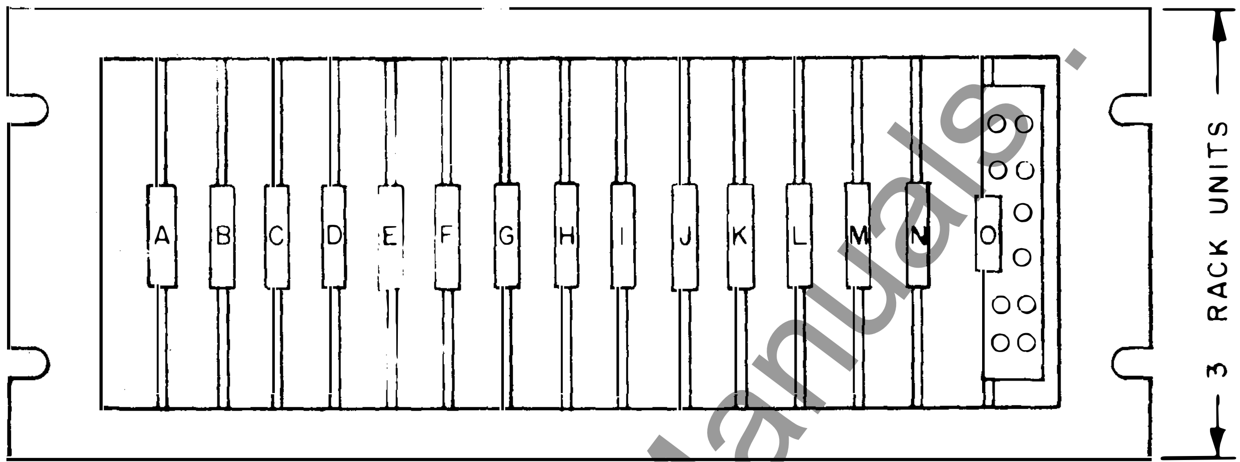


Fig. 2 Photograph (Rear view taken above relay with top cover off and door open)



FRONT VIEW
(COVER REMOVED)

BOARD POSITION	BOARD DESCRIPTION
A	POWER SUPPLY
B	**WEAK FEED LOGIC-1**
C	**WEAK FEED LOGIC-2**
D	**WEAK FEED LOGIC-3**
E	**WEAK FEED LOGIC-4**
F	CHANNEL 1 INTERFACE
G	CHANNEL 2 INTERFACE
H	CHANNEL TRIP
I	CHANNEL SUPERVISION
J	CHANNEL TRANSMITTER KEY
K	CHECK BACK
L	TIMING
M	ARMING
N	OUTPUT
O	TEST

878A323

Fig. 3 Relay component location

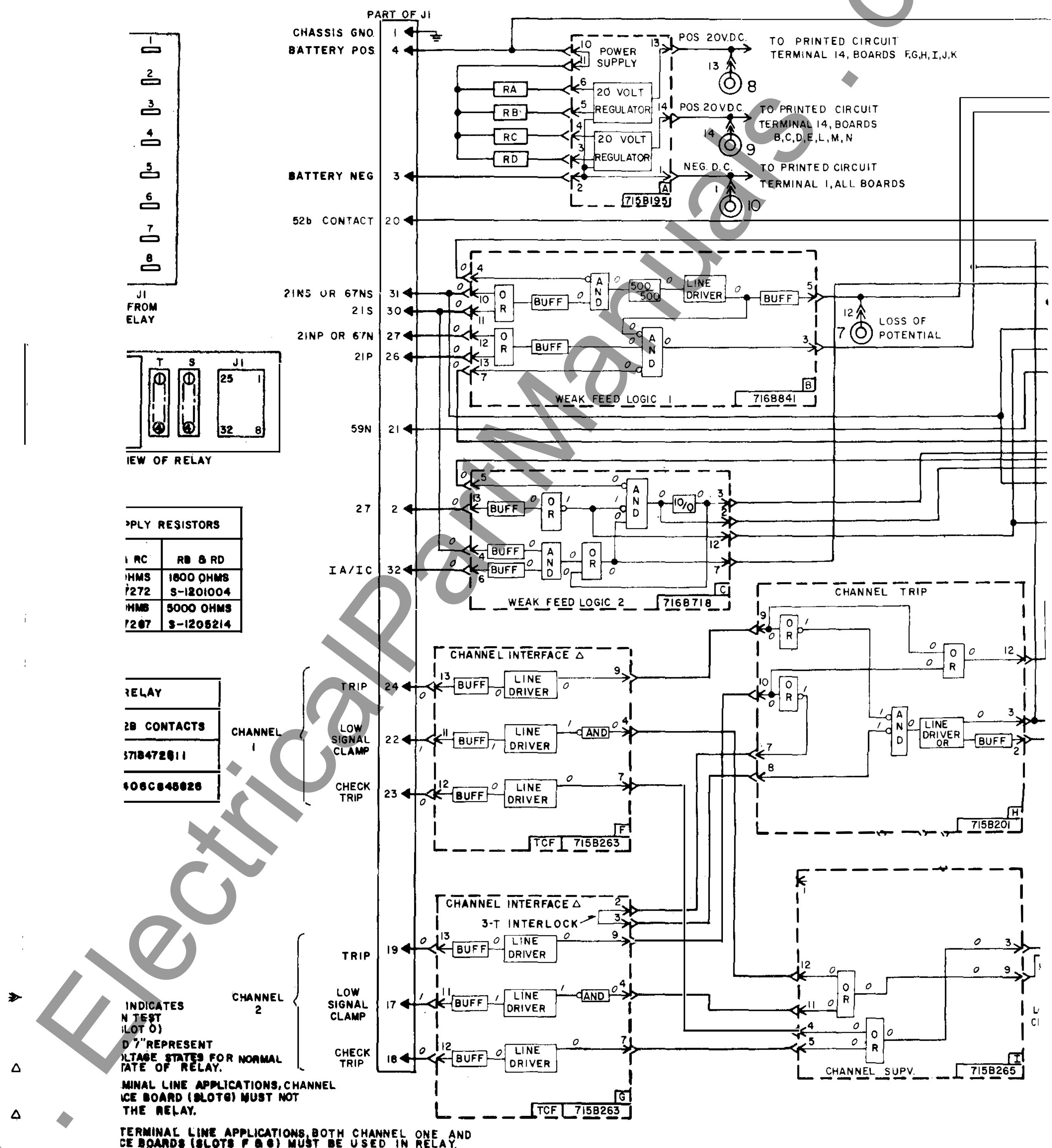
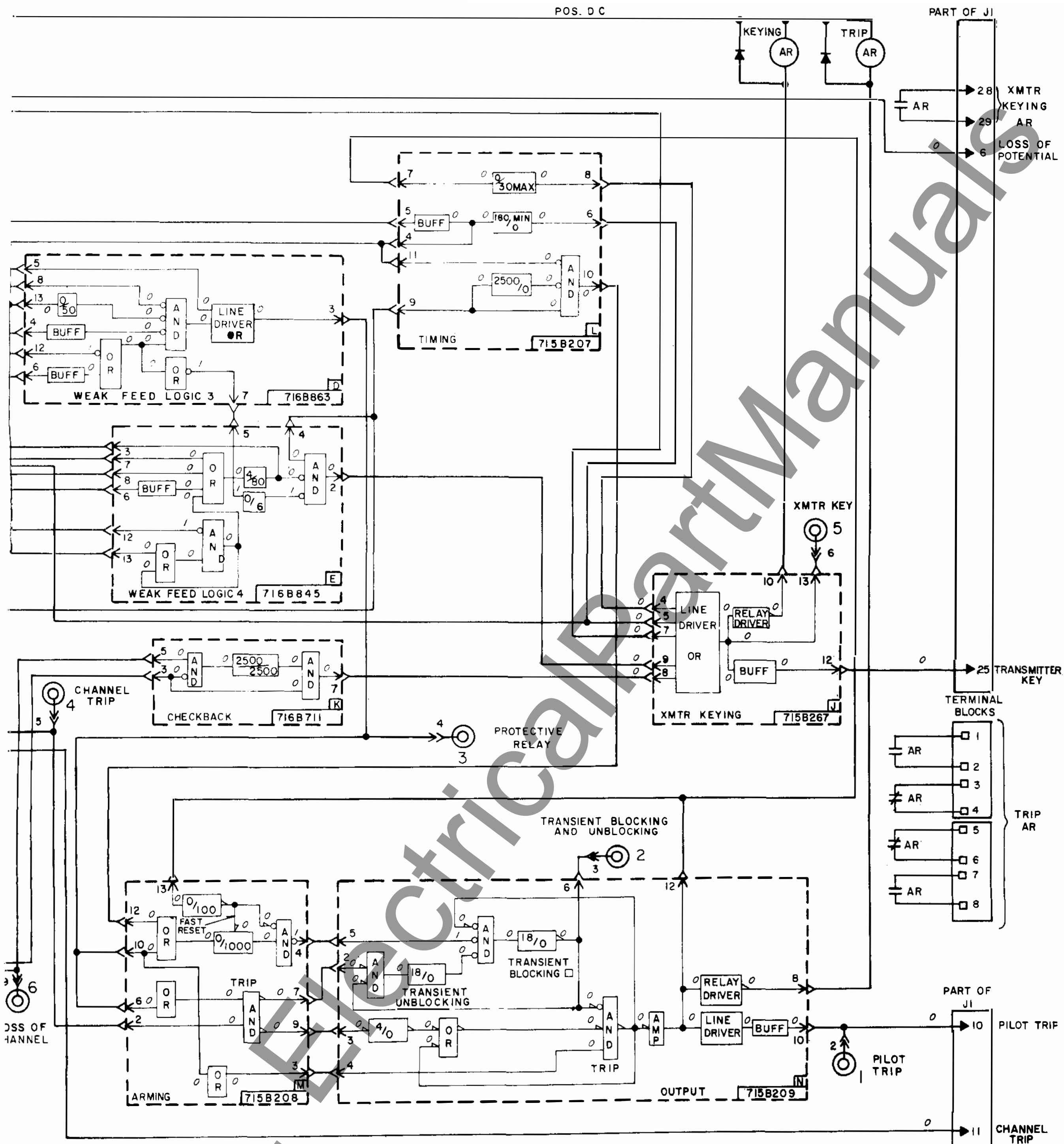


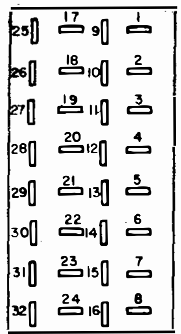
Fig. 5 STU-12 logic — for use with solid state protective



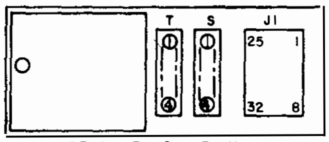
□ = RELAY STYLES AVAILABLE WITH TRANSIENT BLOCK TIME OF 25 MILLISECONDS

elays and a TCF carrier channel — for a weak feed terminal

6263D44



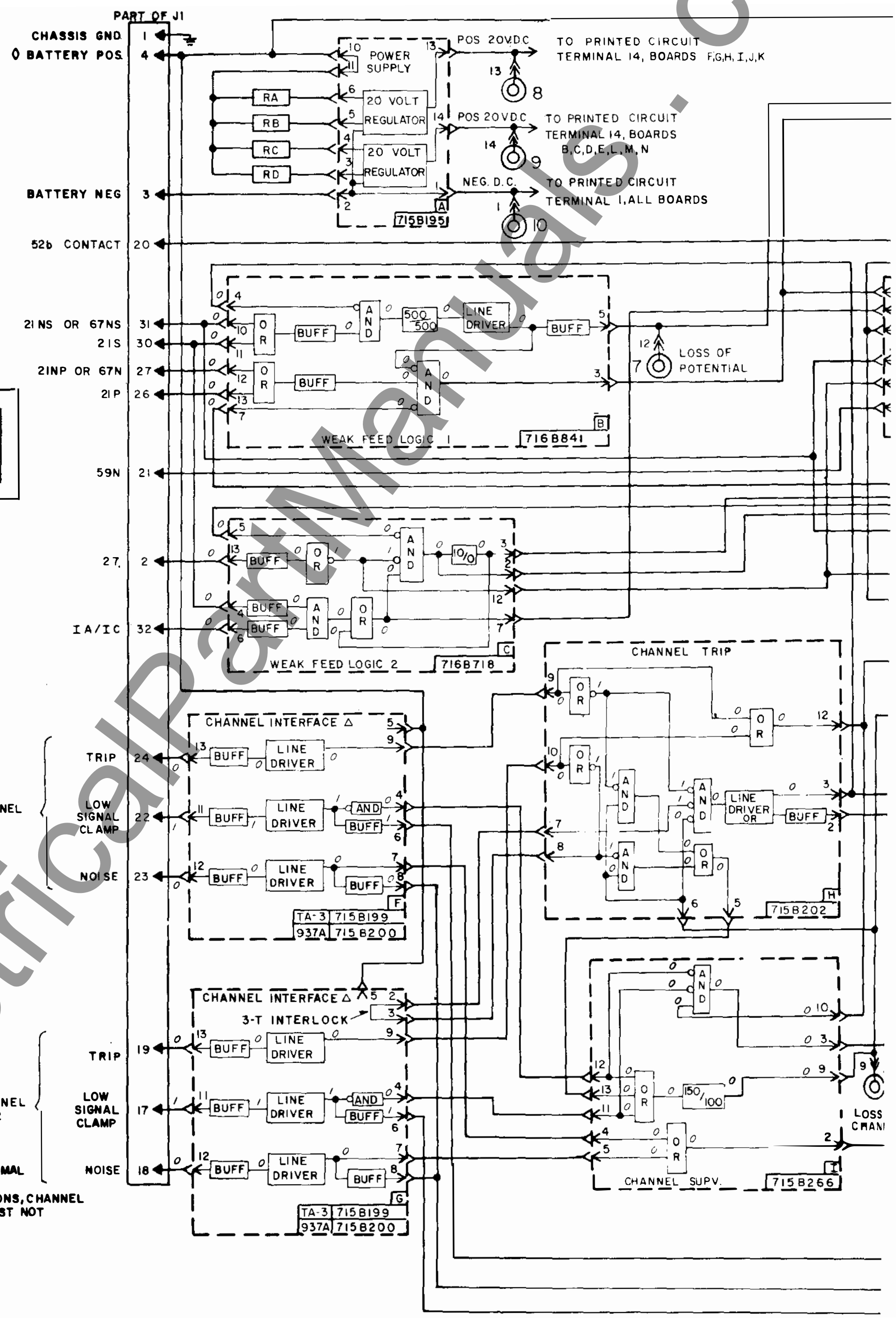
CONNECTOR J1
AS VIEWED FROM
REAR OF RELAY



REAR VIEW OF RELAY

POWER SUPPLY RESISTORS		
VOLT	RA & RC	RB & RD
48VDC	150 OHMS S-1267272	1800 OHMS S-1201004
125VDC	900 OHMS S-1267287	5000 OHMS S-1205214

AR RELAY	
VOLT	2M-2B CONTACTS
48VDC	S-6718472G11
125VDC	S-408C845G26



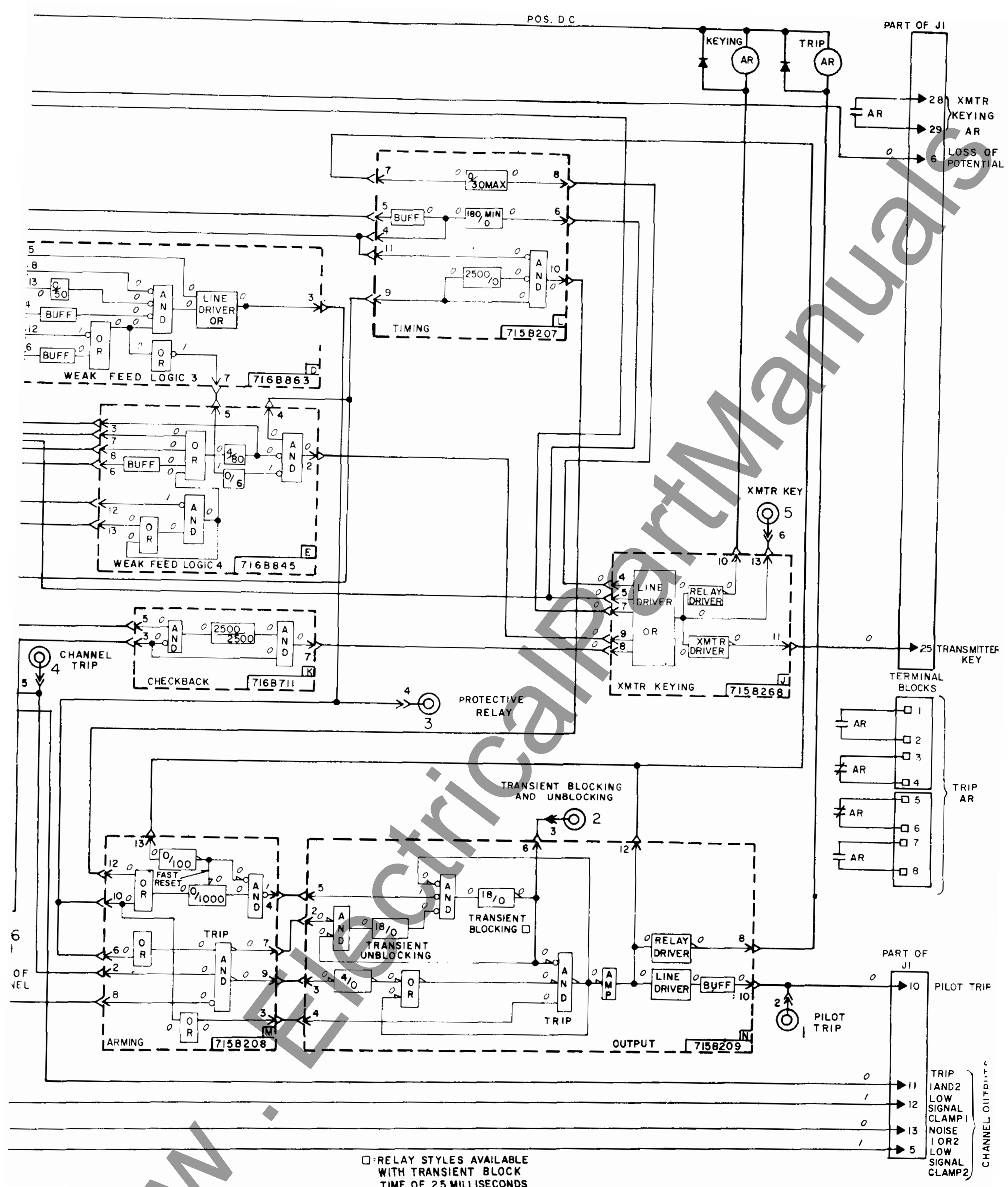
SYMBOL INDICATES POINT ON TEST BOARD (SLOT O)

SYMBOLS "0" AND "1" REPRESENT THE LOGIC VOLTAGE STATES FOR NORMAL OPERATING STATE OF RELAY.

Δ FOR TWO TERMINAL LINE APPLICATIONS, CHANNEL TWO INTERFACE BOARD (SLOT G) MUST NOT BE USED IN THE RELAY.

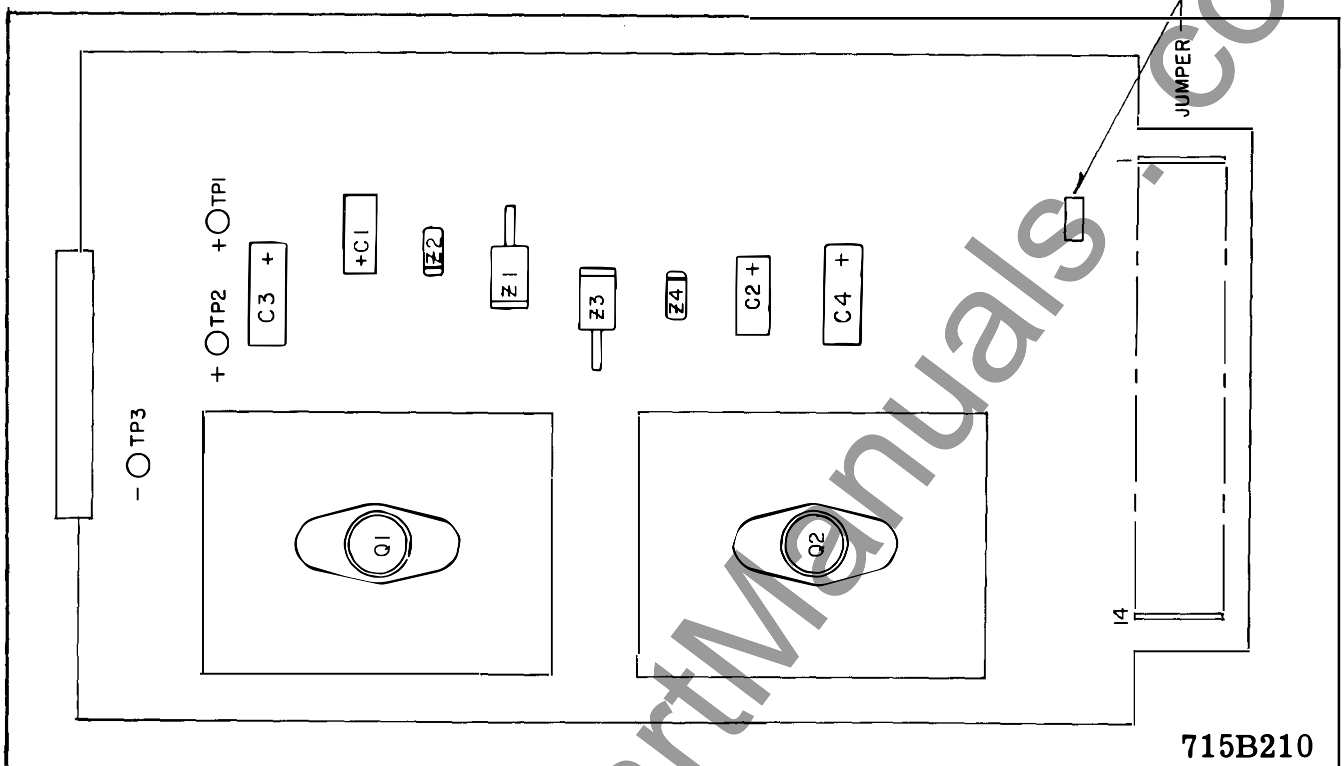
◊ FOR 937A TONES, ONLY 48VDC IS USED.

Fig. 7 STU-12 logic – for use with solid state protectiv

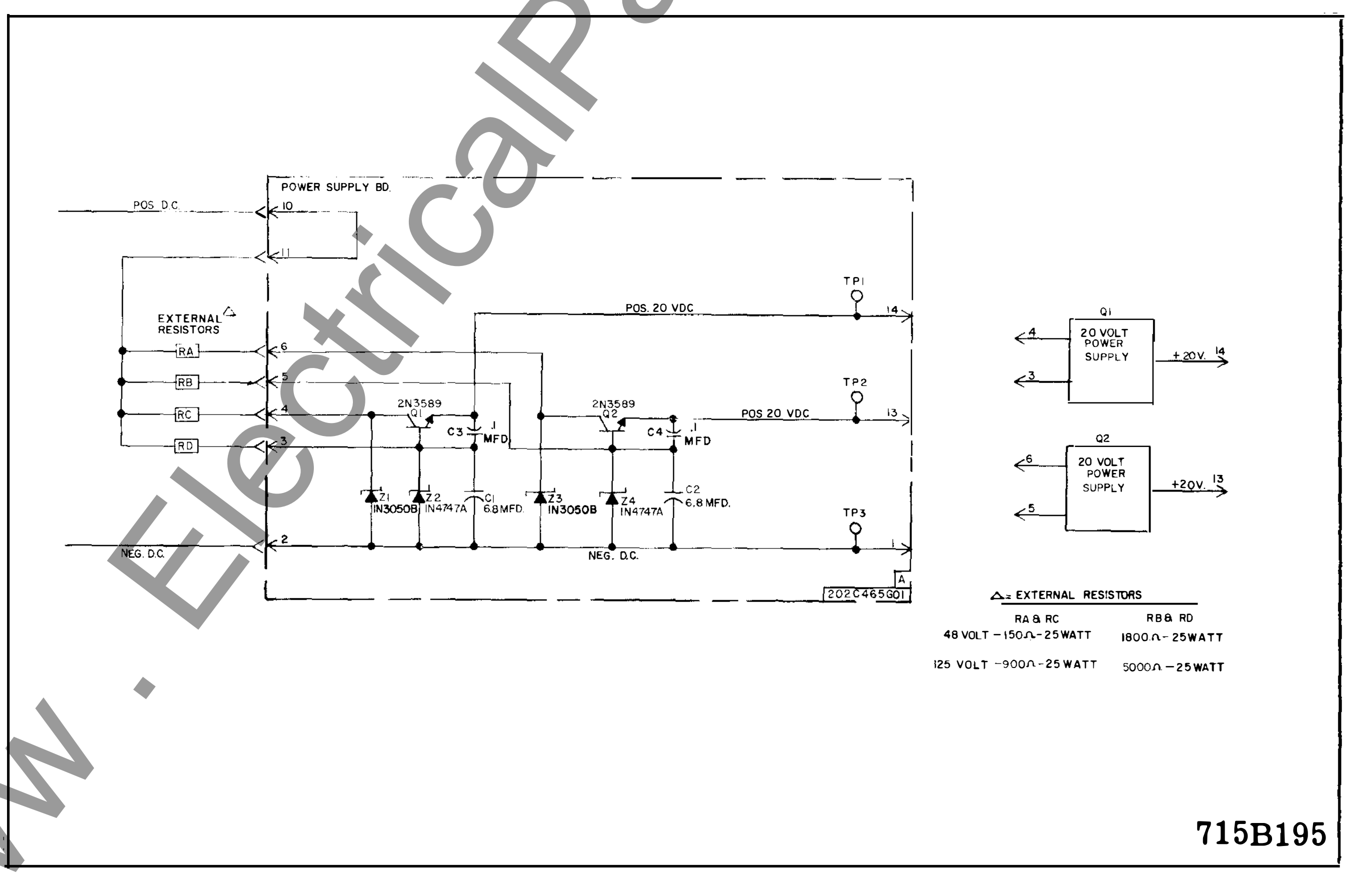


6263D46

e relays and a tone channel for a weak feed terminal



* *Fig. 8 Component Location Power Supply Board*



* *Fig. 9 Internal Schematic Power Supply Board*

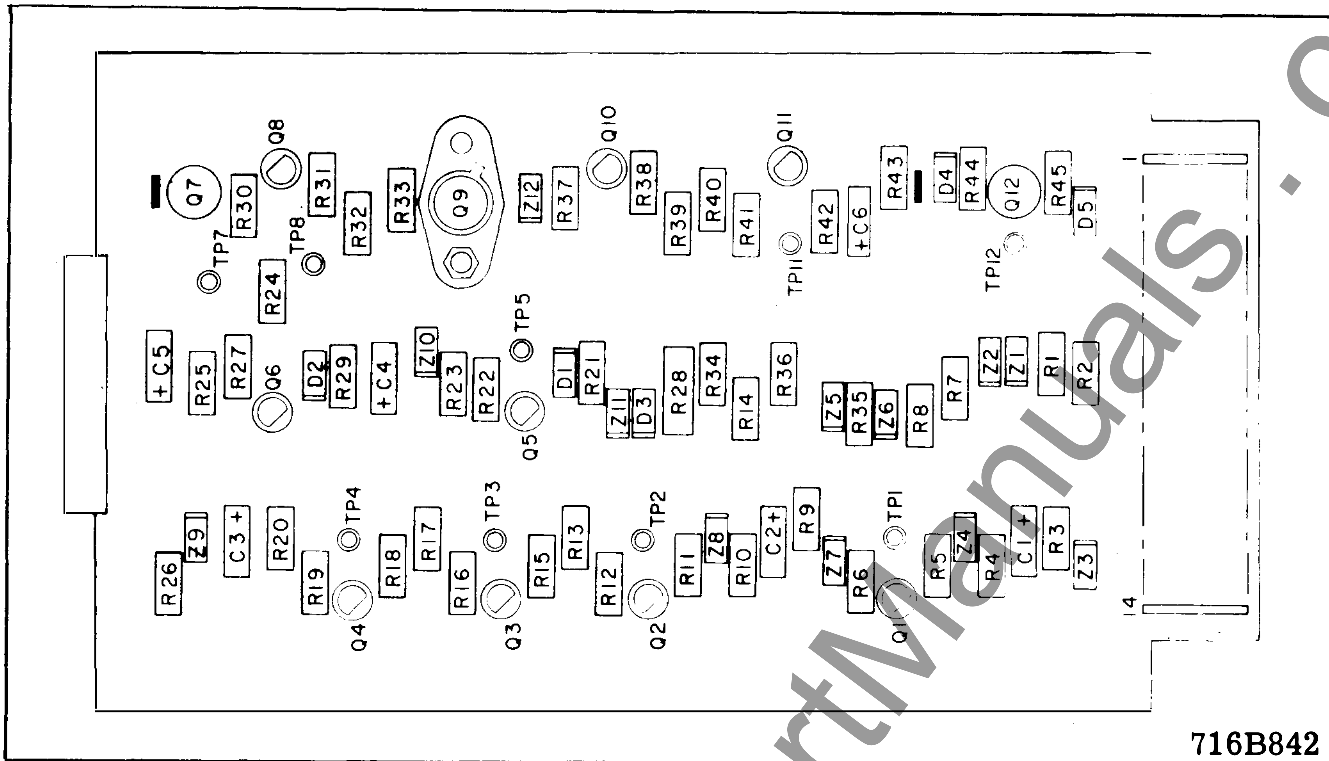


Fig. 10 Component Location – Weak Feed Logic 1 Board

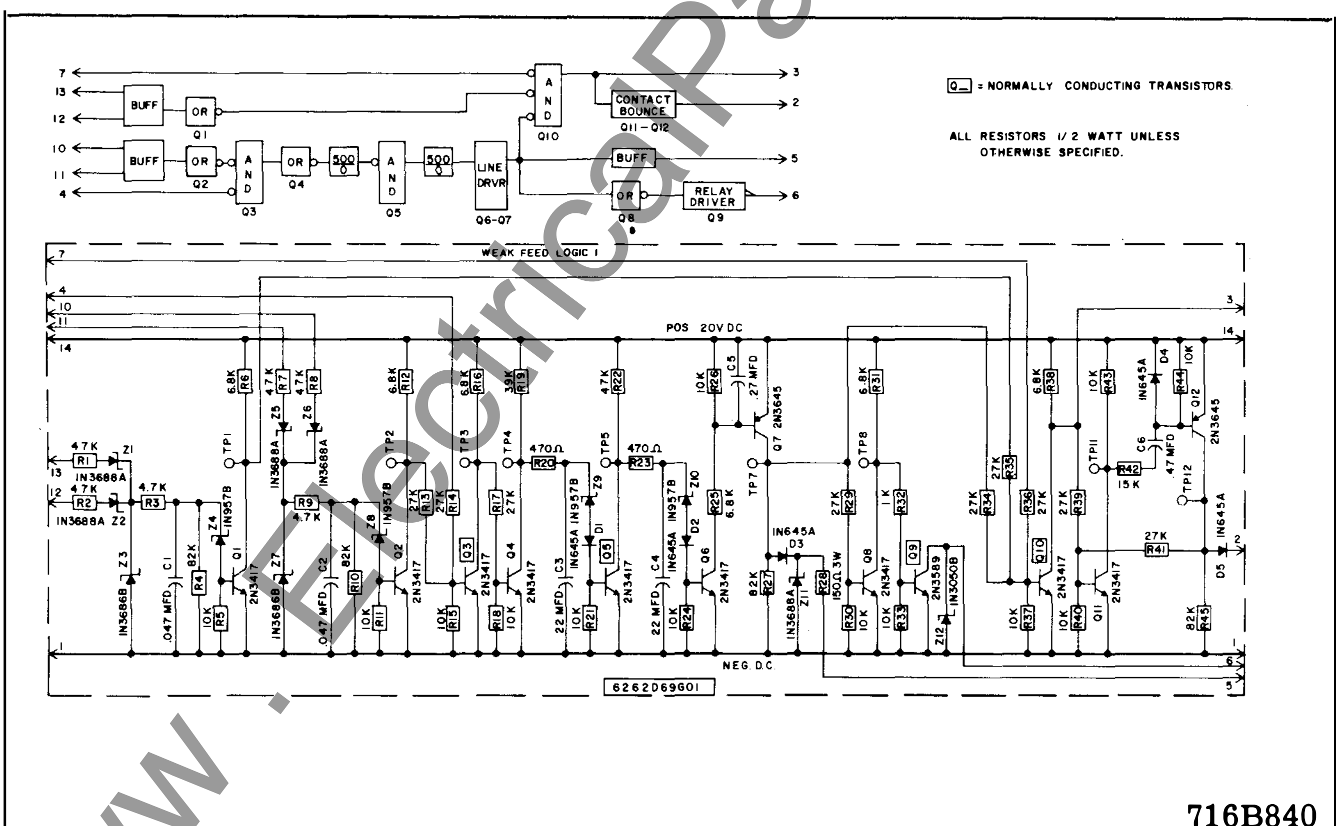


Fig. 11 Internal Schematic – Weak Feed Logic 1 Board for Elec. Mech. System

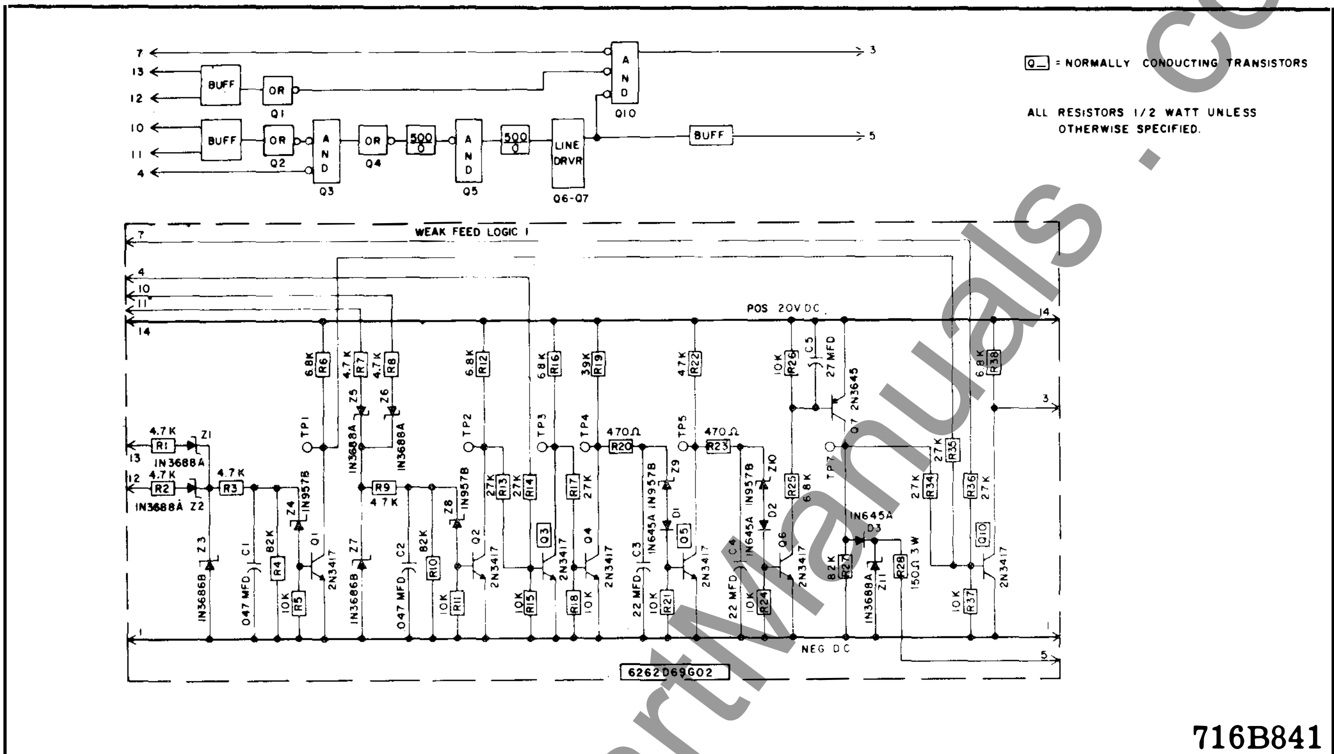


Fig. 12 Internal Schematic — Weak Feed Logic 1 Board for Solid State System

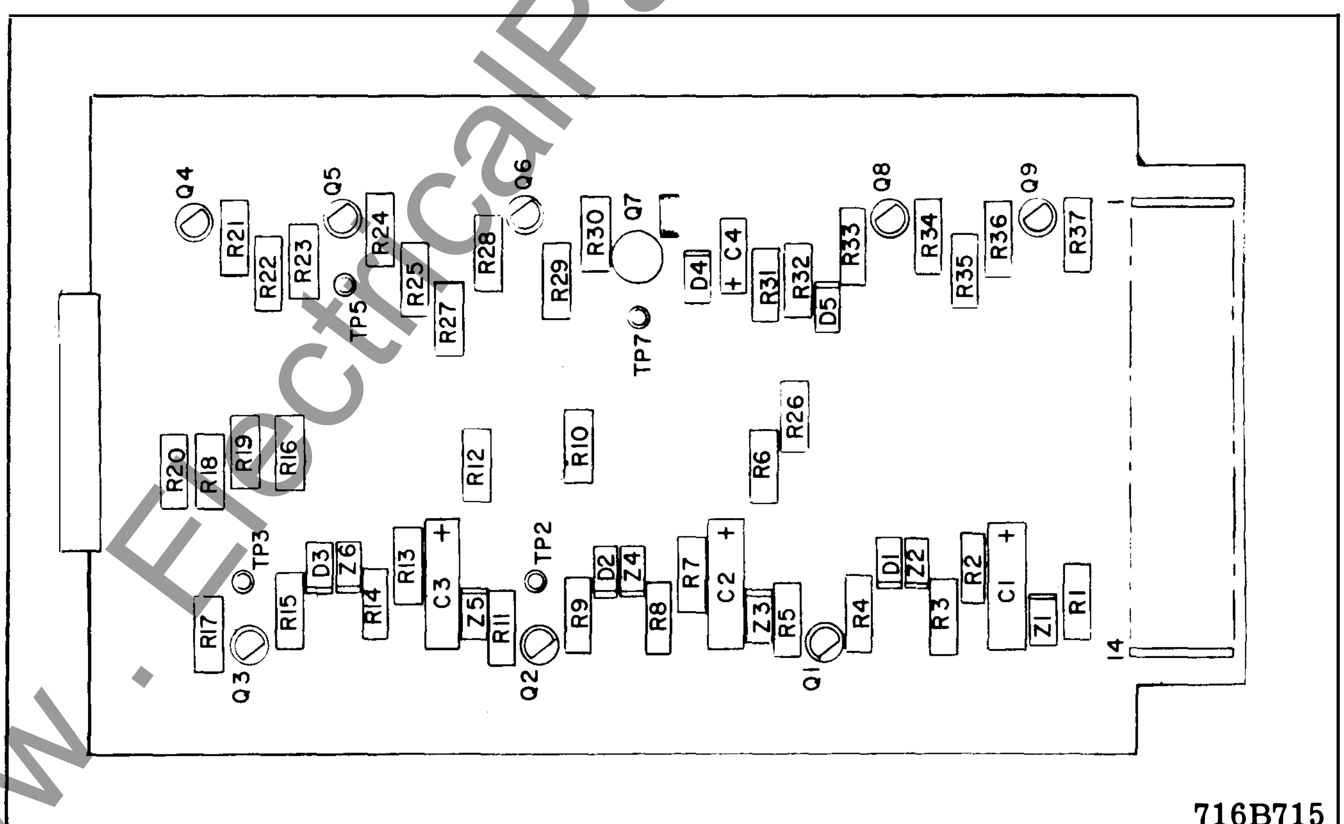


Fig. 13 Component Location — Weak Feed Logic 2 Board

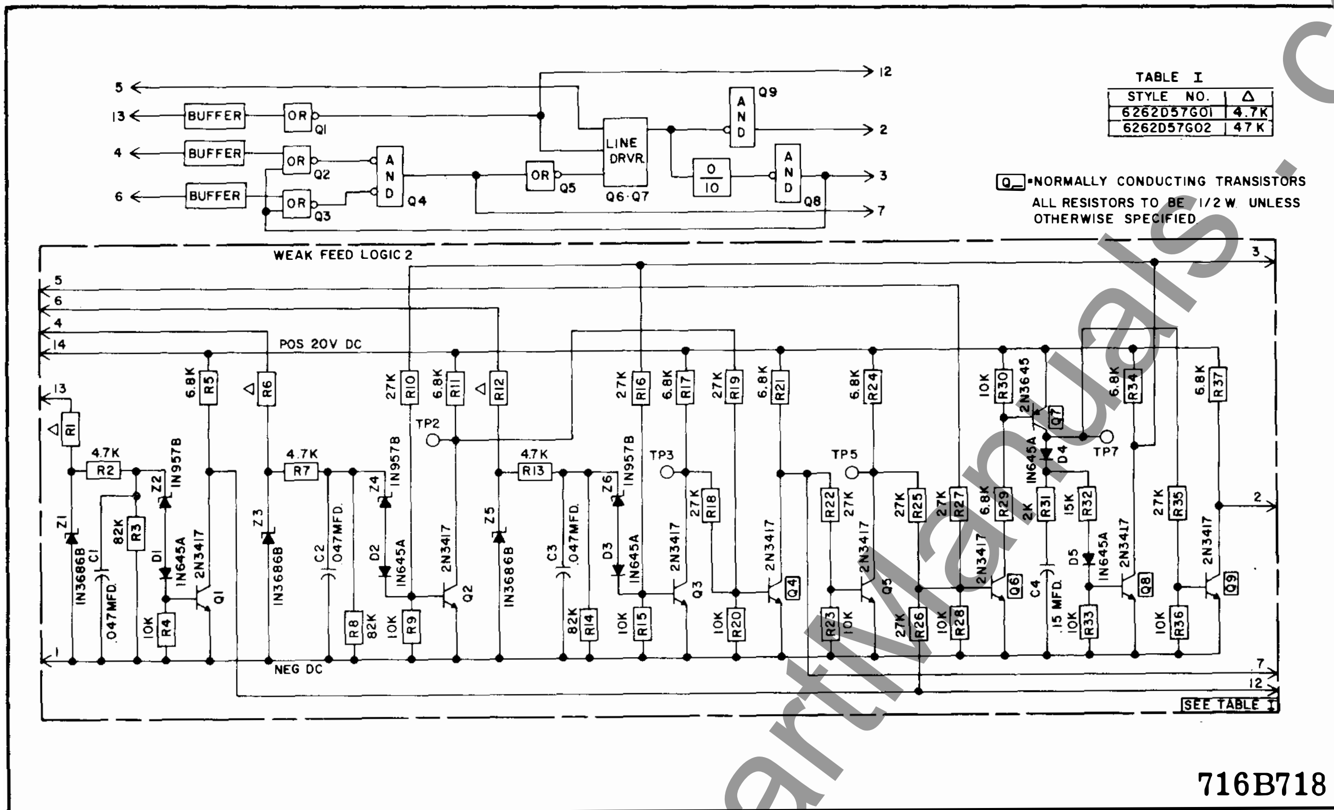


Fig. 14 Internal Schematic – Weak Feed Logic 2 Board

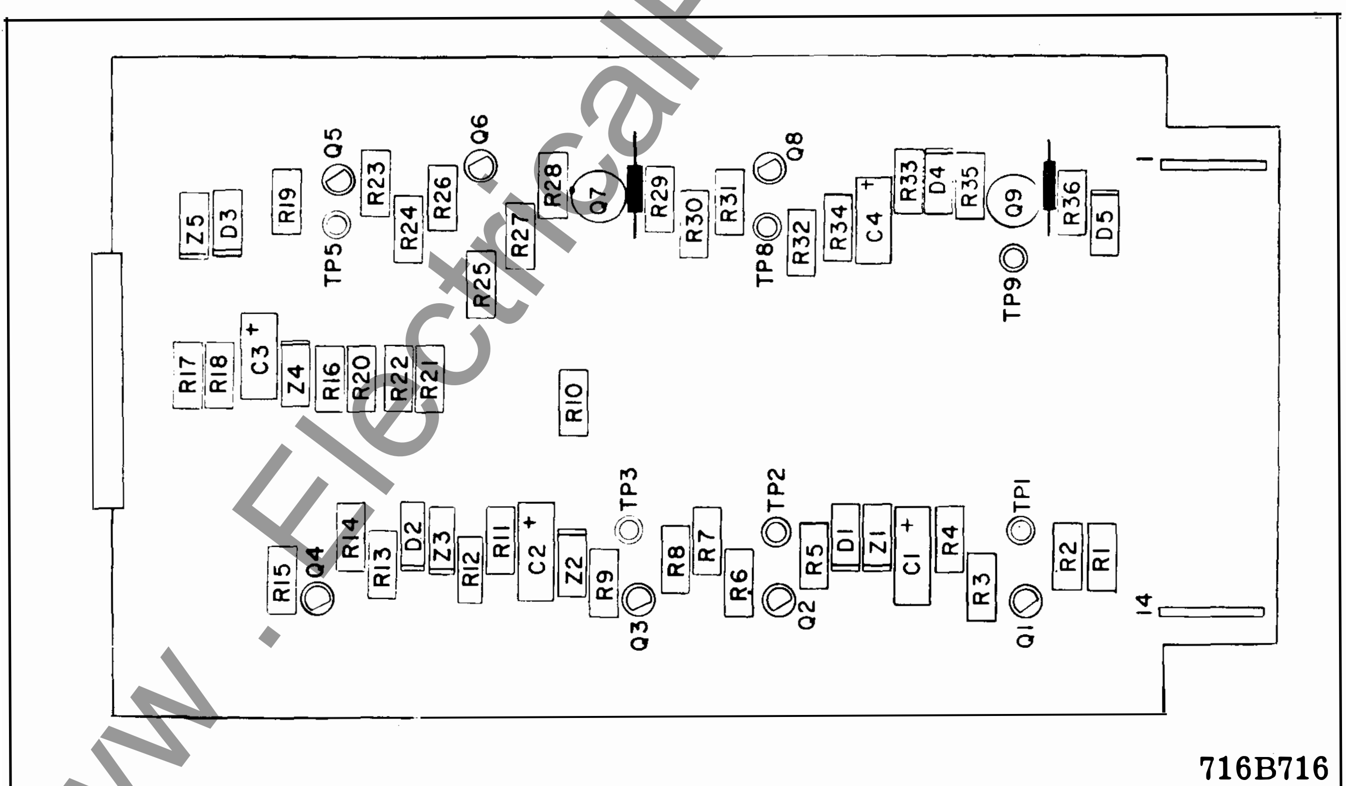


Fig. 15 Component Location – Weak Feed Logic 3 Board

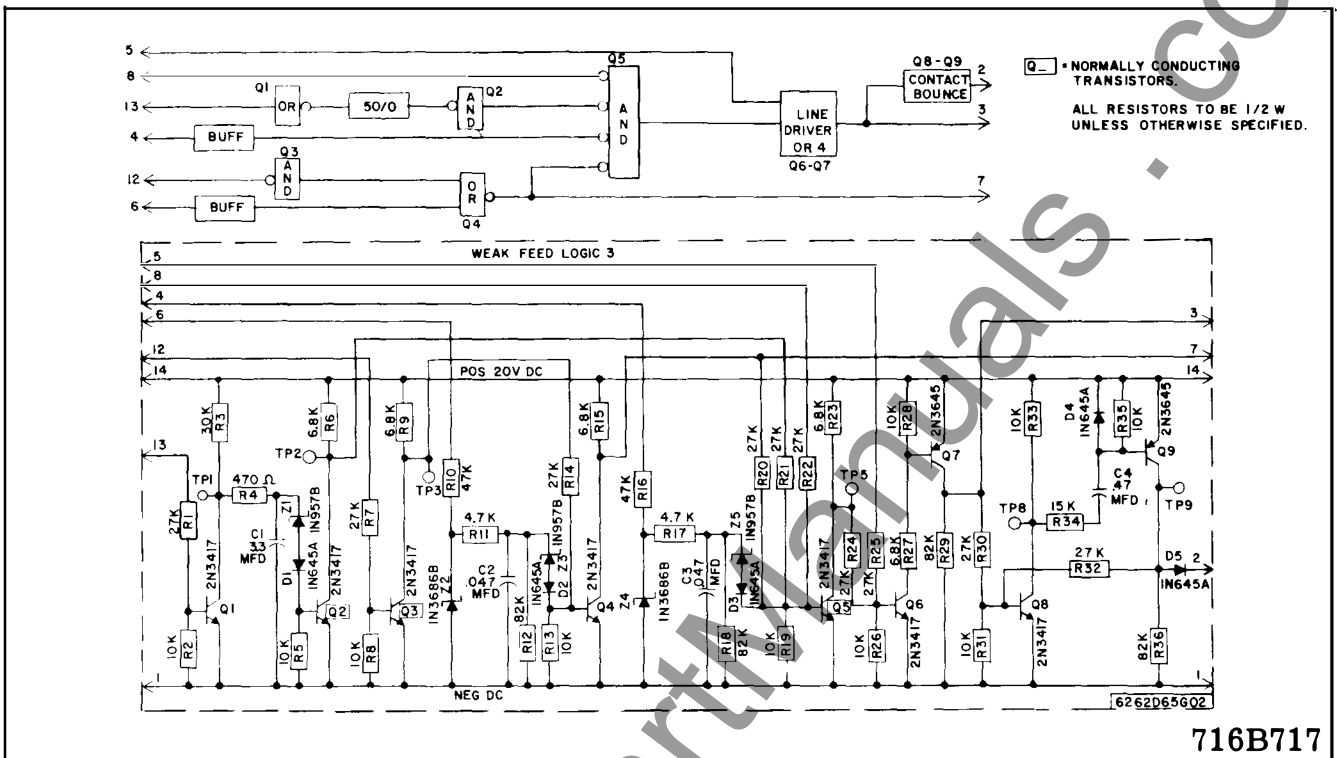


Fig. 16 Internal Schematic — Weak Feed Logic 3 Board for Elec. Mech. Systems

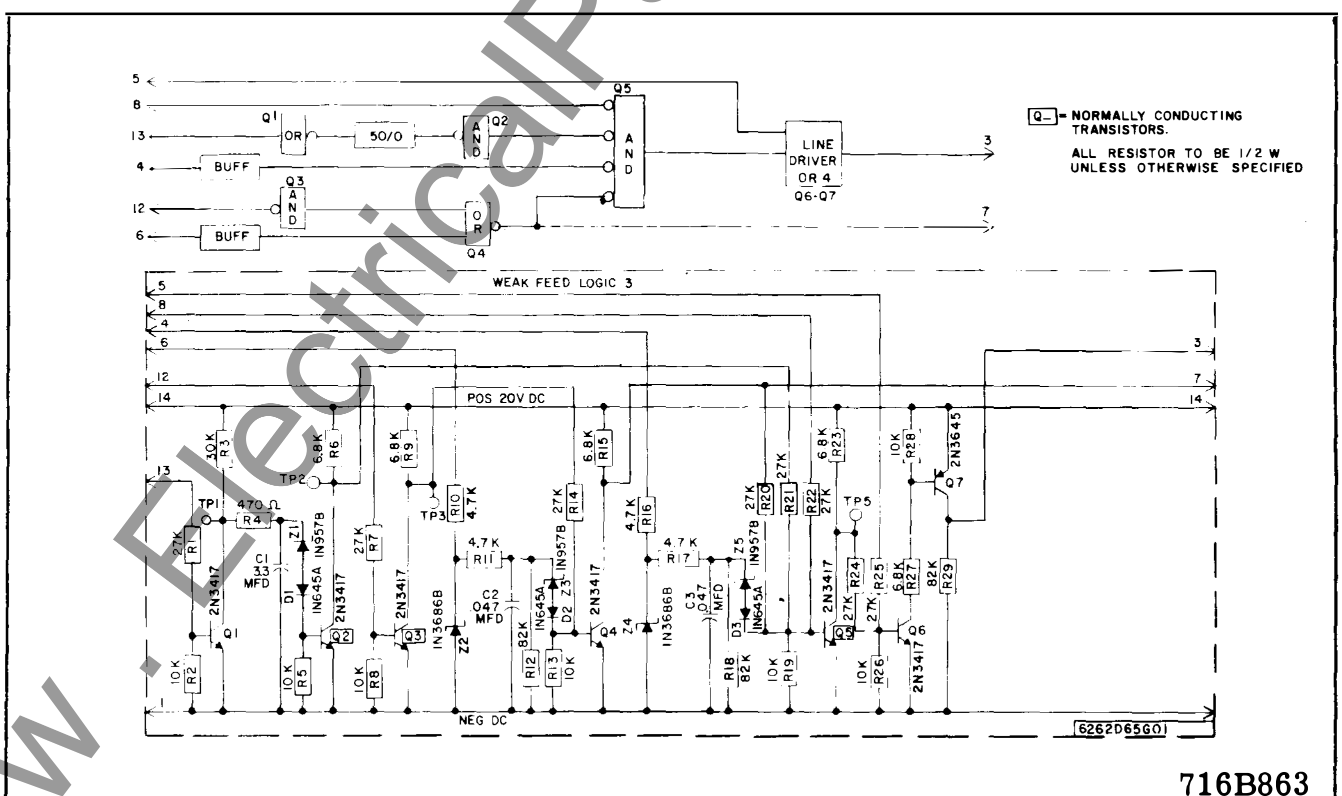


Fig. 17 Internal Schematic — Weak Feed Logic 3 Board for Solid State Systems

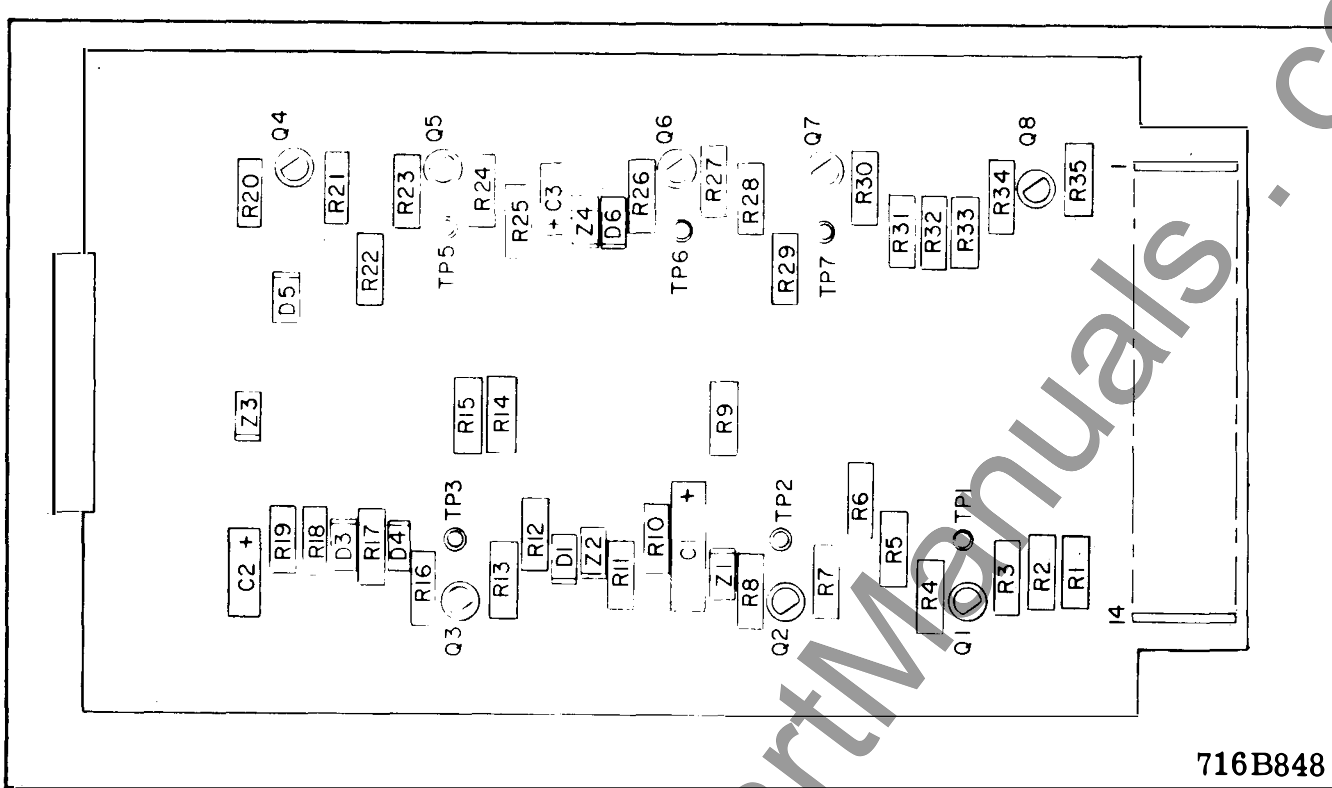


Fig. 18 Component Location – Weak Feed Logic 4 Board

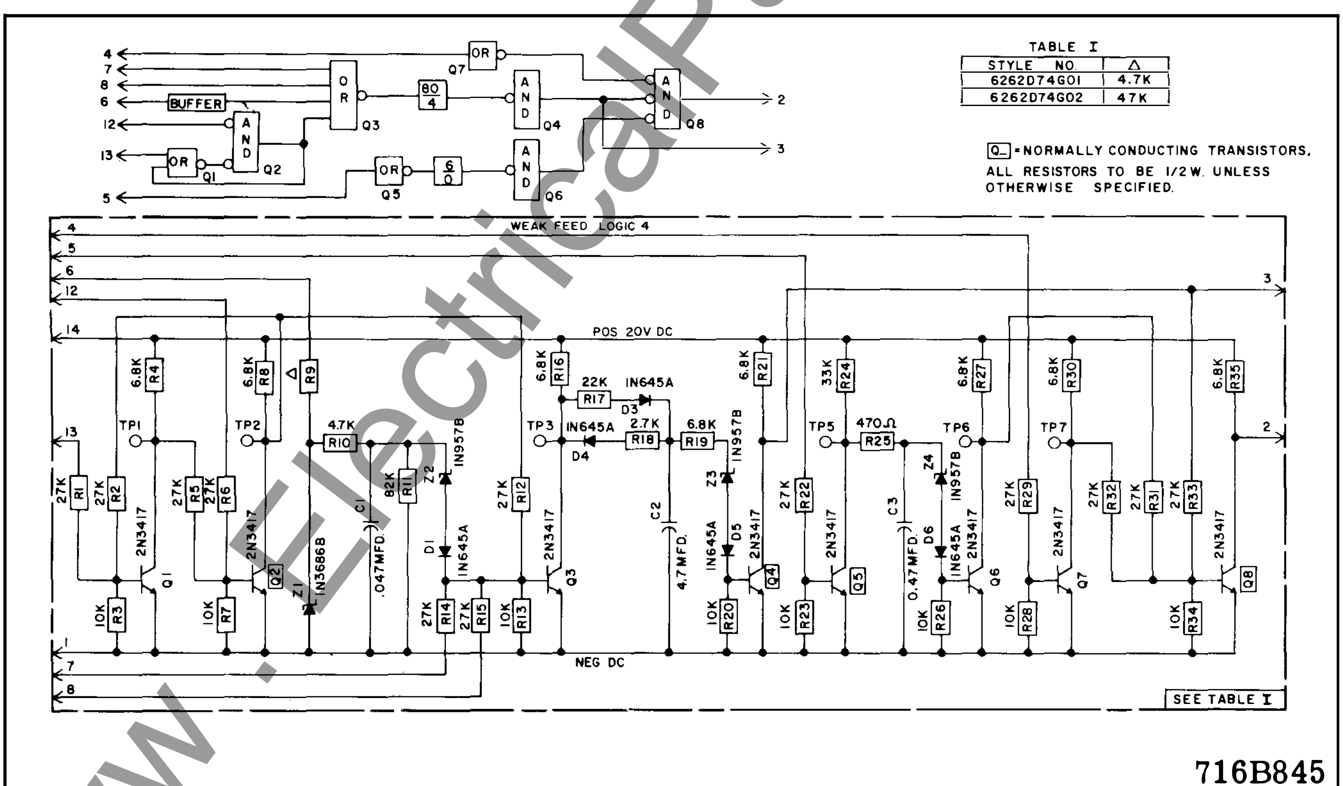


Fig. 19 Internal Schematic – Weak Feed Logic 4 Board

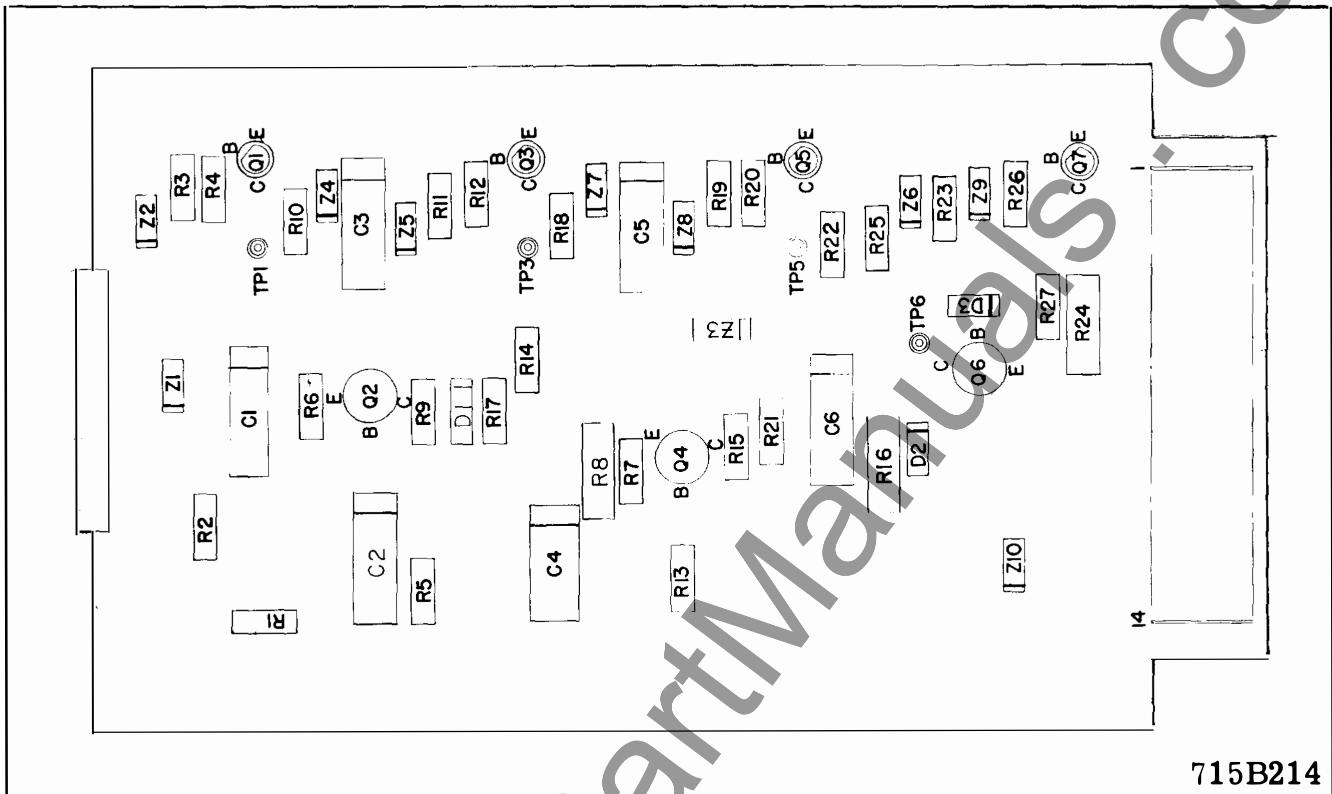

715B214

Fig. 20 Component Location Channel Interface Board

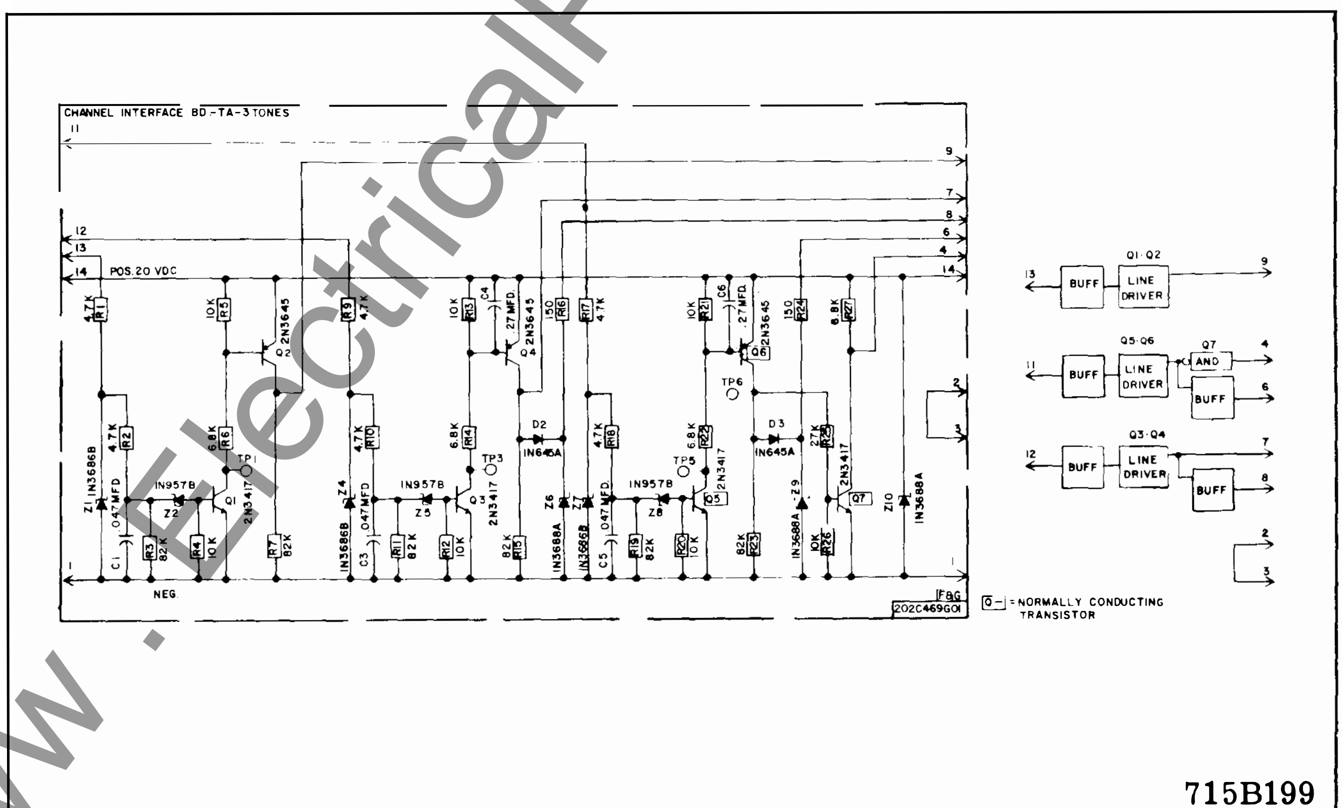

715B199

Fig. 21 Internal Schematic Channel Interface Board for TA-3 Tone

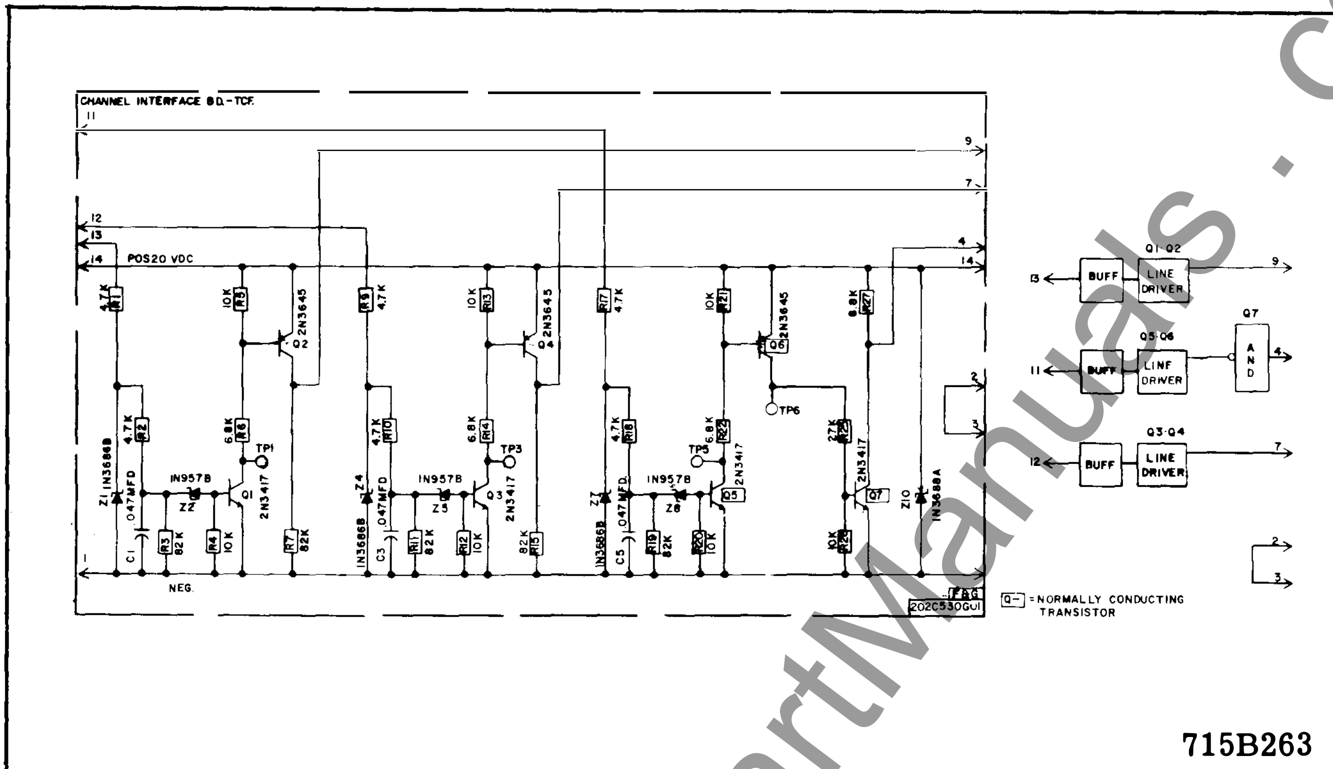


Fig. 22 Internal Schematic Channel Interface Board for TCF Carrier

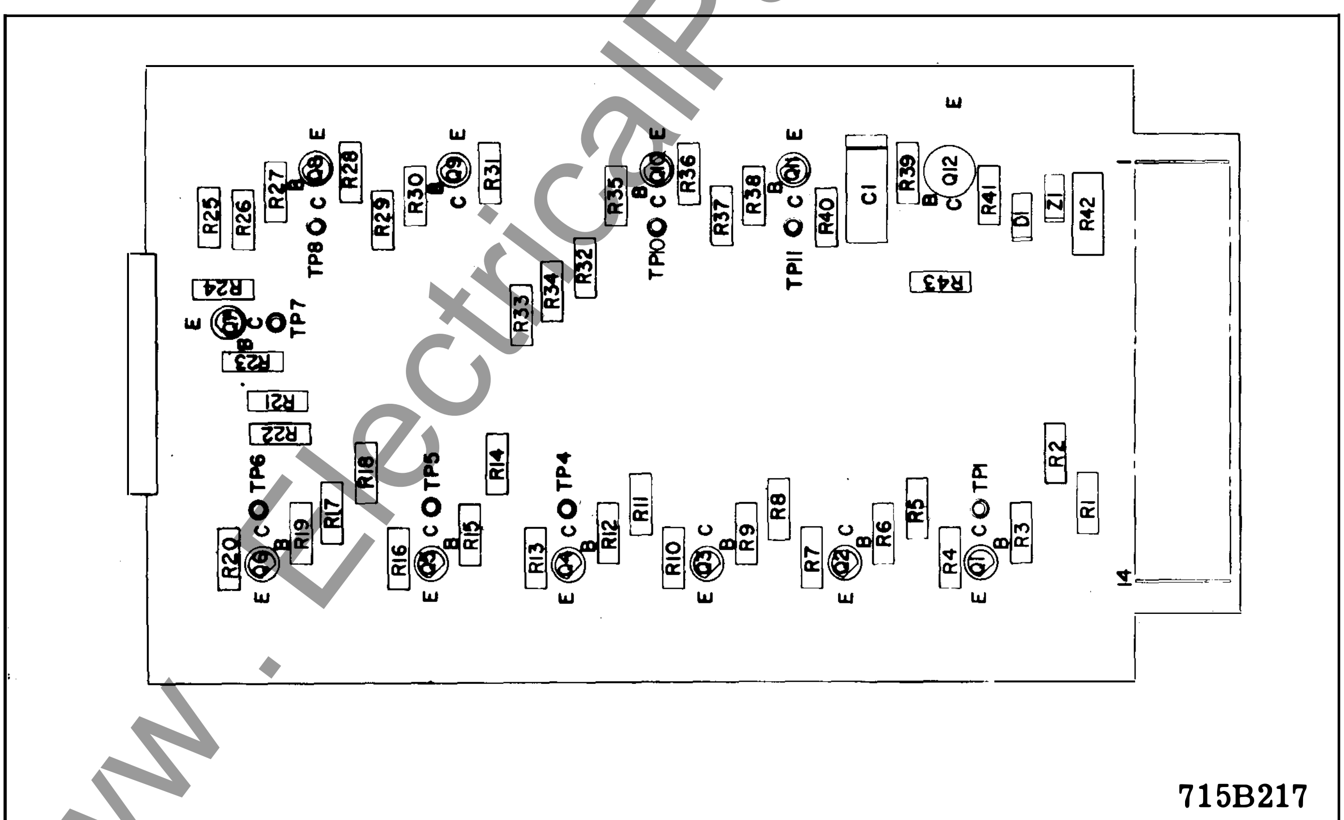


Fig. 23 Component Location Channel Trip Board

state, not "1". When a low signal clamp operation ("1" to "0") is received from the tone channel, then the 150/100 MS timer picks up and applies a "1" signal to one input of each of the two guard AND's on the CHANNEL TRIP BD. Now, if either or both receiver trip signals are "1" or become a "1" within the 100 millisecond dropout time of the 150/100 MS timer, then a "1" output will be produced at the output of the guard return AND and the OR it works into. Terminal 5 of the CHANNEL TRIP BD. will become a "1" and hold the 150/100 MS timer picked up by applying a "1" input to the 3 input loss of channel OR on the CHANNEL SUPERVISION BD. By inspecting the logic it can be seen that both receiver trip signals (one for two terminal applications) must return to guard, logic "0" to, make the channel operative after a loss of channel condition.

8. Channel Checkback Test

A. TCF frequency shift carrier channel
Refer to logic drawings, Fig. 4 and 5. Information in this section does not cover the the complete test, but only that portion concerning the STU-12 relays.

At the local terminal, the carrier transmitter will be disconnected from the line thus causing a loss of channel condition at the remote terminal. This will cause the loss of channel OR on the CHANNEL SUPERVISION BD. (Remote Terminal) to assume a "1", and satisfy the two input AND (preceding the 2500/2500 MS timer) and in 2500 milliseconds pickup the 2500/2500 MS timer on the CHECKBACK BD. The "1" output of the 2500/2500 MS timer will satisfy one input of the AND following it. Next, a test switch will be operated at the local terminal and the following will happen: a protective relay signal (for example, 21P) will be simulated, the transmitter will be reconnected to the line to restore the channel, and the local transmitter will be keyed to the trip frequency. At the remote terminal the TCF receiver logic will not give a trip output since the channel was not restored to the guard frequency. However, there will be a "1" signal obtained from the CHECK TRIP output of the receiver. This check trip output will satisfy the other input to the AND on the CHECKBACK BD. causing the transmitter to be keyed to the trip frequency. Since the check trip signal also applies a "1" input to the negated input of the AND energizing the 2500/2500 MS timer, it will no longer be satisfied and the timer will dropout causing keying to stop in 2.5 seconds. However, within the 2.5 seconds of keying, the STU-12 relay at the local terminal will trip because of reception of both a received trip signal and a simulated protective relay signal.

b. Frequency shift tone channel
Refer to logic drawings, Fig. 6 and 7
Information in this section does not cover the complete test, but only that portion concerning the STU-12 relay.

At the local terminal, the tone transmitter will be disconnected from the line thus causing a loss of channel condition at the remote terminal. This will cause the loss of channel OR on the CHANNEL SUPERVISION BD. (remote terminal) to assure a "1" output to pickup the 150/100 MS timer. This satisfies the two input AND on the Check Back Bd. and in 2500 milliseconds the 2500/2500 MS timer will pick up. The "1" output of the 2500/2500 MS timer will satisfy one input of the AND following it. Next, a test switch will be operated at the local terminal and the following will happen: a protective relay signal (for example, 21P) will be simulated, the transmitter will be reconnected to the line to restore the channel, and the local transmitter will be keyed to trip frequency. At the remote terminal, the tone receiver trip signal will be a "1" thus causing the three input AND on the CHANNEL SUPERVISION BD. to operate and produce a "1" at terminal 3 of this board. This "1" will satisfy the other input to the AND on the CHECKBACK BD. causing the transmitter to be keyed to the trip frequency. Since at the same time, the input to the 2500/2500 MS timer is lost, then the keying signal to local terminal will only last 2.5 seconds. However, within this time of keying, the STU-12 relay will trip because of the reception of both a received trip signal and a simulated protective relay signal.

9. Electromechanical Systems

When the STU-12 relay is used with electromechanical protective relays, two contact bounce circuits are used. The contact bounce circuit will produce a logic "1" output immediately upon reception of an input logic "1" signal. This output will last for approximately 20 milliseconds. The contact bounce circuits on the W.F. Logic 1 and 3 boards permit transmitter keying and an input to set up tripping respectively. These circuits prevent additional delay in tripping due to a bouncing elecmech protective relay contact.

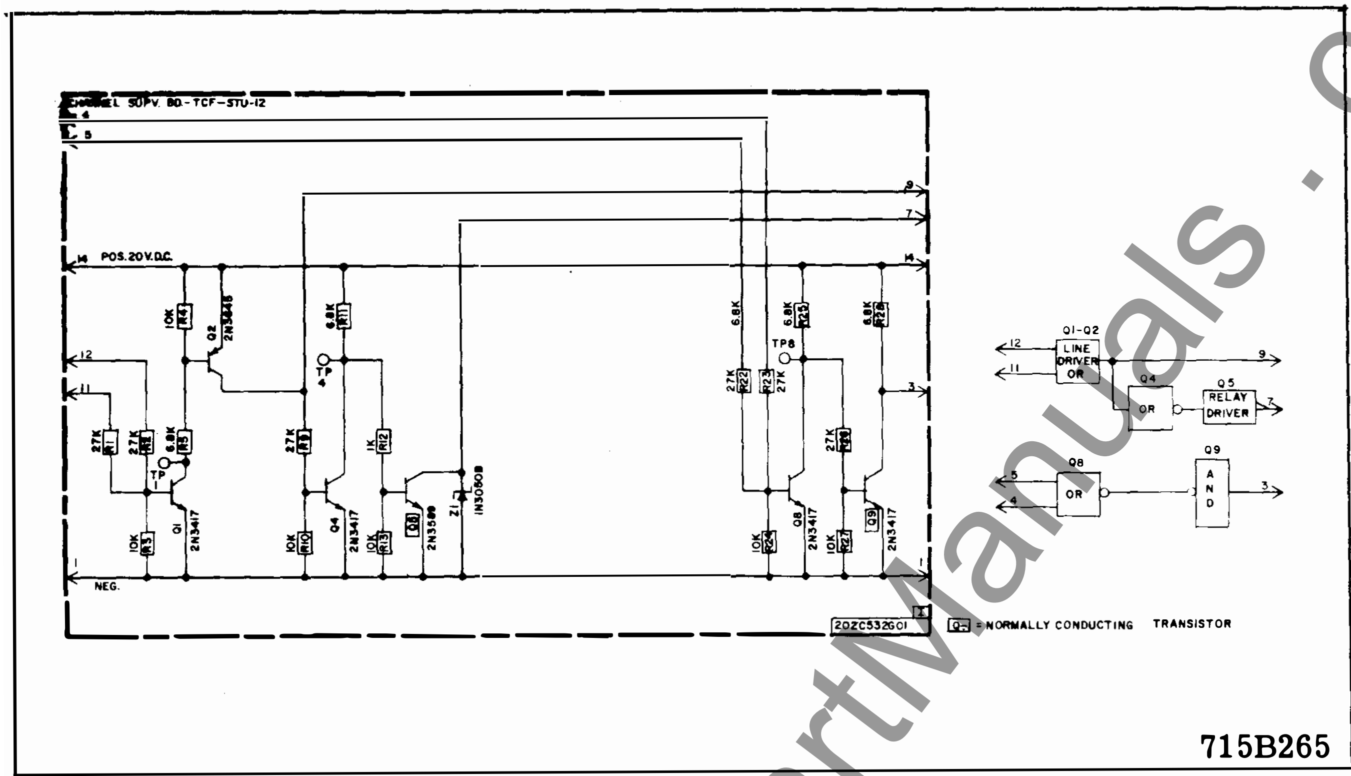


Fig. 30 Internal Schematic Channel Supervision Board for TCF Channel

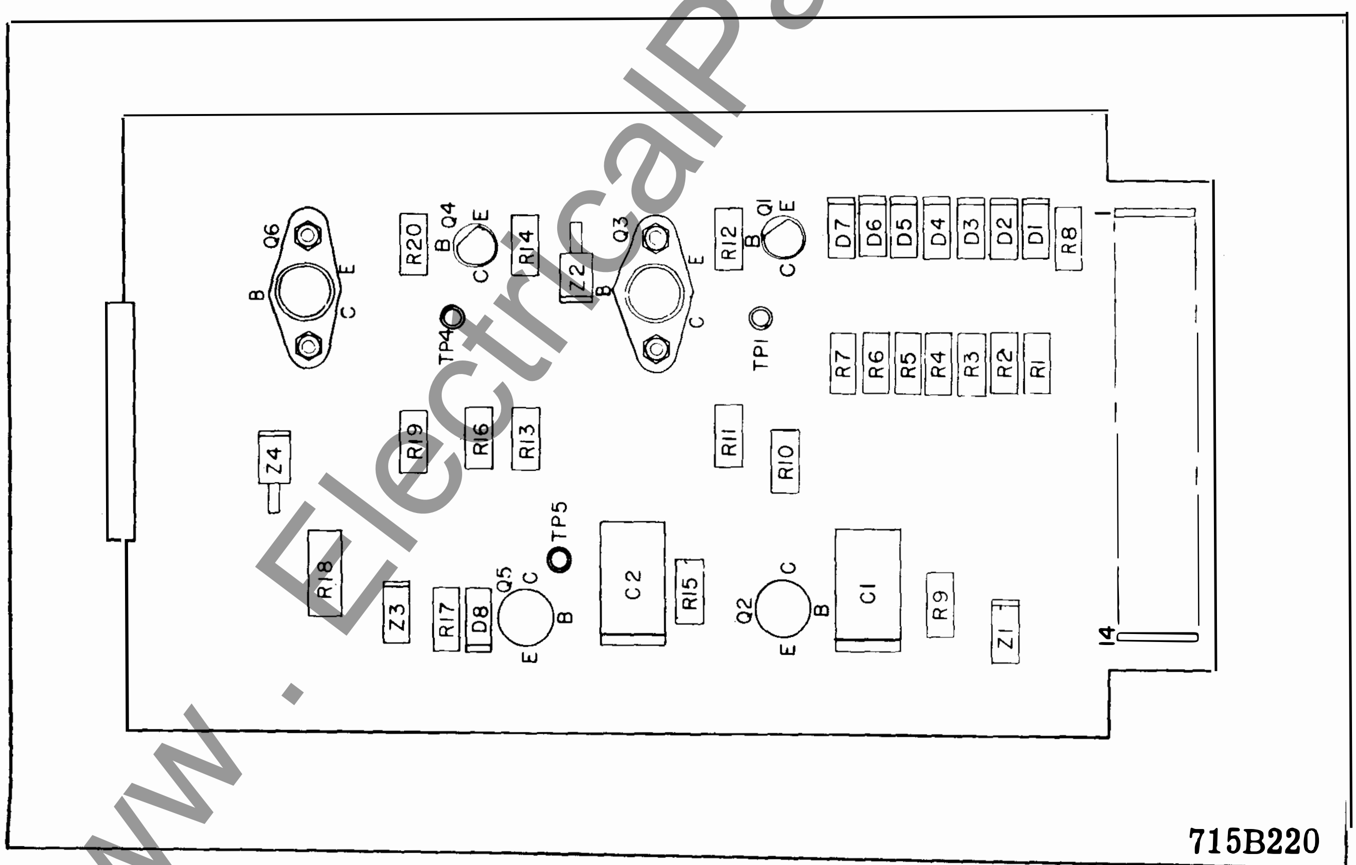


Fig. 31 Component Location Transmitter Key Board

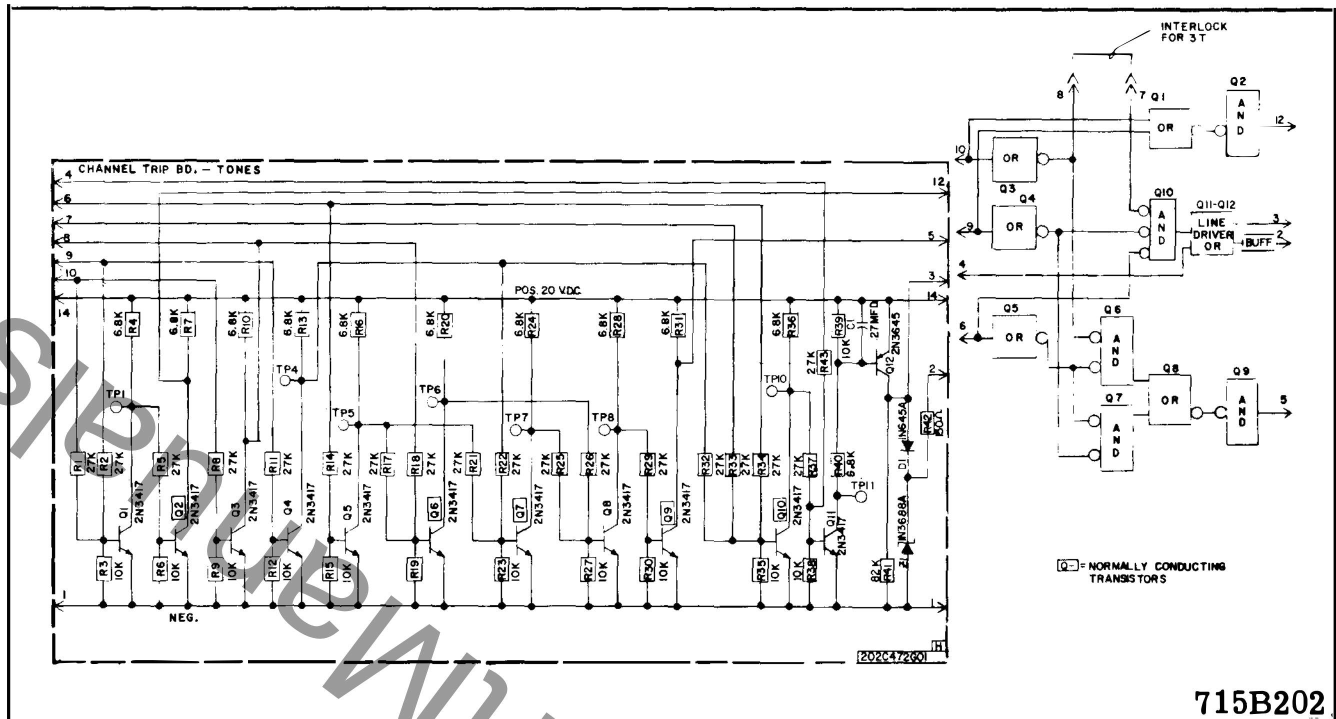


Fig. 24 Internal Schematic Channel Trip Board for Tones

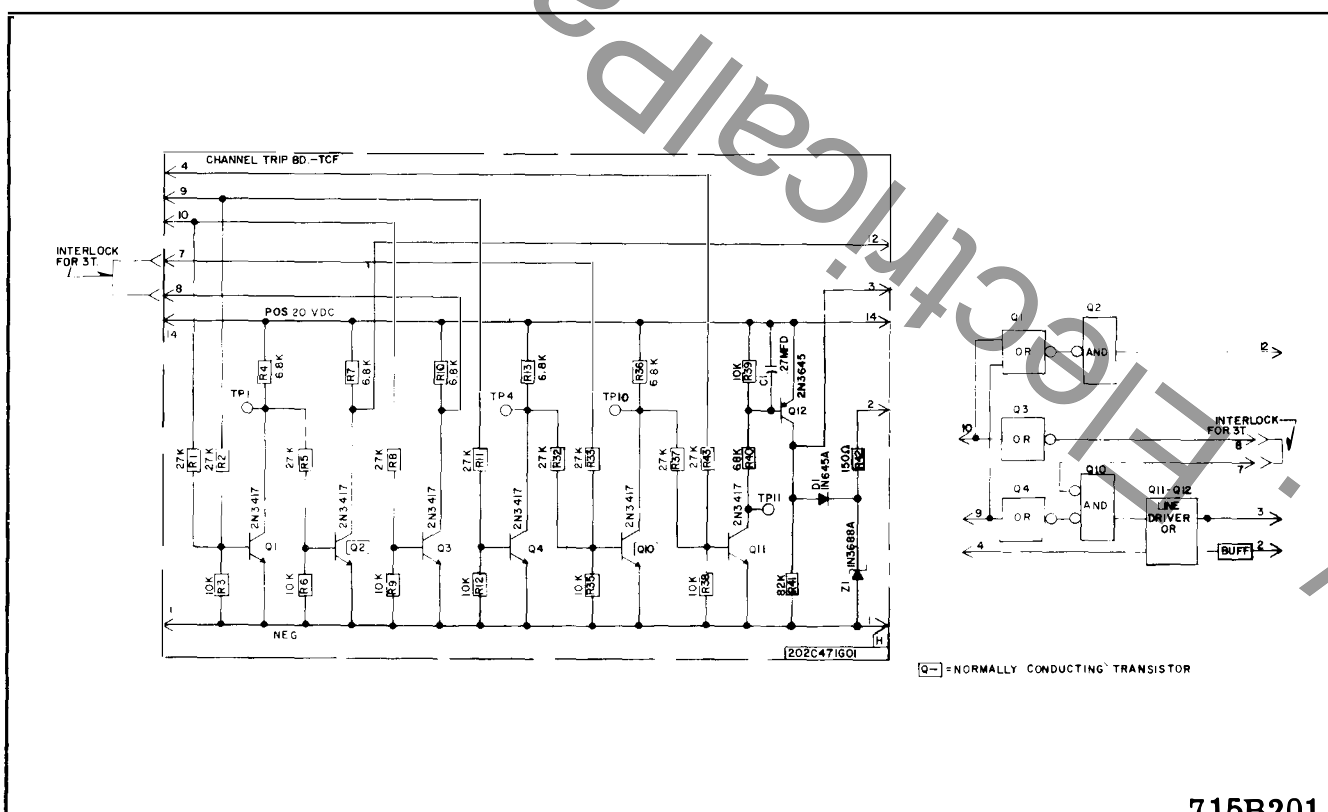


Fig. 25 Internal Schematic Channel Trip Board for TCF

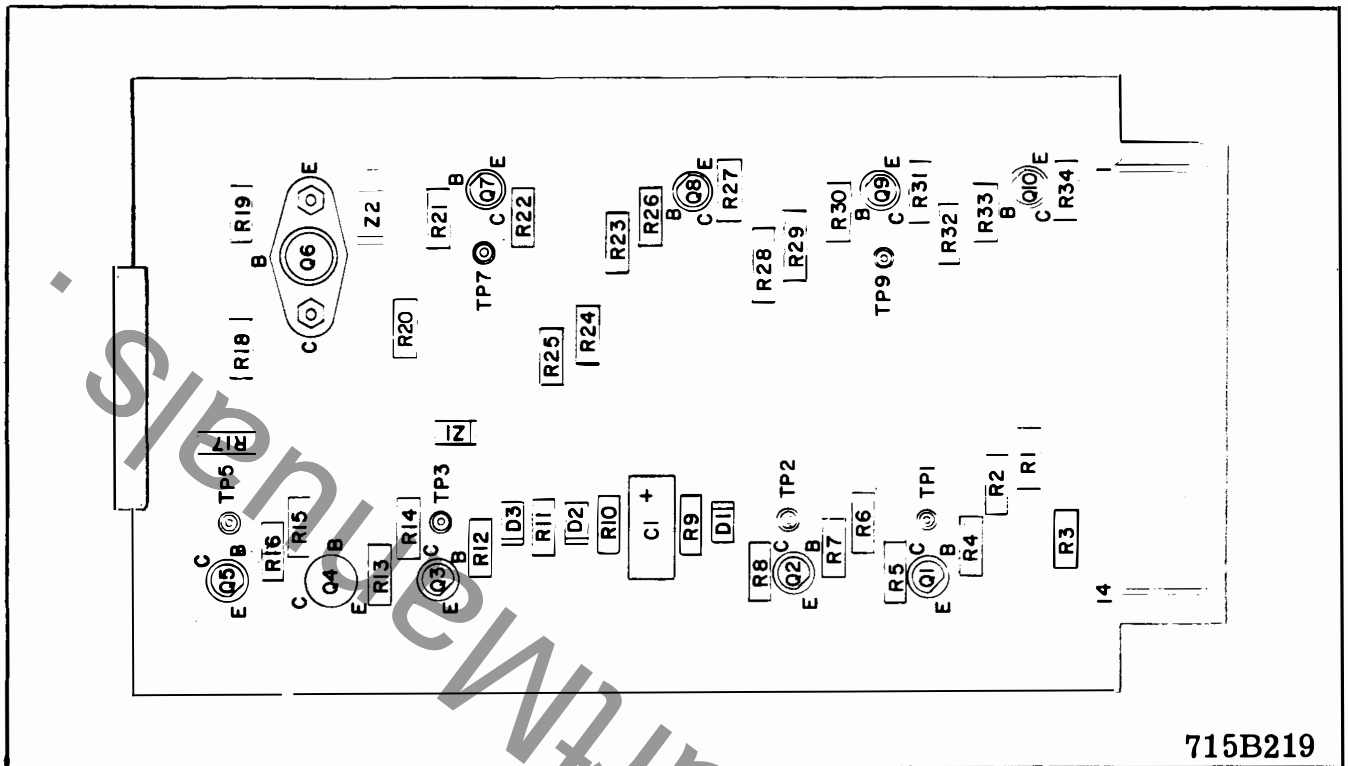


Fig. 26 Component Location Channel Supervision Board Tone Channel

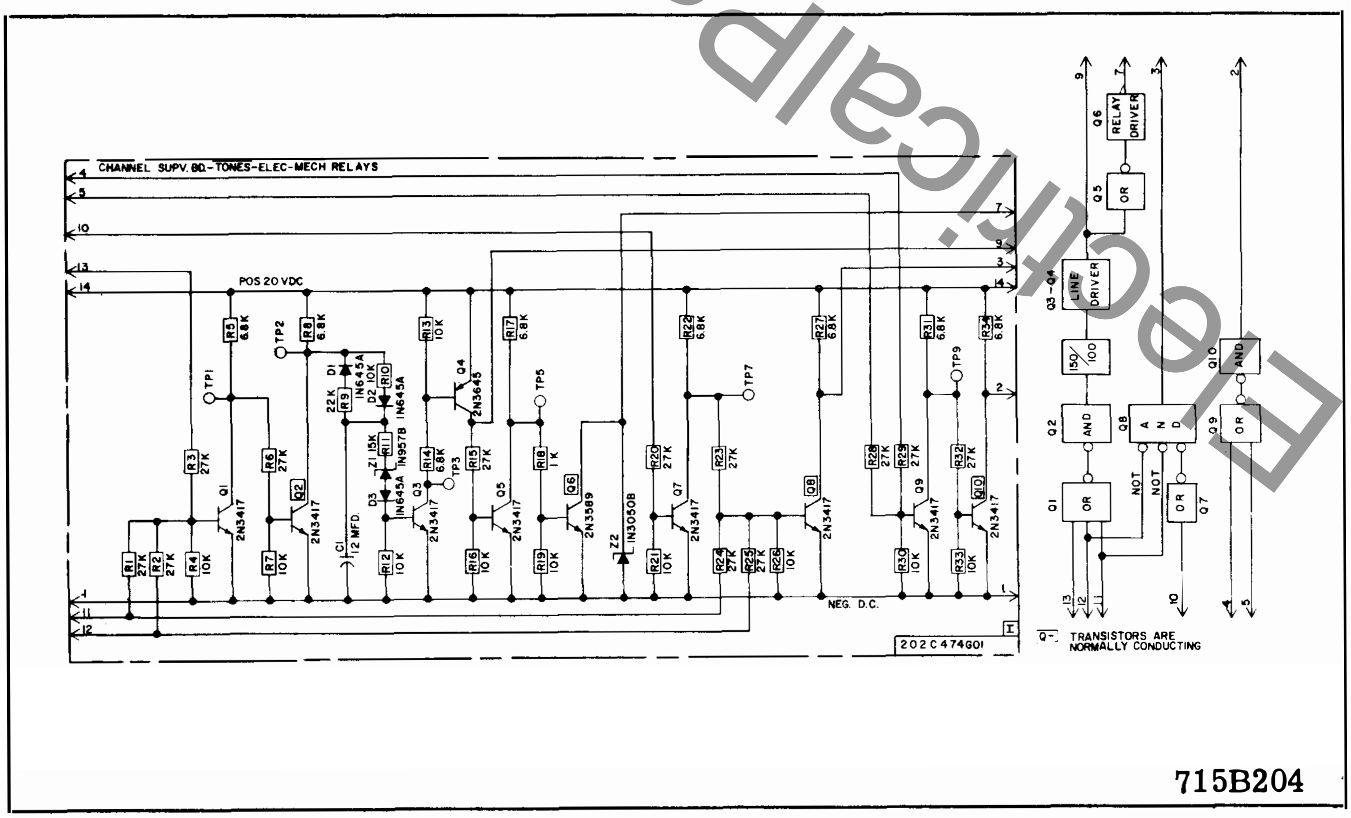
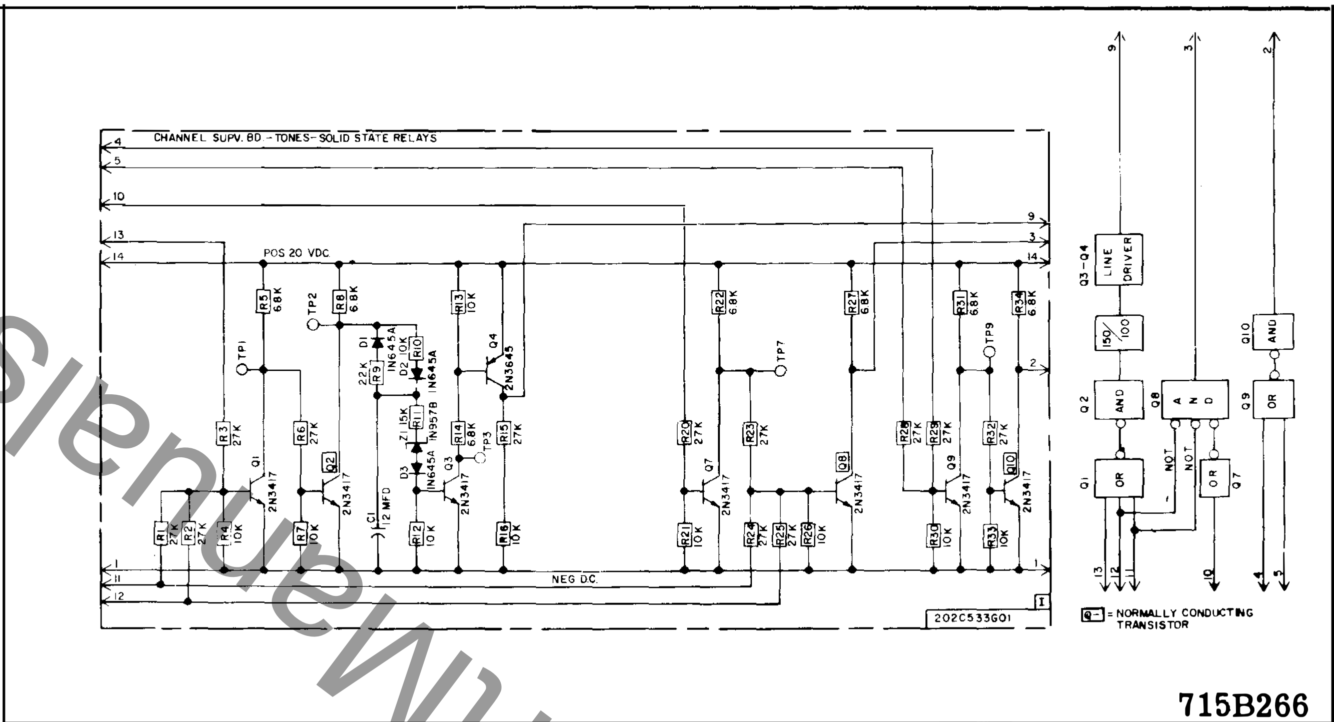
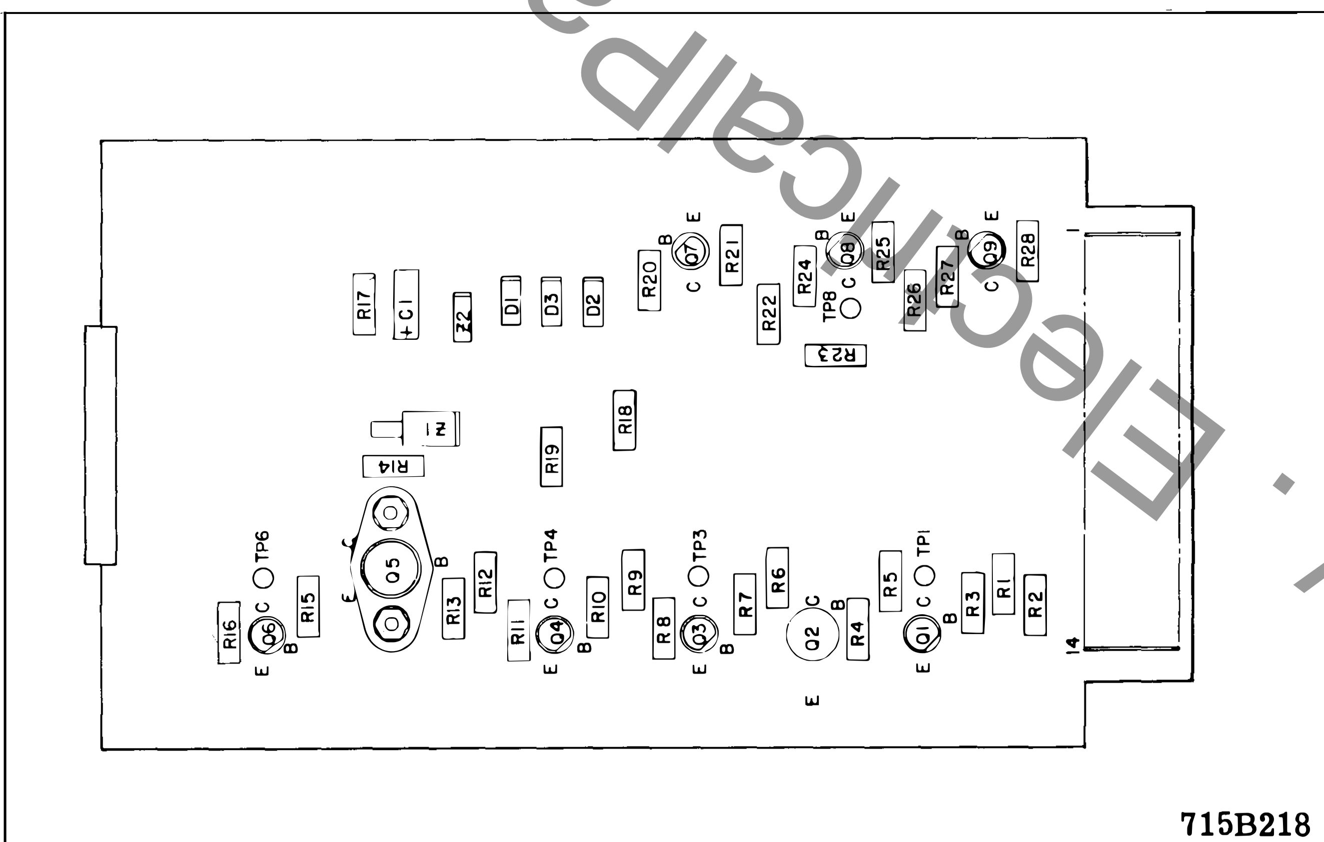


Fig. 27 Internal Schematic Channel Supervision Board for Tone Channel and Elec. Mech. System



715B266

Fig. 28 Internal Schematic Channel Supervision Board for Tone Channel and Solid State System



715B218

Fig. 29 Component Location Channel Supervision Board TCF Channel

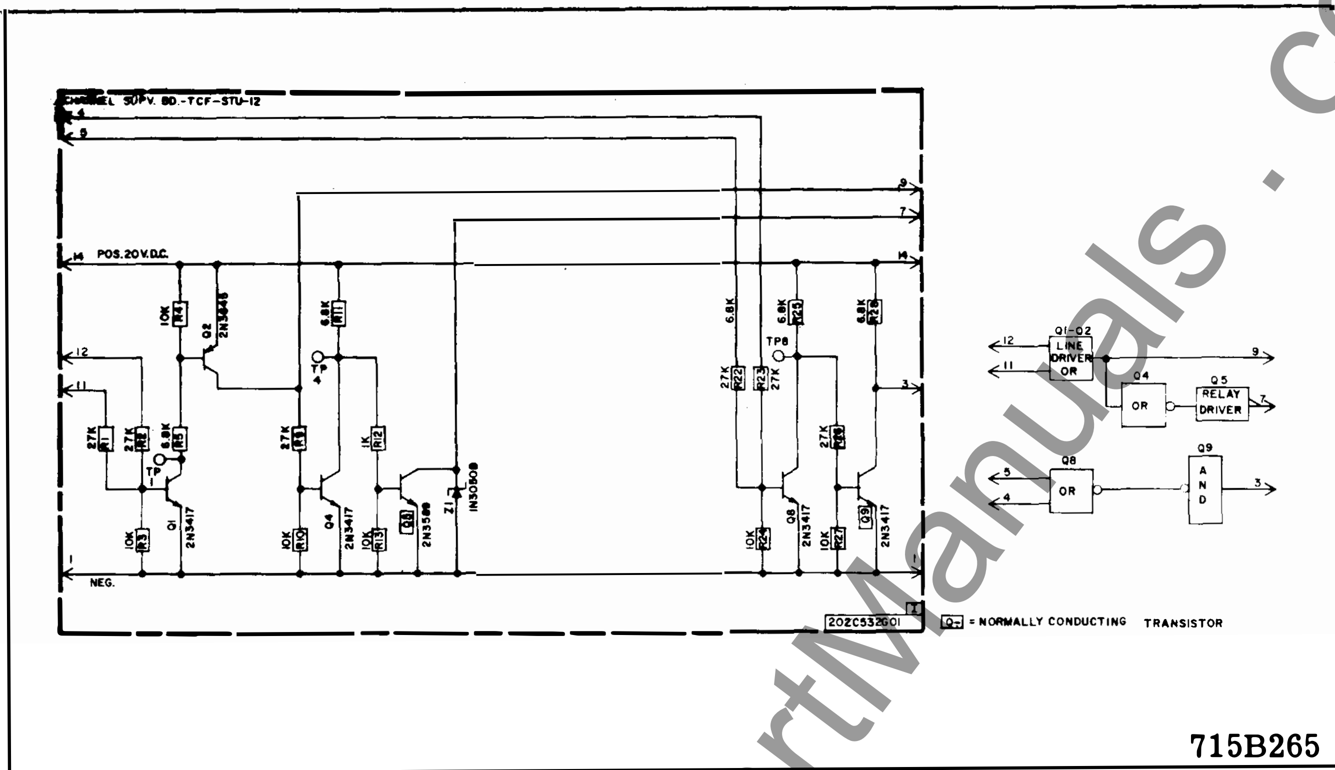


Fig. 30 Internal Schematic Channel Supervision Board for TCF Channel

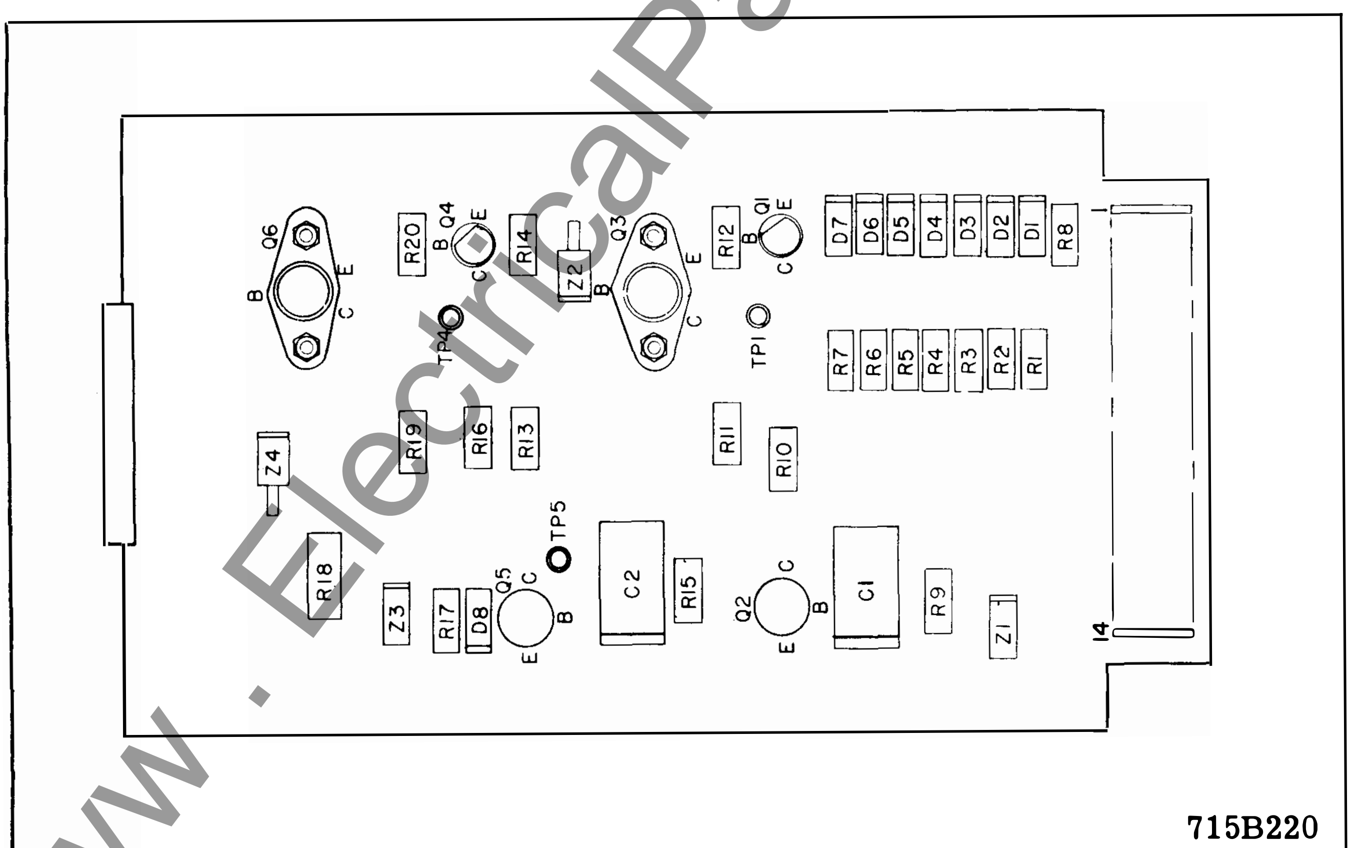


Fig. 31 Component Location Transmitter Key Board

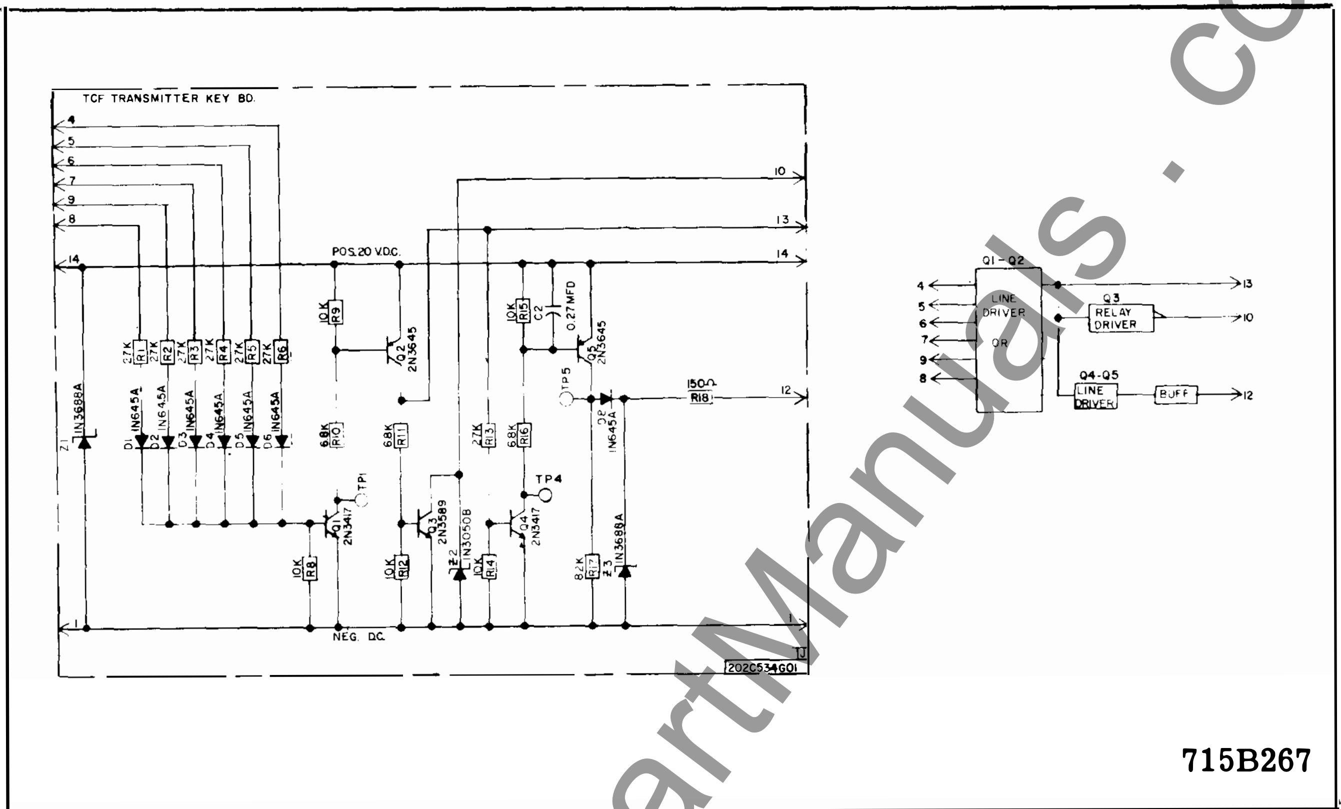


Fig. 32 Internal Schematic Transmitter Key Board for TCF Channel

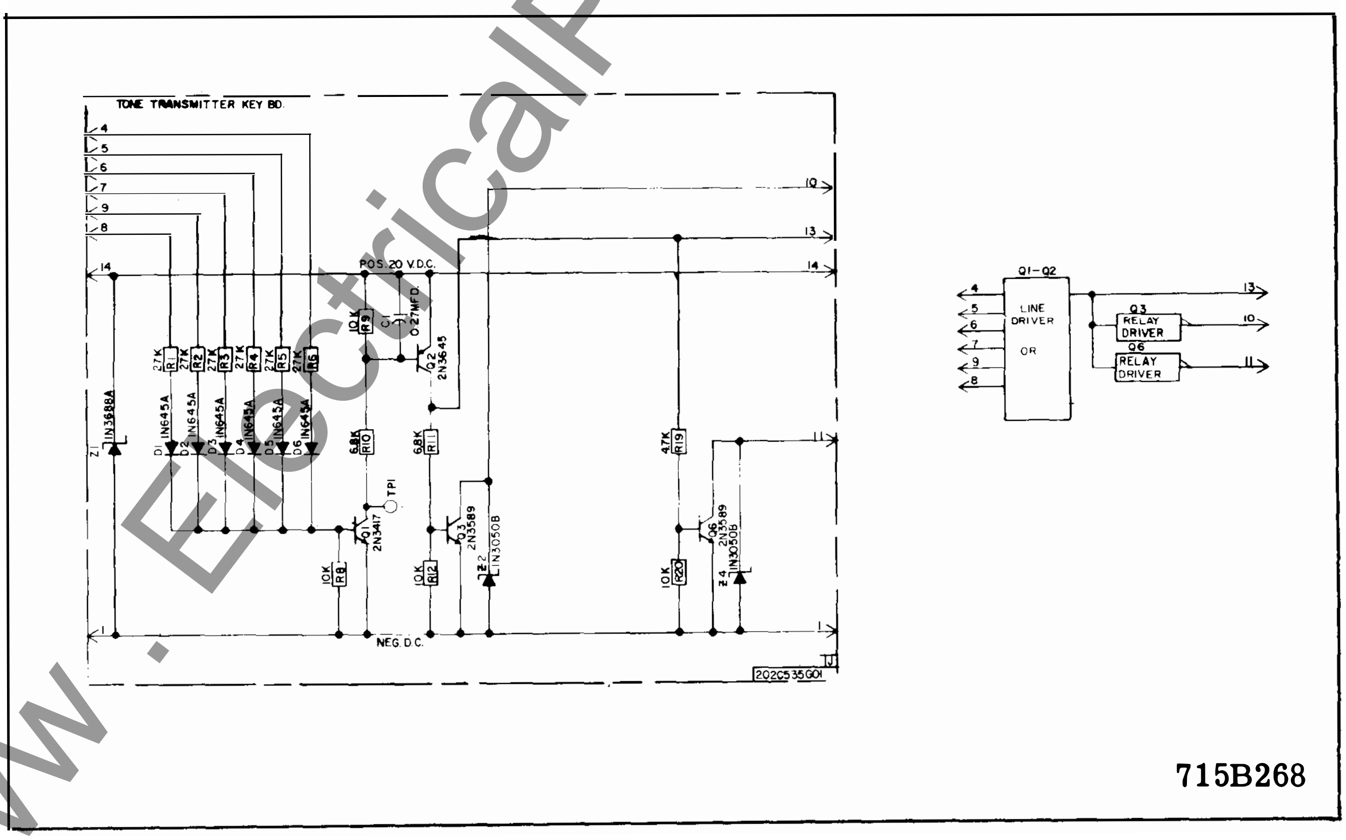


Fig. 33 Internal Schematic Transmitter Key Board for a Tone Channel

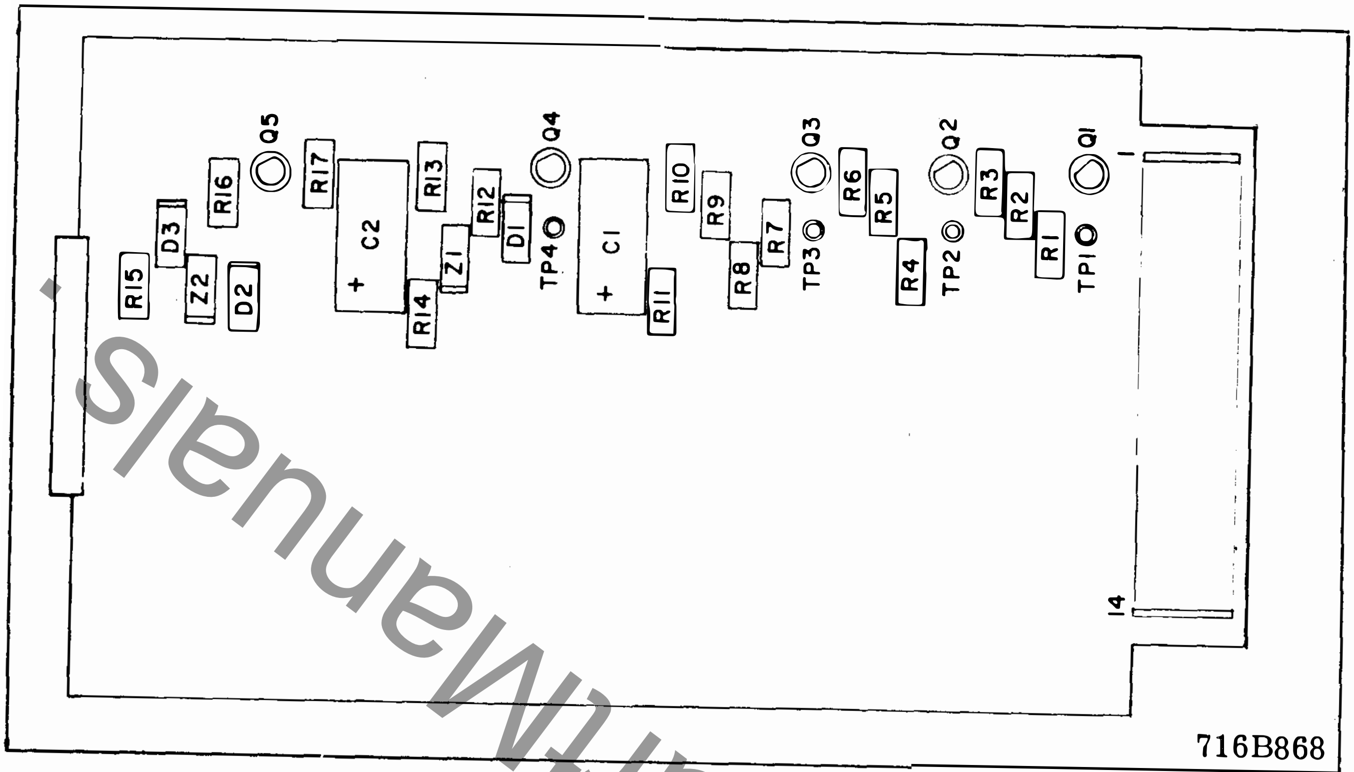


Fig. 34 Component Location Checkback Board

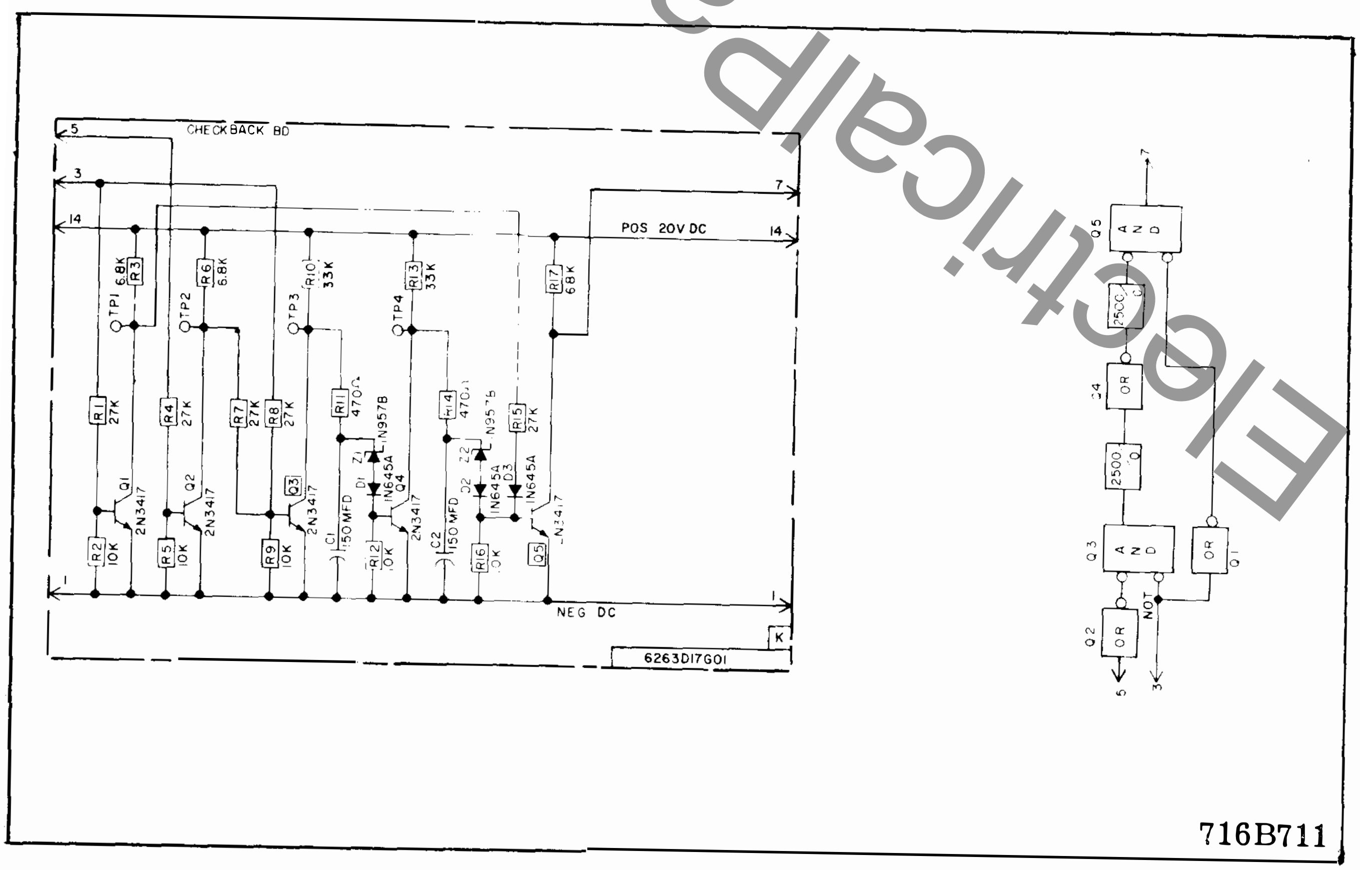


Fig. 35 Internal Schematic Checkback Board

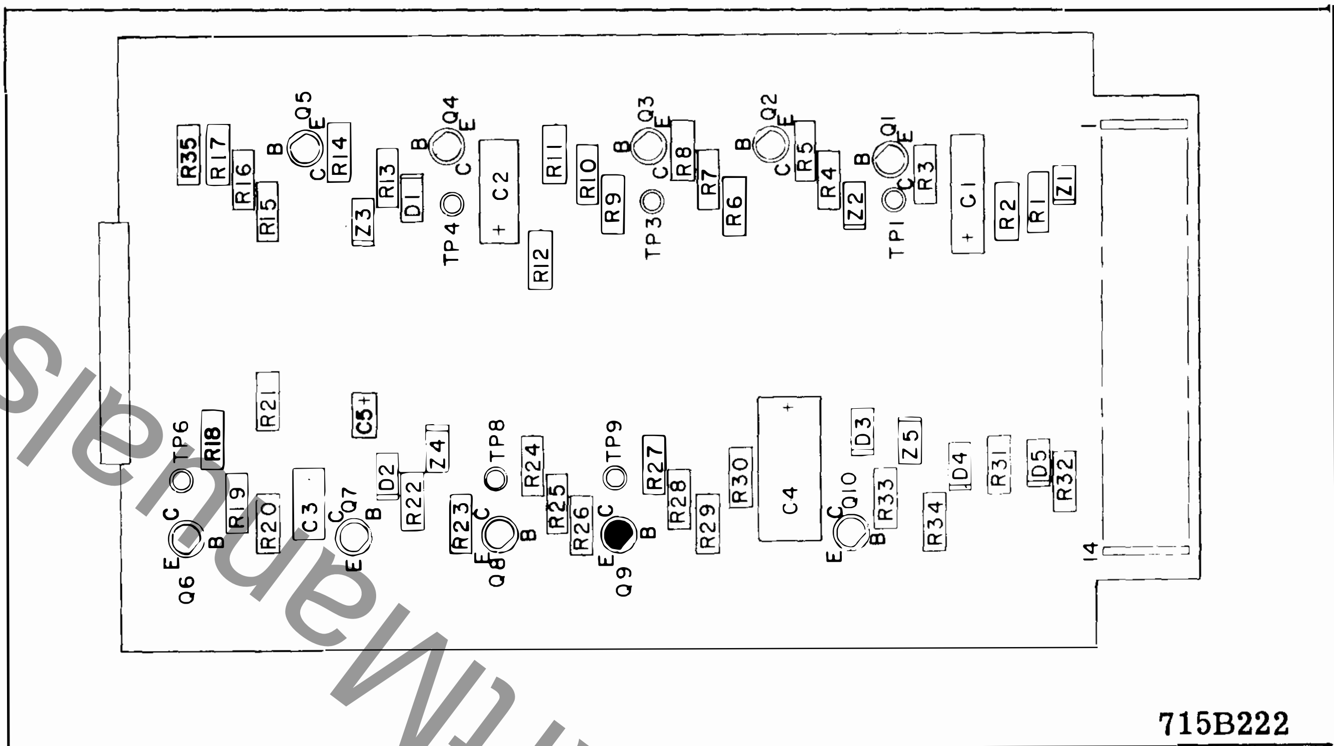


Fig. 36 Component Location Timing Board

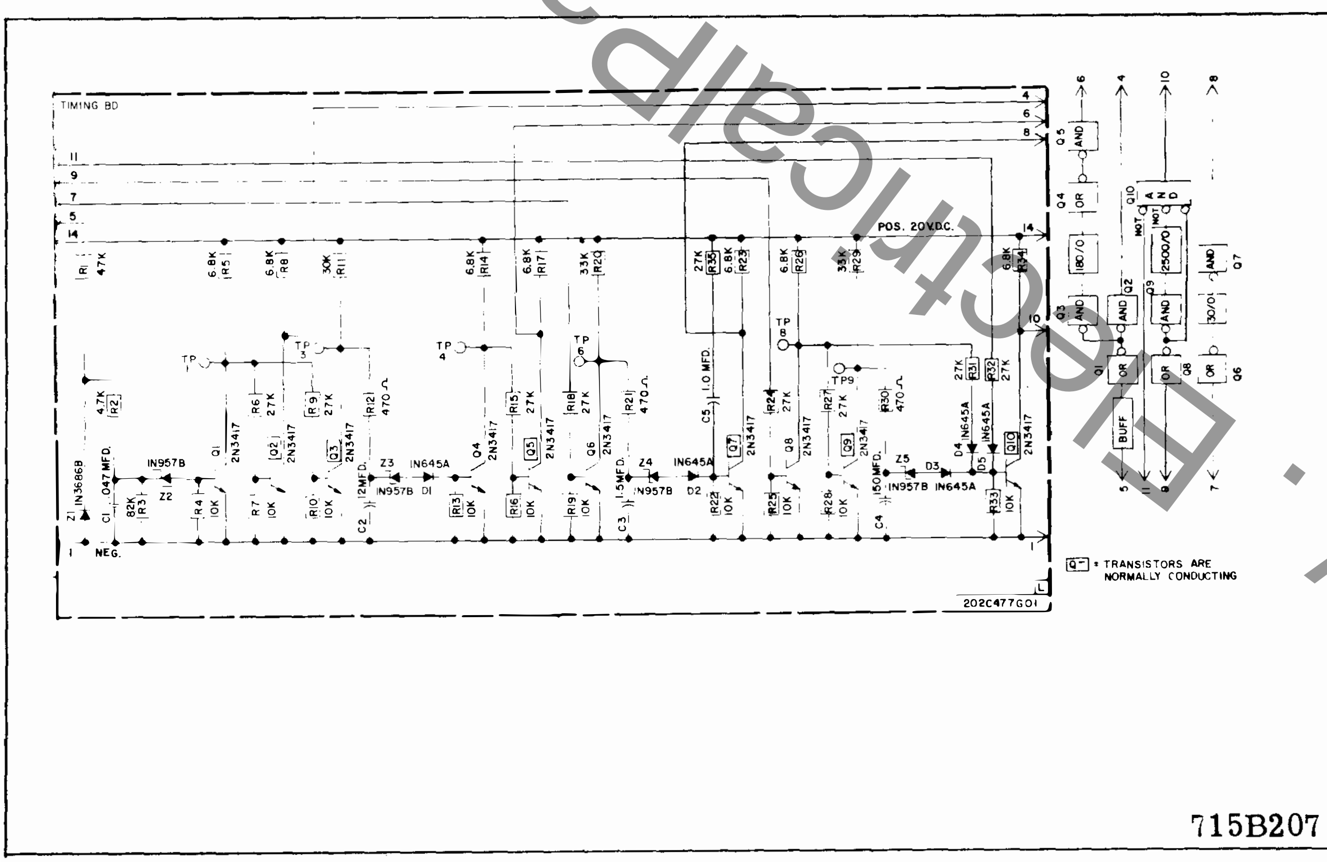


Fig. 37 Internal Schematic Timing Board

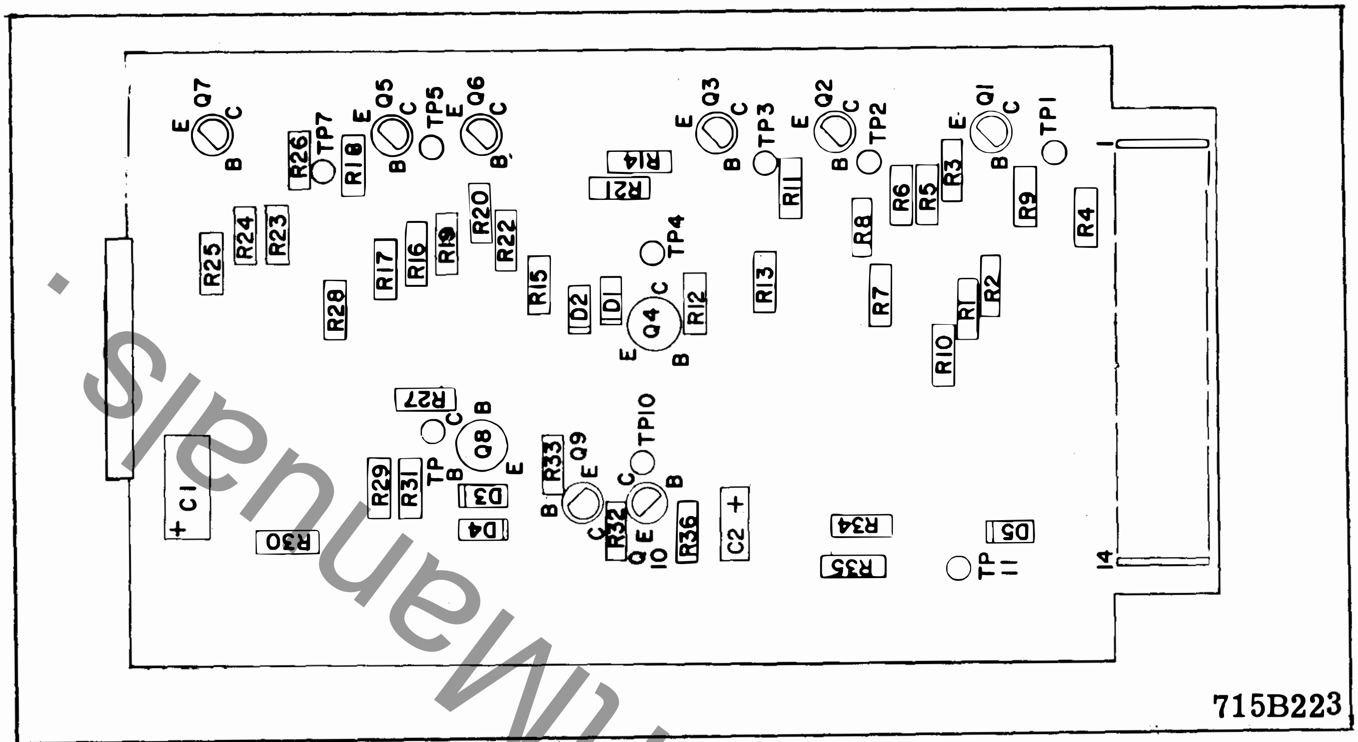


Fig. 38 Component Location Arming Board

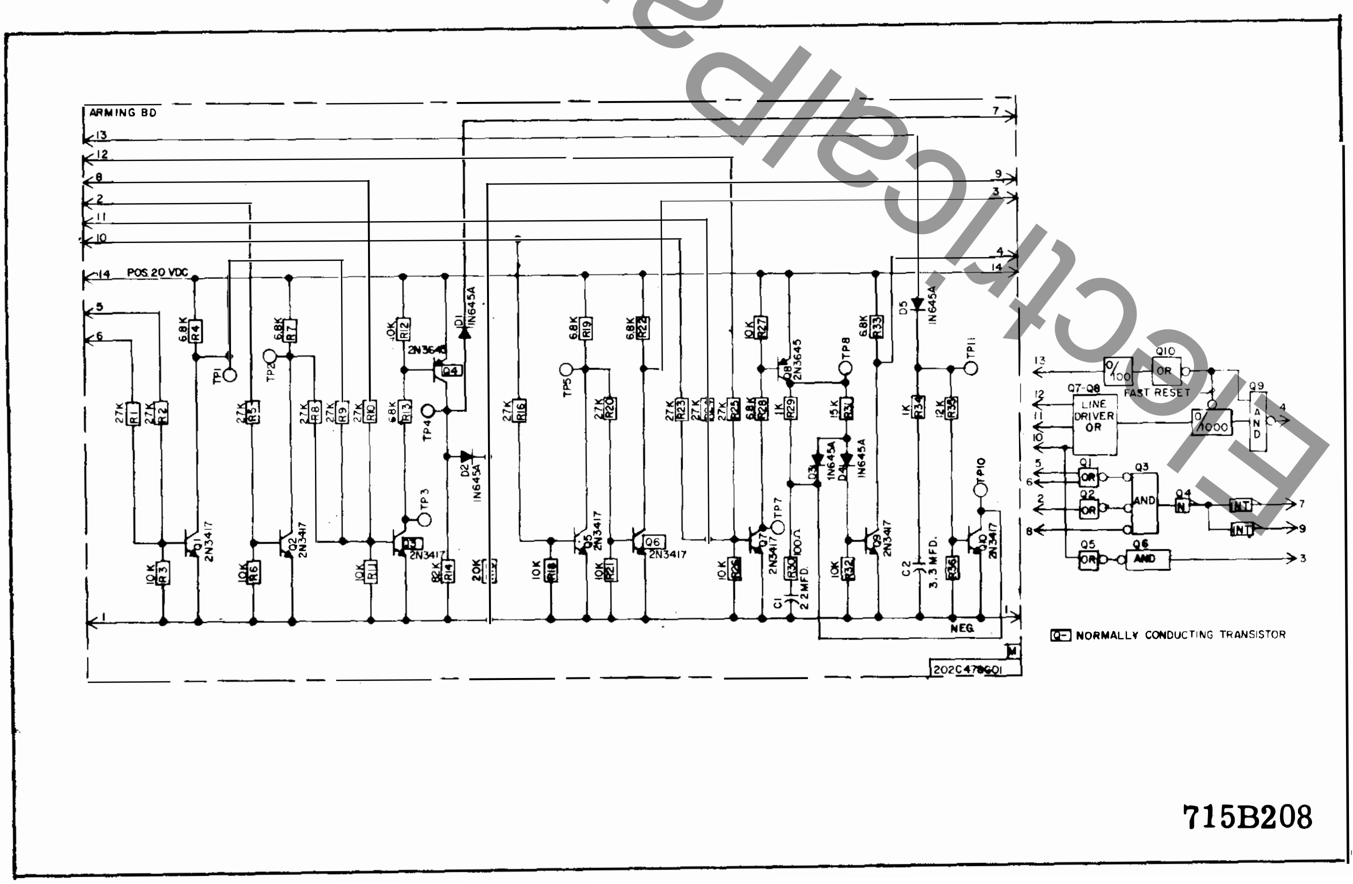
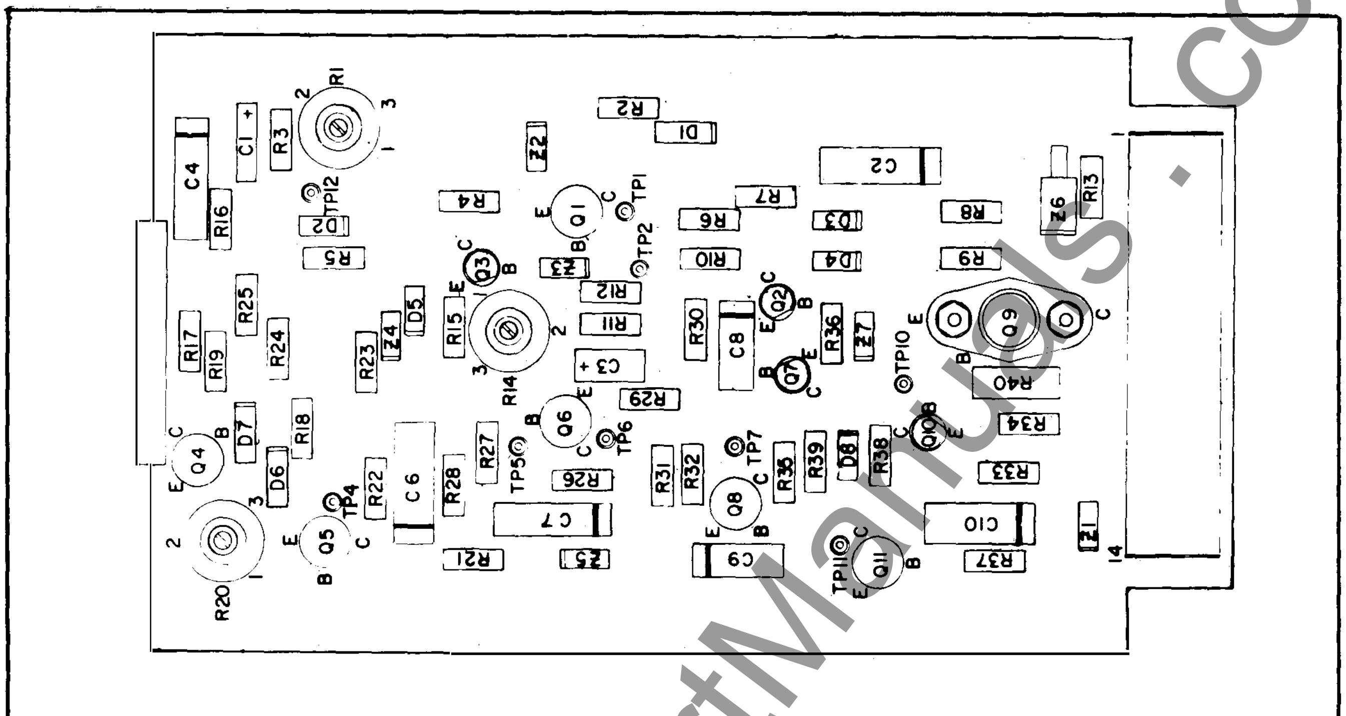


Fig. 39 Internal Schematic Arming Board



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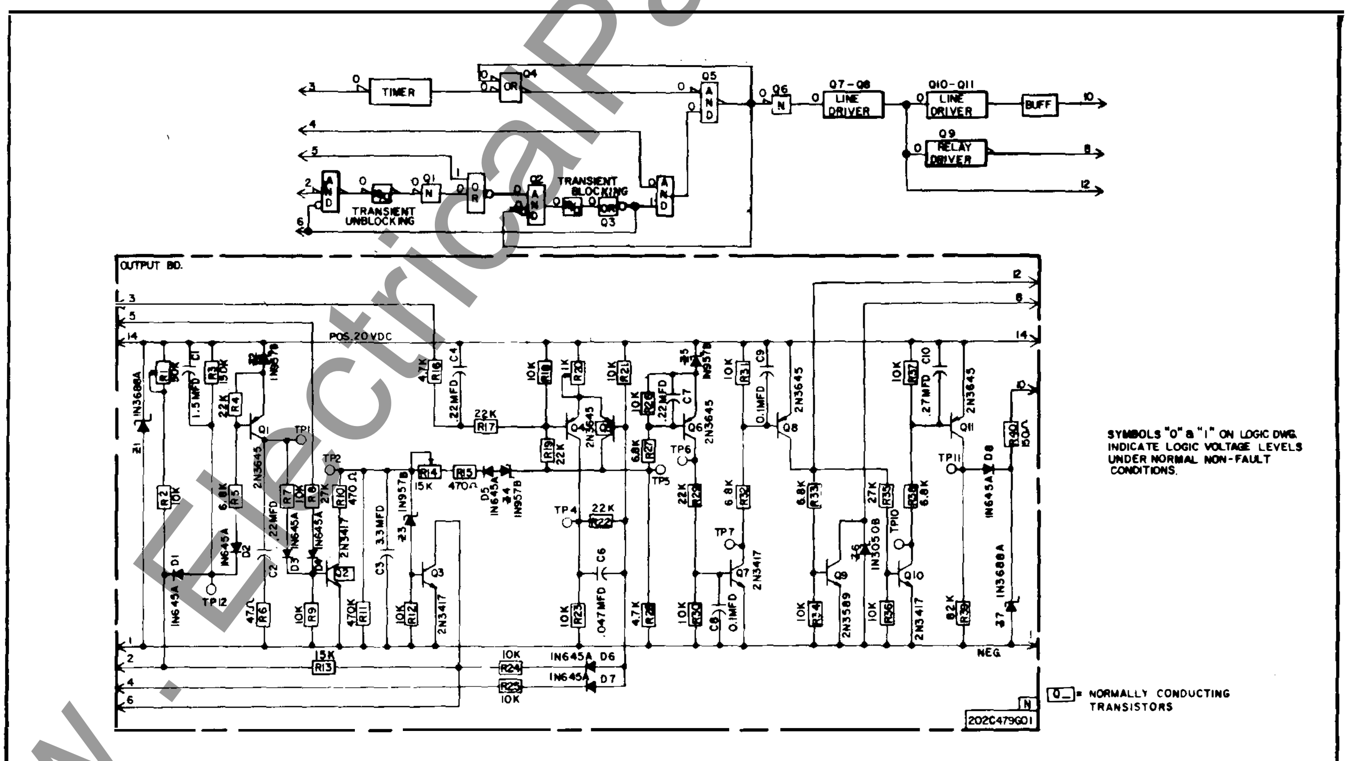
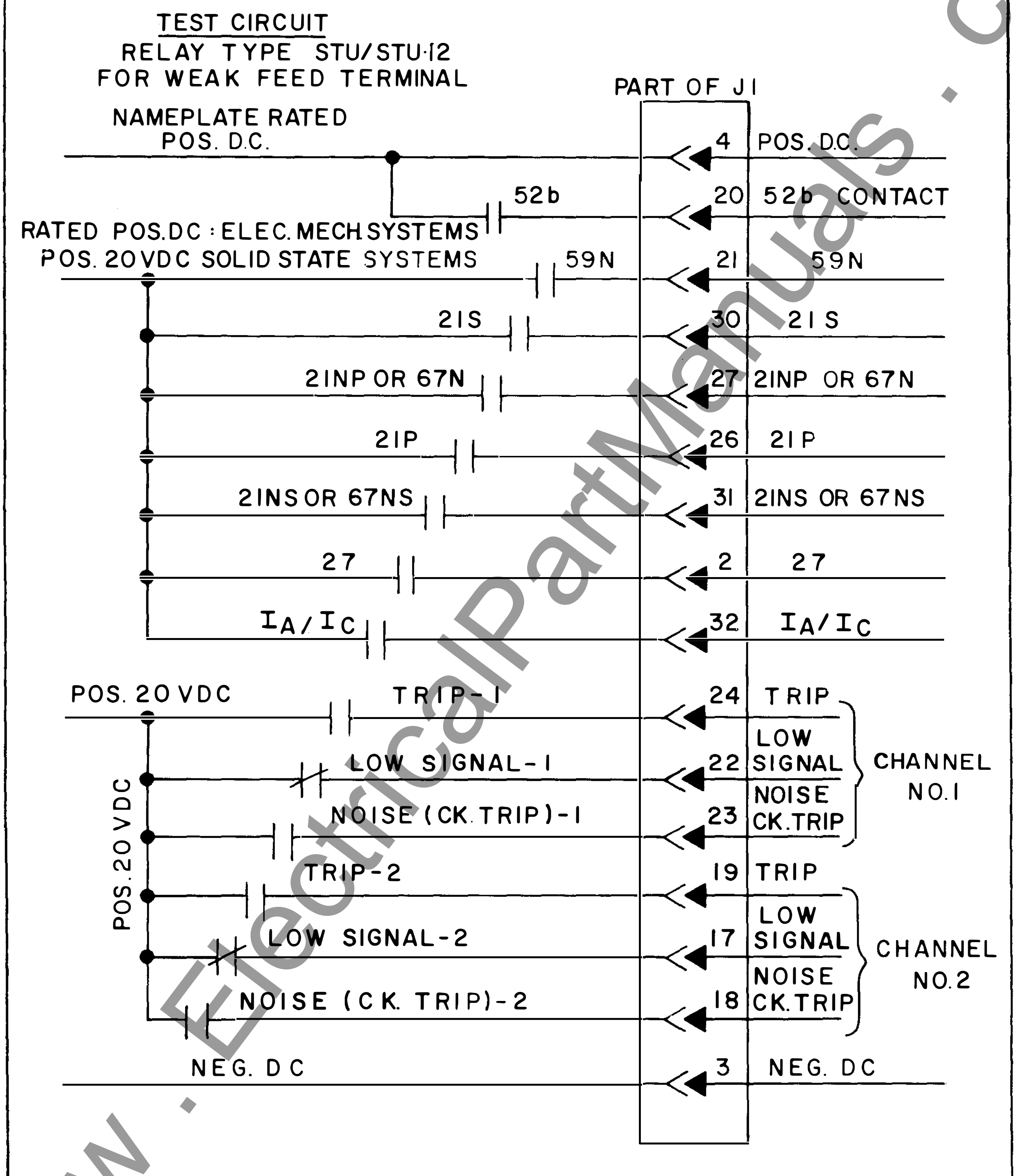
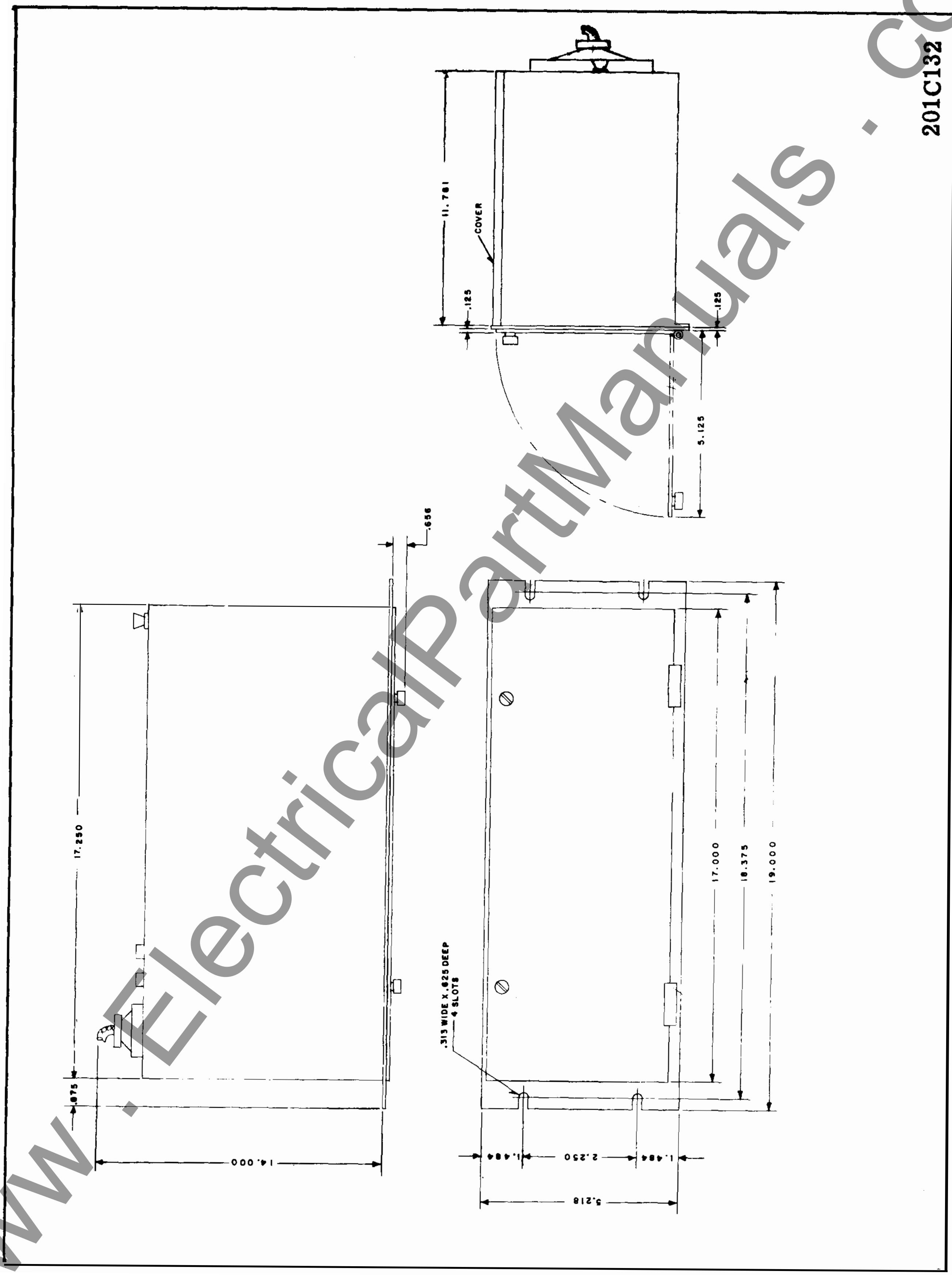


715B209


TEST CIRCUIT
RELAY TYPE STU/STU-12
FOR WEAK FEED TERMINAL
PART OF J1
NAMEPLATE RATED
POS. D.C.
4 POS. D.C.
52b
20 52b CONTACT
RATED POS.DC : ELEC. MECH SYSTEMS
POS. 20 VDC SOLID STATE SYSTEMS
59N
21 59N
21S
30 21S
21NP OR 67N
27 21NP OR 67N
21P
26 21P
21NS OR 67NS
31 21NS OR 67NS
27
2 27
IA/IC
32 IA/IC
POS. 20 VDC
TRIP-1
24 TRIP
LOW SIGNAL-1
22 LOW SIGNAL
NOISE (CK.TRIP)-1
23 NOISE CK.TRIP
CHANNEL NO.1
POS. 20 VDC
TRIP-2
19 TRIP
LOW SIGNAL-2
17 LOW SIGNAL
NOISE (CK. TRIP)-2
18 NOISE CK.TRIP
CHANNEL NO.2
NEG. DC
3 NEG. DC

878A366


201C132
11.781
COVER
.125
.125
5.125
.656
17.250
.875
14.000
17.000
18.375
19.000
.313 WIDE X .625 DEEP
4 SLOTS
1.484
2.250
1.484
5.218

WESTINGHOUSE ELECTRIC CORPORATION

RELAY-INSTRUMENT DIVISION **NEWARK, N. J.**

Printed in U.S.A.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE STU-12 TRANSFER TRIP RELAY

CAUTION: It is recommended that the user of this equipment become acquainted with the information in either these instructions or the systems instruction leaflet 40-205 before energizing this relay. Failure to observe this precaution may result in damage to the equipment. Before putting the relay into service, operate the relay to check the electrical connections.

Do not remove or insert printed circuit boards while the STU-12 relay is energized.

APPLICATION

The type STU-12 relay is a solid state directional comparison permissive overreaching transfer trip auxiliary relay for use with solid state or electromechanical distance relays, and a frequency shift type TCF carrier or TA-3 tone channel. This relay will prevent tripping for faults external to the protected line section to which it is applied and permit high speed simultaneous tripping for internal faults. The relay will respond to indications of fault direction and distance provided by the phase and ground distance relays, thereby controlling the transmission of a trip signal and the initiation of high speed tripping for internal faults. Either two or three terminal line applications may be used where all line terminals provide adequate fault current to operate the overreaching distance relays.

CONSTRUCTION

The STU-12 relay is mounted on a standard 19" wide panel 5-$\frac{1}{4}$" high (3 rack units) with edge slots for mounting on a standard relay rack or panel. For the outline and drilling plan refer to Fig. 41.

A hinged and removable door on the front of the chassis covers the printed circuit boards. The photograph in Fig. 1 shows the front view of the relay with the door open. A sealing post at the top center in front may be used to lock and seal the relay when in service.

The rear panel consists of a hinged door which may be opened to expose various components mounted inside. Mounted on the hinged door are two AR type auxiliary relays and, when used, two AL telephone type relays. The AR relay is a small high-speed attracted armature type of unit. An insulated member, fastened to the free end of the armature, draws down four moving contact springs to close or open the contacts when the relay coil is energized. This relay is available for inspection by removing the locking screw and swinging the hinged door outward. In the AL relays, an electromagnet attracts a right-angle iron bracket which in turn operates a set of make or break contacts.

Four power supply resistors are mounted in the rear housing of the chassis. In addition, one 32 terminal connector, J1, and two, (4) terminal, terminal blocks are mounted on the rear of the panel. The photo in Fig. 2 shows the rear view of the STU-12 relay with the top cover off and rear door open.

All of the circuitry suitable for mounting on printed circuit boards is contained in an enclosure behind the front door. The printed circuit boards slide into position in slotted guides at the top and bottom of the enclosure, and engage a terminal block at the rear of the compartment. Each board and terminal block are keyed so that they cannot be accidently inserted into the wrong slot location. A handle mounted on the front end of the board is used for identification, and for removing and inserting the circuit. In addition the handles also serve as a bumper with the front door to prevent the board from becoming disconnected from its terminal block. The boards may be removed for replacement purposes or for use in conjunction with a board extender (Style No. 849A534G01) which permits access to the boards test points and terminals for making measurements while the relay is energized.

Either 13 or 14 printed circuit boards are used in the STU-12 chassis. The location and title of the printed circuit boards are shown on the relay component location drawing, Fig. 3.

Printed Circuit Boards

Following is a description of all the printed circuit boards used in the STU-12 relay. Refer to the functional relay logic shown in Fig. 4, 5, 6, and 7. The internal schematics associated with the printed circuit boards contain a detailed NOR/NAND logic diagram to simplify understanding of the transistor logic.

For those users not generally acquainted with logic circuit notation or with device symbols of those components used in the STU-12 drawings, it is recommended that a copy of Westinghouse instruction leaflet I.L. 41-000.1 entitled SYMBOLS FOR SOLID STATE PROTECTIVE RELAYING be consulted.

Power Supply Board

The Power Supply board located in slot A contains two 20 volt transistor regulators: These voltage regulators will operate from a nominal battery supply of 48 or 125 volts dc by varying resistors RA, RB, RC and RD mounted in the rear of the chassis. The location of components on this board is shown in Fig. 8, and the internal schematic is Fig. 9.

Protective Relay (P.R.) Interface Boards

The Protective Relay (P.R.) Interface board located in slot B contains the buffered interface logic for the distance relays and the functional test switch. Other logic associated with the protective relays is included.

Location of components on this board is shown in Fig. 10. Two internal schematics are used: Fig. 11 - For use with electromechanical distance relays and Fig. 12 - For use with solid state distance relays. The difference in the two schematics is the buffered distance relay input; 48/125 V DC input for electromechanical systems, 20 V DC input for solid state systems.

Loss of Potential Boards

The Loss of Potential board located in slot C contains a 500/0 millisecond time delay and logic to cause an alarm and voltage output if a distance relay inadvertantly operates on a blown ac potential fuse or has a sustained output for greater than 500 milliseconds. An input AND prevents operation of the timer if both channel trip signals are obtained.

In relays for use with electromechanical systems, a relay driver is provided on this board to energize the Loss of Potential AL telephone relay mounted in the rear of the chassis.

Location of components on this board is shown in Fig. 13. Two internal schematics are used: Fig. 14 - For use with electromechanical systems and Fig. 15 for use with solid state systems.

Elec-Mech (E.M.) Interface Board

The Elec-Mech (E.M.) interface board located in slot D is used only in systems using electromechanical distance relays. Upon receipt of a distance relay signal, this circuit of two timers (0/25 and 20/0 millisecond) and associated logic will immediately simulate a protective relay signal for 20 milliseconds, thereby overriding any contact bounce in the electromechanical relays.

Location of components on this board is shown in Fig. 16, and the internal schematic in Fig. 17.

Channel Interface Boards

The Channel Interface boards located in slot F (Channel 1) and slot G (Channel 2 - when used) contain the buffered interface logic for connection with the channel equipment and provide the outputs to work into the Channel Trip and Supv. boards. In addition, the TA-3 Channel Interface board contains buffered outputs.

An interlock feature is also included in order to convert from a 2 to 3 terminal line relay and conversely. **CHANNEL TWO INTERFACE** board in slot G must be used in the relay for **THREE TERMINAL LINE** applications, but MUST BE REMOVED for TWO TERMINAL LINE systems.

A conversion kit may be ordered to change a 2 TERM LINE relay to 3 TERM LINE. This kit includes instructions, nameplate and a CHANNEL INTERFACE BOARD.

The location of components for both the TA-3 and TCF - CHANNEL INTERFACE boards is shown in Fig. 18. Internal schematics are shown in Fig. 19 for the TA-3 CHANNEL and Fig. 20 for the TCF CHANNEL.

Channel Trip Boards

The CHANNEL TRIP board located in slot H contains the connecting logic between the channel trip signals and the remainder of the relay logic. A buffered output for channel 1 and 2 trip is included on this board.

The TONE CHANNEL TRIP board also has additional logic comprised of two AND's and an OR for a guard return function. This logic is inherent to the TCF channel equipment, therefore it is not required in this relay.

Location of components on this board is shown in Fig. 21. Two internal schematics are used: TONE CHANNEL TRIP BOARD - Fig. 22, TCF CHANNEL TRIP BOARD - Fig. 23.

Channel Supervision Board - TCF Channel

The Channel Supervision board for a TCF channel is located in slot I and contains the connecting logic between the supervisory functions of the channel equipment and the remainder of the relay logic. Both LOW SIGNAL CLAMP outputs work into an OR, as do both CHECK TRIP outputs.

For electromechanical systems, a relay driver is used for energizing a loss of channel AL telephone relay.

The location of components for this board is shown in Fig. 27., and the internal schematic in Fig. 28.

Channel Supervision Board - Tone Channel

The Channel Supervision board for a TONE channel is located in slot I and contains the connecting logic between the supervisory functions of the channel equipment and the remainder of the relay logic. A 150/100 millisecond time delay and associated logic is used to monitor the LOW SIGNAL CLAMP outputs for loss of channel. For electromechanical systems, a relay driver is used for energizing a Loss of Channel AL telephone relay. The NOISE outputs work into OR logic on this board.

Location of components for this board is shown in Fig. 24. Two internal schematics are used: Fig. 25 for electromechanical systems and Fig. 26 for solid state systems.

Transmitter Key Board

The Transmitter Key board located in slot J contains OR logic to combine all inputs required to key the transmitter, and interface circuitry to key the particular channel equipment. A relay driver circuit is connected to the output of the OR in order to operate an AR relay mounted in the rear of the chassis.

For the channel interface with the TCF transmitter is a positive going (0 to 20 volt) buffered output represented by transistors Q4 and Q5 is shown on the internal schematic, Fig. 30. When the relay is used with tone channels, the transmitter interface is a negative going output similar to the relay driver and is shown by transistor Q6 on internal schematic, Fig. 31.

Location of components for the XMTR KEY board is shown in Fig. 29.

Checkback Board

The Checkback board located in slot K contains logic used to functionally test the channel in both directions. Two separate circuits are included on this board. One circuit comprised of a buffered input, AND circuit and a 2500/0 millisecond time delay is used for keying the transmitter for 2.5 seconds when the TEST switch is operated. The other circuit consisting of two AND circuits and a 2500/2500 millisecond time delay is operated from the CHANNEL TRIP board and is required as part of the channel checkback scheme.

The location of components for this board is shown in Fig. 32, and the internal schematic in Fig. 33.

Timing Board

The Timing board located in slot L contains logic, a buffered input, and three time delays used in conjunction with the remainder of the relay.

After a pilot trip operation, the 0/30 millisecond timer maintains the transmitter keying for 30 milliseconds. The 180/0 millisecond timer delays keying of the transmitter for 180 milliseconds after opening of the local breaker. Input to this timer is a 48/125 V DC buffer circuit.

The 2500/0 millisecond timer and associated logic is used to permit transient blocking for 2.5 seconds if a trip output is obtained from the channel receiver. This circuit is also controlled by the 52b contact input.

The location of components on this board is shown in Fig. 34, and the internal schematic in Fig. 35.

Arming Board

The Arming board located in slot M contains the connecting logic between the Channel, Protective Relay, Elec-Mech and Timing boards for the OUTPUT board. Logic on this board interfaces with and sets up arming of the trip AND, the transient blocking and unblocking timers and the 4/0 millisecond trip timer.

In addition, two time delays, 0/1000 and 0/100 milliseconds, are included on this board. The 0/1000 MS timer holds transient blocking on for an additional 1000 MS to protect against fault power reversals due to unequal breaker reclosing times into a permanent external fault. After a pilot trip operation, the 0/100 MS timer picks up and immediately resets the 0/1000 MS timer to de-energize the transient blocking timer. The 100 MS dropout time is greater than the time it takes to reset the distance relays, remove the input to the 0/1000 MS timer, therefore transient blocking will remain off, after the pilot trip signal is removed.

The location of components for this board is shown in Fig. 36 and the internal schematic in Fig. 37.

Output Board

The Output board located in slot N contains the final logic of the relay. This board utilizes the intelligence supplied by the Arming board to set up either a pilot trip output for internal faults, transient blocking on external faults or transient unblocking for sequential faults.

Three timers are used on this board: a 4/0 millisecond timer to delay the pilot trip output and two 18/0 millisecond timers for transient blocking and unblocking. NOTE: Relays may be supplied with the transient block time calibrated for 25 milliseconds instead of 18 MS to coordinate with the time delay of the channel equipment. The pilot trip output is comprised of and AND circuit whose output works into a logic inverting amplifier. There are two final pilot trip output; a buffered positive going (0 to 20 volt) output and a relay driver to activate an AR relay mounted in the rear of the chassis. Fig. 38 shows location of components on this board, and Fig. 39 shows the internal schematic and detailed logic.

Test Board

The Test board located in slot O is used for facilitating test measurements and routine checks of the relay. This board consists of 10 test terminals mounted on a panel attached to a printed circuit board.

OPERATION

The type STU-12 transfer trip relay is used in a directional comparison permissive overreaching transfer trip relay system for power line protection. High speed tripping is obtained for two or three terminal line applications for faults anywhere on the protected line, providing all terminals contribute adequate fault current to operate the distance fault detectors.

System Operation

In a directional comparison transfer trip system, a continuous guard signal is normally transmitted from each line terminal and received at all other terminals. The phase or ground protective relays key the channel transmitters to the trip frequency to remove blocking at the remote terminals during a fault. Tripping is accomplished when both the local protective relay operates, and the trip signal has been received.

Some features included in this system are a functional test channel checkback scheme, lockout of tripping after 500 milliseconds for abnormal protective relay operation, channel logic to force a guard return, and coordination for bus fault tripping, breaker failure and fault power flow reversal. The description of the preceding features will be further explained under the RELAY OPERATION section.

Refer to system I.L. 40-205 on the permissive overreaching transfer trip system for further system operation.

Relay Operation

Refer to the logic diagrams shown in Fig. 4, 5, 6, and 7 to understand the operation of the STU-12 transfer trip relay.

1. Normal Condition

In Fig. 4, 5, 6, and 7 the logic voltage "0" and "1" states shown refer to the normal operating condition of the STU-12 relay.

2. Internal Fault

For an internal fault, one or more of the protective distance relays will operate and perform the following:

a. Start the 500/0 MS loss of potential timer
b. Produce a logic "1" at TEST TERMINAL 3 (protective relay)
c. Key the transmitter to the trip frequency
d. Pickup the 0/1000 MS timer on the ARMING board and produce a logic "0" at terminal 5 of the OUTPUT board. This will start the transient blocking timer.
e. Arm the trip AND on the OUTPUT board throught the one input OR on the ARMING board.
f. Satisfy one input of the trip AND on the ARMING board.

The channel transmitter will also be keyed at the remote terminal, thus causing the trip outputs of the local channel 1 and 2 receivers to become a logic "1". This will make TEST TERM 4 (CHANNEL TRIP) a logic "1" signal through logic on the CHANNEL INTERFACE and CHANNEL TRIP BDS. This "1" output will satisfy the trip AND on the ARMING BD. causing energization of the 4/0 MS timer on the OUTPUT BD. Four milliseconds later the trip AND on the OUTPUT BD. will be satisfied and produce a Pilot Trip Output before transient blocking becomes effective.

In addition, when a receiver trip output is received as an input to the STU-12 the 2500/0 MS timer on the TIMING BD. will be energized to start transient blocking. This will not affect the initial pilot trip, and once the local breaker opens, then the 52b contact will block the output of this AND on the TIMING BD.

Once a pilot trip signal is obtained for an internal fault, the 0/100 MS timer on the ARMING BD. will rapidly reset the 1000 millisecond dropout time of the 0/1000 MS timer. Therefore, when reclosing into a permanent internal fault, the only time delay will be the 8/0 MS timer.

3. External Fault

If no channel trip signal is received from the remote terminal when the local distance relays operate, then the trip AND on the ARMING BD. will not be satisfied and the 18/0 MS transient blocking timer will time out. TEST TERMINAL 2 (Transient Blocking) will then become a negative logic "1" and block the trip AND of the OUTPUT BD. thereby preventing possible undesirable tripping during transients occuring at the clearing of an external fault.

If an external fault occurs behind the protected line such that the local distance relays do not operate, but either one or both of the channel receivers are keyed to the trip frequency at the remote terminal then transient blocking will also be set up. When either channel trip output assumes a logic "1" state, the 2500/0 MS timer on the TIMING BD. is energized and a logic "1" is obtained at TIMING BD. terminal 10 for 2.5 seconds. This output will activate the 0/1000 MS timer on the ARMING BD. and set up transient blocking 18 milliseconds later.

In addition, for external faults, transient blocking is established to insure against any misoperation due to fault power flow reversals caused by unequal circuit breaker clearing time on parallel lines. The 1000 millisecond reset time of the 0/1000 MS timer on the ARMING BD. prevents misoperations when reclosing into an external fault where fault power flow reversals occur on parallel lines due to unequal breaker reclosing times. In addition, the 1000 millisecond reset time also prevents transient blocking from resetting when short holes appear in the input.

4. Sequential Fault

Occasionally an external fault will be followed by an internal fault before the former is cleared. In order to prevent a long delay in clearing a sequential fault, a transient unblocking 18/0 MS timer is included. Although transient blocking has been initiated by the external fault, the presence of an internal fault will produce a negative logic "1" signal from the trip AND on the ARMING BD. This "1" signal will energize the 4/0 MS timer and satisfy the AND to energize the 18/0 MS transient unblocking timer on the OUTPUT BD. In 18 milliseconds the transient unblocking timer will drop out the transient blocking timer thus satisfying the trip AND on the OUTPUT BD. and causing a pilot trip output.

5. Loss of Potential

Distance relays may tend to operate if the input from the potential device is momentarily interrupted. Since tripping of circuit breakers is undesirable for this loss of ac potential, or any other abnormal protective relay operation, the STU-12 relay will lockout tripping and provide alarm. This ia accomplished by the 500/0 MS timer on the LOSS OF POTENTIAL BD. In 500 milliseconds after a distance relay operation, providing both receiver trip signals are not present, a logic "1" signal will be produced at TEST TERMINAL 7 (Loss of Potential). This "1" signal will block the AND on the PROTECTIVE RELAY INTERFACE BD. thereby simulating no distance relay signal. Output of the 500/0 MS timer will also provide a buffered "1" signal at the J1 connector.

For electromechanical systems, an AL telephone relay will drop out for indication purposes.

6. Channel Transmitter Control

The transmitter may be keyed to the trip frequency by any one of six inputs as follows:

a. Distance relay operation
b. 0/30 MS timer after pilot trip
c. 180/0 MS timer from 52b contact
d. Checkback circuit from test switch
e. Checkback circuit from channel logic
f. Output from EM Interface bd. for electromechanical systems only.

When the transmitter is keyed, TEST TERMINAL 5 (XMTR KEY) becomes a logic "1" signal, the keying AR picks up, and the interface with the transmitter becomes a logic "1" as described under the operation of the XMTR KEYING BD.

After a pilot trip operation the 0/30 MS timer on the TIMING BD. will maintain keying of the trip frequency for 30 milliseconds in order to insure that the remote breaker has tripped before the transmitter returns to normal condition.

After the local circuit breaker opens, the 52b contact will energize the 180/0 MS timer on the TIMING BD. and initiate trip frequency transmission after 180 milliseconds and until such time as the circuit breaker is reclosed. This 180 millisecond delay allows coordination for bus fault tripping of the local breaker, where tripping of the remote breaker would be incorrect and might cause undesired interruption to tapped transformer terminals. Transmission of the trip frequency is necessary to permit tripping of the remote terminal should the remote circuit breaker be closed into a fault, or should a fault develop in the protected line while the local circuit breaker is open.

7. Channel Logic

a. TCF frequency shift carrier channel
Refer to CHANNEL-INTERFACE, TRIP, and SUPERVISION BDS. in logic drawings Fig. 4 and 5.

Two TCF CHANNEL INTERFACE boards are shown: Both boards must be used for three terminal line systems utilizing two receivers. However, for two terminal line applications, the interface board in board slot G must not be used in the relay. An interlock shown on the Channel 2 interface board connects the Channel 2 trip output as one output to the Channel trip AND on the CHANNEL TRIP BD.

For three terminal line applications, both receiver trips signals are required to produce a logic "1" signal at TEST TERMINAL 4. This output will satisfy one input of the ARMING BD. trip AND, block operation of the 500/0 MS loss of potential timer, and produce a buffered "1" output. Either receiver trip signal will produce a "1" signal at terminal 12 of the CHANNEL TRIP BD. to start transient blocking.

For two terminal line applications, the one receiver trip signal will produce a "1" output at TEST TERMINAL 4 (CHANNEL TRIP), and terminal 12 of the CHANNEL TRIP BD.

Operation of either or both low signal clamp inputs ("1" to "0") will cause a "1" signal at TEST TERMINAL 6 (LOSS OF CHANNEL) for use in the channel checkback scheme. For electromechanical systems, an AL telephone relay will dropout for indication of loss of channel. In addition, operation of either Check Trip output will produce a "1" output at terminal 7 of the CHANNEL SUPERVISION BD. This signal is used for the channel checkback scheme.

b. Frequency shift tone channel
   Refer to CHANNEL INTERFACE, TRIP and SUPERVISION BDS. in logic drawings Fig. 6 and 7.

Two TONE CHANNEL INTERFACE boards are shown; Both boards must be used for three terminal line systems utilizing two receivers. However, for two terminal line applications, the interface board in board slot G must not be used in the relay. An interlock shown on the channel 2 interface board connects the channel 2 trip output as one input to the three input channel trip AND on the CHANNEL TRIP BD.

For three terminal line applications, both receiver trip signals and no low signal clamps are required to produce a logic "1" signal at TEST TERMINAL 4 (CHANNEL TRIP). This output will satisfy one input of the ARMING BD. trip AND, block operation of the 500/0 MS loss of potential timer, and produce a buffered output. Either receiver trip signal will produce a "1" signal at terminal 12 of the CHANNEL TRIP BD. to start transient blocking and to energize an AND circuit on the CHANNEL SUPERVISION BD.

For two terminal line applications, the one receiver trip signal will produce a "1" output at TEST TERMINAL 4, and terminal 12 of the CHANNEL TRIP BD.

When a Tone Channel is used with the STU-12 transfer trip relay, the Tone receivers must be internally strapped to clamp to no trip output when a low signal condition occurs. Therefore, tripping will not be allowed under loss of channel.

Either LOW signal clamp operation ("1" to "0") will pickup the 150/100 MS timer and produce a "1" signal at TEST TERMINAL 6 (LOSS OF CHANNEL) for use in channel checkback as well as blocking Channel Trip. For electromechanical systems, an AL telephone relay will dropout for indication of loss of channel. Both low signal clamp outputs on the CHANNEL INTERFACE BDS. are buffered and separately brought out to the J1 connector.

One AND circuit on the CHANNEL SUPERVISION BD. is used for channel checkback. When a receiver trip signal from either channel is received, a logic "1" will be produced at terminal 3 of the CHANNEL SUPERVISION BD. providing both low signal clamps have not operated.

When the noise output operates on either one or both channel receivers, a logic "1" output is produced from the noise OR on the CHANNEL SUPERVISION BD. to block the trip AND of the ARMING BD. Therefore, the STU-12 relay will not trip on receipt of channel noise. Both noise outputs on the CHANNEL INTERFACE BD. are buffered, connected together, and brought out to the J1 connector.

A guard return circuit is included on the CHANNEL TRIP BD. and is comprised of two AND's and an OR. The principle of guard return, is to insure that after a loss of channel condition is cleared up, the receiver trip signal will return in the "0" logic state, not "1". When a low signal clamp operation ("1" to "0") is received from the tone channel, then the 150/100 MS timer picks up and applies a "1" signal to one input of each of the two guard return AND's on the CHANNEL TRIP BD. Now, if either or both receiver trip signals are "1" or become a "1" within the 100 millisecond dropout time of the 150/100 MS timer, then a "1" output will be produced at the output of the guard return AND and the OR it works into. Terminal 5 of the CHANNEL TRIP BD. will become a "1" and hold the 150/100 MS timer picked up by applying a "1" input to the 3 input loss of channel OR on the CHANNEL SUPERVISION BD. By inspecting the logic it can be seen that both receiver trip signals (one for two terminal line applications) must return to guard, logic "0", to make the channel operative after a loss of channel condition.

8. Channel Checkback Test

a. TCF frequency shift carrier channel
Refer to logic drawings, Fig. 4 and 5. Information in this section does not cover the complete test, but only that portion concerning the STU-12 relays.

At the local terminal, the carrier transmitter will be disconnected from the line thus causing a loss of channel condition at the remote terminal. This will cause the loss of channel OR on the CHANNEL SUPERVISION BD. (Remote Terminal) to assume a "1", and satisfy the two input AND (preceding the 2500/2500 MS timer) and in 2500 milliseconds pickup the 2500/2500 MS timer on the CHECKBACK BD. The "1" output of the 2500/2500 MS timer will satisfy one input of the AND following it. Next, the test switch will be operated at the local terminal and the following will happen: a protective relay signal will be simulated through the OR on the PROTECTIVE RELAY INTERFACE BD., the transmitter will be reconnected to the line to restore the channel, and the local transmitter will be keyed to the trip frequency for 2500 milliseconds through the 2500/0 MS timer and AND circuit on the CHECKBACK BD. At the remote terminal, the TCF receiver logic will not give a trip output since the channel was not restored to the guard frequency. However, there will be a "1" signal obtained from the CHECK TRIP output of the receiver. This check trip output will satisfy the other input to the AND on the CHECKBACK BD. causing the transmitter to be keyed to the trip frequency. Since the check trip signal also applies a "1" input to the negated input of the AND energizing the 2500/2500 MS timer, it will no longer be satisfied and the timer will dropout causing keying to stop in 2.5 seconds. However, within the 2.5 seconds of keying, the STU-12 relay at the local terminal will trip because of reception of both a received trip signal and a simulated protective relay signal.

b. Frequency shift tone channel
Refer to logic drawings, Fig. 6 and 7
◆ Information in this section does not cover the complete test, but only that portion concerning the STU-12 relay.

At the local terminal, the tone transmitter will be disconnected from the line thus causing a loss of channel condition at the remote terminal. This will cause the loss of channel OR on the CHANNEL SUPERVISION BD. (remote terminal) to assume a "1" output to pickup the 150/100 MS timer. This satisfies the two input AND on the Check Back Bd. and in 2500 milliseconds the 2500/2500 MS timer will pick up. The "1" output of the 2500/2500 MS timer will satisfy one input of the AND following it. Next, the test switch will be operated at the local terminal and the following will happen: a protective relay signal will be simulated through the OR on the PROTECTIVE RELAY INTERFACE BD., the transmitter will be reconnected to the line to restore the channel, and the local transmitter will be keyed to trip frequency for 2500 milliseconds through the 2500 MS timer and AND circuit on the CHECKBACK BD. At the remote terminal, the tone receiver trip signal will be a "1" thus causing the three input AND on the CHANNEL SUPERVISION BD. to operate and produce a "1" at terminal 3 of this board. This "1" will satisfy the other input to the AND on the CHECKBACK BD. causing the transmitter to be keyed to the trip frequency. Since at the same time, the input to the 2500/2500 MS timer is lost, then the keying signal to local terminal will only last 2.5 seconds. However, within this time of keying, the STU-12 relay will trip because of the reception of both a received trip signal and a simulated protective relay signal.

9. Electromechanical Interface

When the STU-12 relay is used in an electromechanical system the ELEC-MECH (E.M.) INTERFACE BD. is used only for the purpose of preventing additional tripping delay because of contact bounce. When a distance relay operates, the 0/25 MS time delay on the E.M. INTERFACE BD. will immediately pickup to satisfy the AND thereby simulating a protective relay operation. The 25 millisecond dropout time of the 0/25 MS timer will hold the "1" input to the AND in the event that bouncing contacts interrupt the timer input signal. The 20/0 timer will time out and remove the simulated protective relay signal after 20 milliseconds.

CHARACTERISTICS

Control Voltage:	48 V DC (42 to 56 volts) 125 V DC (105 to 140 volts)
Current Drain:	SOLID STATE SYSTEMS Normal - 130 MA Pilot Trip - 240 MA Maximum - 280 MA ELEC-MECH SYSTEMS Normal - 170 MA Pilot Trip - 280 MA Maximum - 320 MA
Temperature Range:	-20 C to +55 C around chassis
Inputs:	
52b Contact -	48/125 Control Voltage Buffered 48V - 1.5 MA MAX CURRENT 125V - 2.5 MA MAX CURRENT

Distance Relays 1, 2, 3	
	SOLID STATE SYSTEMS
	15 to 20 V DC Buffered 2 MA MAX CURRENT
	ELEC-MECH SYSTEMS
	48/125 Control Voltage Buffered 48 V - 1.5 MA MAX CURRENT 125 V - 2.5 MA MAX CURRENT
All Other Inputs are:	15 to 20 V DC, buffered and require 2 MA MAX CURRENT

Outputs:

Transmitter Key:

TCF Frequency Shift Carrier Channel	15 to 20 V DC Buffered 10 MA MAX CURRENT
Frequency Shift Tone	"0" State - Open Circuit "1" State - Short Circuit to Battery Neg. 140 V DC MAX Voltage 40 MA MAX CURRENT

All Other Outputs are 15 to 20 V DC Buffered and provide 10 MA MAX CURRENT.

Time:

Trip Time (4/0)	4.0 to 4.5 Milliseconds (adjustable from 2.0 to 6.0 MS)
Transient Block and Transient Unblock Time (18/0)	18 to 20 Milliseconds (adjustable from 12 to 30 MS) (Relays may be ordered with a transient blocking time of 24 to 27 milliseconds)
Low Signal Lockout Time	130 to 180 Milliseconds
Loss of Potential Time (500/0)	400 to 600 Milliseconds
Dimensions:	relay height - 5.25" (3 rack units) relay width - 19" relay depth - 14"
Weight:	approximately 12 lbs.

SETTINGS

No setting is required on the STU-12 relay.

INSTALLATION

The STU-12 relay is generally supplied in a cabinet or on a relay rack as part of a complete system. The location must be free from dust, excessive humidity, vibration, corrosive fumes or heat. The maximum temperature around the chassis must not exceed 55 C.

The outline and drilling plan of the STU-12 relay is shown in Fig. 41.

ADJUSTMENTS AND MAINTENANCE

Acceptance Check

It is recommended that an acceptance check be applied to the STU-12 relay to verify that the circuits are functioning properly. The following procedure can be used for this purpose.

Connect the STU-12 relay to the test circuit of Fig. 40. Apply rated dc to J1 terminals 3 and 4 as shown, and use an auxiliary 20 volt regulator or the internal 20 volts of the STU-12 relay for the inputs to the switches. On STU-12 relays for use with electro-mechanical distance relays, rated positive dc must be applied to the PR 1, 2, and 3 switches. Note that the low signal switches for channels 1 and 2 are normally closed and all other switches are open.

Since the STU-12 relay varies in logic depending on the channel equipment, insure that it is checked per the proper channel. When reference is made to AL relays, this refers to STU-12 relays for use only with electro-mechanical systems utilizing elec-mech distance relays.

When reference is made to TEST TERMINAL, this means one of the 10 test terminals on the TEST BD. in board slot 0. All voltages are to be measured with respect to negative, TEST TERMINAL 10. Voltage measurements may vary by ±10%. Information in this acceptance test applies to a relay with a transient blocking time of 18 MS. For relays with a transient blocking time of 25 MS., limits are 24 to 27 milliseconds.

A. Normal Condition

TEST TERMINAL 1: 0 Volts
" " 2: 20 Volts
" " 3: 0 Volts
" " 4: 0 Volts
" " 5: 0 Volts
" " 6: 0 Volts
" " 7: 0 Volts
" " 8: 20 Volts
" " 9: 20 Volts

Keying AR - Not picked up
Trip AR - Not picked up
Loss of Channel AL - Picked up (Elec-Mech System)
Loss of Potential AL - Picked up (Elec-Mech System)

B. Channel Logic - 2 Term Line Relays Only
(For 3 Term Line relays, disregard this section and continue on section C)

1. TCF Carrier Channel

a. Channel Trip - 2500/0 MS timer (TIMING BD.), 0/1000 MS timer
Close Trip-1 switch
Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds, then rise from 0 to 20 volts in 3100 to 4100 milliseconds
Test Term 4: Voltage rise from 0 to 20 volts
Open Trip-1 switch

b. Loss of Channel
Open LOW SIGNAL-1 switch
Test Term 6: Voltage rise from 0 to 20 volts
Loss of Channel AL will drop out
Close LOW SIGNAL-1 switch

2. Tone Channel

a. Channel Trip - 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer
Close Trip-1 switch
Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds, then rise from 0 to 20 volts in 3100 to 4100 milliseconds
Test Term 4: Voltage rise from 0 to 20 volts
Open Trip-1 switch

b. Loss of Channel - 150/100 MS timer (CHANNEL SUPERVISION BD.)

Open LOW SIGNAL-1 switch
Test Term 6: Voltage rise from 0 to 20 volts in 130 to 180 milliseconds
Loss of Channel AL will drop out
Close LOW SIGNAL-1 switch
Test Term 6: Voltage drop from 20 to 0 volts in 75 to 125 milliseconds

c. Guard Return

Open LOW SIGNAL-1 switch, then close Trip-1 switch
Test Term 4: Voltage must remain at zero
Close LOW SIGNAL-1 switch
Test Term 6: Voltage must remain at 20 volts
Open Trip-1 switch
Test Term 6: Voltage must drop from 20 to 0 volts

C. Channel Logic - 3 Term Line Relays Only

(For 2 Term Line relays, the preceding section was used and this part may be disregarded)

1. TCF Carrier Channel

   a. Channel 1 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer
      Close Trip-1 switch
      Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds
      Test Term 4: Voltage remains at zero
      Open Trip-1 switch

   b. Channel 2 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer
      Close Trip-2 switch
      Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milli- then rise from 0 to 20 volts in 3100 to 4100 milliseconds
      Test Term 4: Voltage remains at zero
      Open Trip-2 switch

   c. Channel 1 and 2 Loss of Channel
      Open LOW SIGNAL-1 switch
      Test Term 6: Voltage rise from 0 to 20 volts
      Loss of Channel AL must drop out
      Close LOW SIGNAL-1 switch, then open LOW SIGNAL-2 switch
      Test Term 6: Voltage rise from 0 to 20 volts
      Loss of Channel AL must drop out
      Close LOW SIGNAL-2 switch

   d. Channel 1 and 2 switches
      Test Term 4: Voltage rise from 0 to 20 volts
      Open Trip-1 and Trip-2 switches

2. Tone Channel

   a. Channel 1 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer
      Close Trip-1 switch
      Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds
      Test Term 4: Voltage remains at zero
      Open Trip-1 switch

   b. Channel 2 - TRIP 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.) transient blocking timer
      Close trip-2 switch
      Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milli-

seconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds
Test Term 4: Voltage remains at zero
Open Trip-2 switch

c. Guard Return - Channel 1 - Trip and Low Signal - 150/100 MS timer
Open LOW SIGNAL-1 switch
Test Term 6: Voltage rise from 0 to 20 volts in 130 to 180 milliseconds
Loss of Channel AL must drop out
Close Trip-1 switch, then close LOW SIGNAL-1 switch
Test Term 6: Voltage must remain at 20 volts
Open Trip-1 switch
Test Term 6: Voltage must drop from 20 to 0 volts in 75 to 125 milliseconds

d. Guard Return - Channel 2 - Trip and Low Signal - 150/100 MS timer
Open LOW SIGNAL-2 switch
Test Term 6: Voltage rise from 0 to 20 volts in 130 to 180 milliseconds
Loss of Channel AL must drop out
Close Trip-1 switch, then close LOW SIGNAL-1 switch
Test Term 6: Voltage must remain at 20 volts
Open Trip-1 switch
Test Term 6: Voltage must drop from 20 to 0 volts in 75 to 125 milliseconds

e. Channel 1 and 2 - Trip and Low Signal
Close Trip-1 and Trip-2 switches
Test Term 4: Voltage rise from 0 to 20 volts
Open LOW SIGNAL-1 switch
Test Term 4: Voltage drop from 20 to 0 volts
Open Trip-1 and Trip-2 switches, then close LOW SIGNAL-1 switch

D. Distance Relay Operation

a. Distance relay operation-loss of potential 500/0 MS timer
Close PR-1 switch
Test Term 7: Voltage rise from 0 to 20 volts in 400 to 600 milliseconds
Loss of Potential AL must drop out
Test Term 3 & 5: Voltage rise from 0 to 20 volts immediately and then drop from 20 to 0 volts in 400 to 600 milliseconds
XMTR key AR picks up immediately then drops out in 400 to 600 milliseconds
Open PR-1 switch
The same as the preceding must happen by closing either the PR-2 or PR-3 switch

b. Distance relay operation - no loss of potential
Close Trip-1 and Trip-2 switches
(Trip-2 switch not required for 2 Term Line relays)

Close either PR-1, PR-2, PR-3 switches
Test Term 7: Voltage must remain at zero, the loss of potential timer must not pickup
Open Trip-1, Trip-2, and PR switches

E. Test Switch Operation - 2500/0 MS timer (CHECKBACK BD.)
0/1000 MS timer (ARMING BD.)
18/0 Transient blocking timer (OUTPUT BD.)

Close test switch
Test Term 3: Voltage must rise from 0 to 20 volts
Test Term 2: Voltage must drop from 20 to 0 volts in 18 to 20 milliseconds
Test Term 5: Voltage must rise from 0 to 20 volts immediately, then drop from 20 to 0 volts in 2000 to 3000 milliseconds
Also, XMTR KEY AR must pickup for 2 to 3 seconds
Open Test switch
Test Term 2: Voltage must rise from 0 to 20 volts in 900 to 1300 milliseconds

F. 52b Contact Operation - 180/0 MS timer (TIMING BD.)
Close 52b switch
Test Term 5: Voltage must rise from 0 to 20 volts in 180 to 230 milliseconds
Open 52b switch

G. Channel Checkback Operation

1. TCF Carrier Channel
2500/2500 MS timer (CHECKBACK BD.), check trip inputs

Open LOW SIGNAL-1 switch
TP4 on CHECKBACK BD. voltage must drop from 8 to 0 volts in 2000 to 3000 milliseconds
Close CK Trip-1 switch
Test Term 5: Voltage must rise from 0 to 20 volts immediately then drop from 20 to 0 volts in 2000 to 3000 milliseconds
XMTR KEY AR must pickup for 2 to 3 seconds
Close LOW SIGNAL-1 switch, then open CK Trip-1 switch
For relay used for 3 Term Line, also do the following:
Open LOW SIGNAL-2 switch and wait for 3 seconds, then close CK Trip-2 switch
Test Term 5: Voltage must rise from 0 to 20 volts immediately then drop from 20 to 0 volts in 2 to 3 seconds.
Close LOW SIGNAL-2 switch, then open CK Trip-2 switch

2. Tone Channel
2500/2500 MS timer (CHECKBACK BD.)

Open LOW SIGNAL-1 switch
TP4 on CHECKBACK BD.: Voltage must drop from 8 to 0 volts in 2000 to 3000 milliseconds
Close Trip-1 switch, then close LOW SIGNAL-1 switch
Test Term 5: Voltage must rise from 0 to 20 volts immediately then drop from 20 to 0 volts in 2000 to 3000 milliseconds

XMTR KEY AR must pick up for 2 to 3 seconds
Open Trip-1 switch
For relays used for 3 Term Line, also do the following:
Open both LOW SIGNAL-1 and LOW SIGNAL-2 switches then close Trip-2 switch. Wait for 3 seconds then close both LOW SIGNAL-1 and 2 switches
Test Term 5: Voltage must rise from 0 to 20 volts immediately after closing both the LOW SIGNAL switches then drop from 20 to 0 volts in 2 to 3 seconds
Open Trip-2 switch

H. Pilot Trip - 4/0 MS Timer (OUTPUT BD.)

Close 52b switch in order to prevent the 2500/0 MS timer from starting transient blocking
Close Trip-1 switch, and also, for 3 Term Line relays, close Trip-2 switch
Then, close TEST Switch
Test Term 1: Voltage must rise from 0 to 20 volts in 4.0 to 4.5 milliseconds
Trip AR must pickup
Open Trip-1 and Trip-2 switches
Test Term 1: Voltage must remain at 20 volts
Open Test switch and Trip AR must drop out
Open 52b switch

I. Pilot Trip After Transient Unblocking 18/0 MS Timer (OUTPUT BD.)

Close Test switch
Then, close Trip-1 switch, and also for 3 Term Line relays, close Trip-2 switch
Test Term 1: Voltage rise from 0 to 20 volts in 18 to 20 milliseconds
Open Test switch
Test Term 1: Voltage drop from 20 to 0 volts
Open Trip-1 and Trip-2 switches

J. Continue Key after pilot trip - 0/30 MS Timer (TIMING BD.)

Close test switch, then wait until XMTR KEY AR drops out then close Trip-1 switch and for 3 Term Line relays, also close Trip-2 switch
As soon as the voltage on Test Term 1 rises from 0 to 20 volts then the 0/30 MS timer will pickup in less than 1 millisecond and the voltage at Test Term 5 will rise from 0 to 20 volts
Then open Test switch
Test Term 5: Voltage must drop from 20 to 0 volts in 24 to 30 milliseconds
Open Trip-1 and Trip-2 switches

K. Fast Reset of 0/1000 MS timer after pilot trip .0/100 MS timer (ARMING BD.)

For checking this 0/100 MS timer, it will be necessary to use a jumper
Close Test switch, then close Trip-1 switch and also for 3 Term

Line relays close Trip-2 switch
Terminal 4 (ARMING BD.): Voltage must rise from 0 to 16 volts in less than 2 milliseconds after the voltage at Test Term 1 rises from 0 to 20 volts
In order to check the 100 millisecond reset time, it is necessary to connect a jumper from TP-8 to terminal 14 on the ARMING BD.
Open Test switch
Terminal 4 (ARMING BD.): Voltage must drop from 16 to 0 volts in 70 to 170 milliseconds
Open Trip-1 and Trip-2 switches, and remove the jumper

L. Elec-Mech Interface 0/25 and 20/0 MS timers (ELEC-MECH (E.M.) INTERFACE BD.)

This section is to be used only for those STU-12 relays which are for use with electromechanical distance relays
Close PR-1, PR-2, or PR-3 switches
Terminal 4 (E.M. INT. BD.): Voltage must rise from 0 to 11 volts immediately then drop back to zero in 16 to 24 milliseconds
Open PR-1, PR-2 and PR-3 switches
Terminal 4 (E.M. INT. BD.): Voltage must remain at zero.

M. Noise Operation

This section is to be used only for those STU-12 relays which are for use with a frequency shift tone channel.
Close NOISE-1 switch
Then close Test switch and Trip-1 switch, and also for 3 Term Line relays close Trip-2 switch
Test Term 1: Voltage must remain at zero
Open Noise-1 switch
Test Term 1: Voltage must rise from 0 to 20 volts
Trip AR must pickup
Open Test, Trip-1 and Trip-2 switches
For 3 Term Line relays, repeat above test using Noise-2 switch instead by Noise-1 switch.

Recommended Routine Maintenance

Periodic checks of the relaying system are desirable to indicate impending failure so that the equipment can be taken out of service for correction. Any accumulated dust should be removed at regular maintenance intervals.

All contacts should be periodically cleaned. A contact curnisher, Style No. 182A836H01, is recommended. The use of abrasive material is not recommended because of the danger of embedding small particles in the face of the soft silver and thus impairing the contact.

CALIBRATION

The proper adjustments to insure correct operation of the relay have been made at the factory and should not be disturbed after receipt by the customer. However, if the adjustments or if the components or printed circuit boards which affect calibration have been changed, then the STU-12 relay should be rechecked per the acceptance check information.

All time delays are fixed except for the three timers on the OUTPUT BD.: 18/0 MS transient blocking timer, 18/0 MS transient unblocking timer, and the 4/0 MS trip timer. These adjustable timers can be recalibrated as follows using an auxiliary timer or oscilloscope.

Transient Block 18/0 MS Timer - OUTPUT BD.

(NOTE: For relays having a transient blocking timer of 25/0 MS limits are 24 to 27 milliseconds)

Start timer on Test switch (positive pulse)
End timer on Test Term 2 (negative pulse)

Close Test switch and the voltage on Test Term 2 must drop from 20 to 0 volts in 18 to 20 milliseconds (24 to 27 MS)

This time can be adjusted by turning potentiometer R14 on the OUTPUT clockwise for more time or counter clockwise for less time. (After recalibrating this timer also recheck the calibration of the 4/0 MS timer)

Pilot Trip 4/0 MS Timer - OUTPUT BD.

Start timer on Test switch (positive pulse)
End timer on Test Term 1 (positive pulse)

For this calibration, close 52b switch

Close Trip-1 switch, and also Trip-2 switch for 3 Term Line relays

Then close Test switch and the voltage on Test Term 1 must rise from 0 to 20 volts in 4.0 to 4.5 milliseconds

This time can be adjusted by turning potentiometer R20 on the OUTPUT BD. clockwise for more time or counter-clockwise for less time.

(After recalibrating this timer, also recheck calibration of the 18/0 MS transient block timer)

Transient Unblocking 18/0 MS Timer - OUTPUT BD.

Start timer on Trip-1 switch (positive pulse)
End timer on Test Term 1 (positive pulse)

Close Test switch, and also close Trip-2 switch for 3 Term Line relays

Then close Trip-1 switch and the voltage on Test Term 1 must rise from 0 to 20 volts in 18 to 20 milliseconds

This time can be adjusted by turning potentiometer R1 on the OUTPUT BD. clockwise for more time and counter-clockwise for less time.

Tripping Relay (AR)

The type AR tripping relay unit has been properly adjusted at the factory to insure correct operation and should not be disturbed after receipt by the customer. If, however, the adjustments are disturbed in error, or it becomes necessary to replace some part in the field, use the following adjustment procedure. This procedure should not be used until it is apparent that the AR unit is not in proper working order, and then only if suitable tools are available for checking the adjustments.

a. Adjust the set screw at the top of the frame to obtain a 0.009 inch gap at the rear end of the armature air gap.

b. Adjust each contact spring to obtain 4 grams pressure at the very end of the spring. This pressure is measured when the spring moves away from the edge of the slot in the insulated crosspiece.

c. Adjust each stationary contact screw to obtain a contact gap of 0.020 inch. This will give 15-30 grams contact pressure.

Trouble Shooting

The components of the STU-12 relay are operated well within their ratings and normally will give long and trouble-free service. However, if a relay has given an indication of trouble in service or during routine checks, then using "0" and "1" logic notation, the faulty printed circuit board can be traced to using the diagrams in Fig. 4, 5, 6, or 7. In turn, the faulty, component or circuit can be found using the individual schematics of the printed circuit boards which show the detailed transistor NOR/NAND logic.

Each NOR/NAND logic block represents a transistor on the schematic. The output of each individual logic block is the collector of the transistor which represents that block. The collector of each transistor is either connected to a test point or printed circuit terminal. A box around the transistor indicates that it is conducting for the normal condition of the relay.

Following is an explanation of the voltage levels for the "0" and "1" logic notation as shown for the normal relay condition in Figs. 4, 5, 6, and 7. This logic notation will also apply to the detailed logic on the printed circuit board internal schematics.

For positive logic - represented by logic blocks, with no arrows. "0" is equivalent to less than 0.5 volts with respect to negative, Test Term 10.

"1" is equivalent to 8 to 20 volts with respect to negative, Test Term 10.

For negative logic - represented by logic blocks with open arrow heads, "0" is equivalent to 8 to 20 volts with respect to negative, Test Term 10, except for the output of the relay driver, where a "0" is rated positive dc.

"1" is equivalent to less than 0.5 volts with respect to negative, Test Term 10.

A board extender, Style No. 849A534G01, is available for facilitating circuit voltage measurements. After withdrawing anyone of the circuit boards, the extender is inserted into that slot. The board is then inserted into the terminal block on the front of the extender to restore all circuit connections.

The Test Terminals on the Test Bd. in the board position to the extreme right are helpful in checking the overall relay operation. Following are the voltages that will occur at these Test Terminals under various conditions:

NOTE: All voltages referred to are taken with respect to negative, Test Terminal 10.

Test Terminal 1: Pilot Trip

Normal Condition - 0 volts
Internal Fault - 20 volts

For an internal fault, either a distance relay or test switch operation and both receiver trip signals (one receiver trip signal for 2 Term Line relays) are required.

Test Terminal 2: Transient Blocking & Unblocking

Normal Condition - 20 volts
External Fault - 0 volts

The following will simulate an external fault:
- distance relay operation
- test switch operation
- either channel receiver trip operation

Test Terminal 3: Protective Relay

Normal Operation - 0 volts
Distance Relay Operation - 20 volts
Test Switch Operation - 20 volts

Test Terminal 4: Channel Trip

Normal Condition - 0 volts
Operation of Channel 1 and 2 receiver trip outputs - (for 2 Term Line relays, only 1 channel required) - 20 volts

Test Terminal 5: XMTR Key

Normal Condition - 0 volts
Distance Relay Operation - 20 volts
52b contact operation - 20 volts
Internal Fault

(pilot trip signal) - 20 volts
Test Switch operation - 20 volts for 2.5 seconds
Channel Checkback scheme - 20 volts for 2.5 seconds

Test Terminal 6: Loss of Channel

Normal Condition - 0 volts
Operation of either channel 1 or 2 Low signal clamp - 20 volts

Test Terminal 7: Loss of Potential

Normal Condition - 0 volts
Distance relay operation - 20 volts after 500 MS time delay
Distance relay and both receiver trip signal operation
(one receiver trip signal for 2 Term Line relays) - 0 volts

Test Terminal 8 and 9: Pos. 20 V DC

Normal Condition - 0 volts

Test Terminal 10: Negative DC

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing the repair work. When ordering parts, always give the complete nameplate data, and the component Style No. given in the Electrical Parts List.

ELECTRICAL PARTS LIST

Power Supply Board - S# 202C465G01

Circuit Symbol	Reference	Style
	CAPACITORS	
C1, C2	6.8 MFD, 35 V, ±20%	184A661H10
	DIODES	
D1, D2	1N645A	837A692H03
	RESISTORS	
None on PCB	None	
	TRANSISTORS	
Q1, Q2	2N3589	837A617H01
	ZENER DIODES	
Z1, Z3	1N3050A (180 V - 1W)	187A936H16
Z2, Z4	1N4747A (20 V - 1W)	849A487H01
Heat Sink for Q1 & Q2		849A517H01

Protective Relay - S# 202C466G01 - Solid State Systems
Interface Board - S# 202C475G01 - Elec-Mech Systems

Circuit Symbol	Reference	Style
	CAPACITORS	
C1, C2	.047 MFD, 200 V DC	849A437H04
	DIODES	
D1, D2	1N645A	837A692H03
	RESISTORS	
R1, R2, R3 Δ	4.7 K, ½W, ±2%	629A531H48
R1, R2, R3 #	47 K, ½W, ±2%	629A531H72
R4, R15, R16	4.7 K, ½W, ±2%	629A531H48
R5, R17, R22	82 K, ½W, ±2%	629A531H78
R6, R9, R13, R19, R20	10 K, ½W, ±2%	629A531H56
R7, R10, R14, R21	6.8 K, ½W, ±2%	629A531H52
R8, R11, R12, R18	27 K, ½W, ±2%	629A531H66
	TRANSISTORS	
Q1, Q2, Q3, Q4	2N3417	848A851H02
Q5	2N3645	849A441H01

ELECTRICAL PARTS LIST

Protective Relay - S# 202C466G01 - Solid State Systems
Interface Board - S# 202C475G01 - Elec-Mech Systems

Circuit Symbol	Reference	Style
	ZENER DIODES	
Z1, Z2, Z3	1N3688A, 24 V, ±10%	862A288H01
Z4, Z6	1N3686B, 20 V, ±5%	185A212H06
Z5, Z7	N957B, 6.8 V, ±5%	186A797H06

Δ - SOLID STATE SYSTEMS
\# - ELEC-MECH SYSTEMS

Loss Of - S# 202C467G01 - Elec-Mech Systems
Potential Board - S# 202C529G01 - Solid State Systems

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	22 MFD, 35 V	184A661H16
C2	.27 MFD, 200 V DC	188A669H05
	DIODES	
D1, D2	1N645A	837A692H03
	RESISTORS	
R1, R4, R5, R16	27 K, ½W, ±2%	629A531H66
R2, R6, R9, R10, R15, R18	10 K, ½W, ±2%	629A531H56
R3, R11, R16	6.8 K, ½W, ±2%	629A531H52
R7 Δ	43 K, ½W, ±2%	629A531H71
R8	470 ohm, ½W, ±2%	629A531H24
R12	82 K, ½W, ±2%	629A531H78
R13	150 ohm, 3W, ±5%	762A679H01
R17	1 K, ½W, ±2%	629A531H32
	TRANSISTORS	
Q1, Q2, Q3, Q5	2N3417	848A851H02
Q4	2N3645	849A441H01
Q6	2N3589	837A617H01
	ZENER DIODES	
Z1	1N957B, 6.8 V, ±5%	186A797H06
Z2	1N3688A, 24 V, ±10%	862A288H01
Z3	1N3050B, 180 V.	187A936H17

Δ - INDICATES TYPICAL VALUE

ELECTRICAL PARTS LIST

Elec-Mech Interface Board - S# 202C468G01

Circuit Symbol	Reference	Style
CAPACITORS		
C1, C2	1.5 MFD, 35 V, ±5%	187A508H18
DIODES		
D1, D2, D3, D4, D5	1N645A	837A692H03
RESISTORS		
R1	27 K, $\frac{1}{2}$W, ±2%	629A531H66
R2, R5, R9, R12, R14, R15	10 K, $\frac{1}{2}$W, ±2%	629A531H56
R3 Δ	30 K, $\frac{1}{2}$W, ±2%	629A531H67
R4	22 ohm, $\frac{1}{2}$W, ±5%	187A290H09
R6	12 K, $\frac{1}{2}$W, ±2%	629A531H58
R7 Δ	12 K, $\frac{1}{2}$W, ±2%	629A531H58
R8	470 ohm, $\frac{1}{2}$W, ±2%	629A531H24
R10, R11, R13	22 K, $\frac{1}{2}$W, ±2%	629A531H64
R16	6.8 K, $\frac{1}{2}$W, ±2%	629A531H52
TRANSISTORS		
Q1, Q2, Q3, Q4, Q5	2N3417	848A851H02
ZENER DIODES		
Z1, Z2	1N957B	186A797H06

Δ - INDICATES TYPICAL VALUE

Channel Interface Board - S# 202C530G01 - TCF Int.
- S# 202C469G01 - TA3 Int.

Circuit Symbol	Reference	Style
CAPACITORS		
C1, C3, C5	.047 MFD, 200 V DC	849A437H04
C4, C6	.27 MFD, 200 V DC	188A669H05
DIODES		
D2, D3	1N645A	837A692H03

ELECTRICAL PARTS LIST

Elec-Mech Interface Board - S# 202C468G01 - (continued)

Circuit Symbol	Reference	Style
	RESISTORS	
R1, R2, R9, R10 R17, R18	4.7 K, ½W, ±2%	629A531H48
R3, R7, R11, R15 R19, R23	82 K, ½W, ±2%	629A531H78
R4, R5, R12, R13, R20, R21, R26	10 K, ½W, ±2%	629A531H56
R6, R14, R22, R27	6.8 K, ½W, ±2%	629A531H52
R16, R24	150 ohm, 3W, ±5%	762A679H01
R25	27 K, ½W, ±2%	629A531H66
	TRANSISTORS	
Q1, Q3, Q5, Q7	2N3417	848A851H02
Q2, Q4, Q6	2N3645	849A441H01
	ZENER DIODES	
Z1, Z4, Z7	1N3686B, 20 V, ±5%	185A212H06
Z2, Z5, Z8	1N957B, 6.8 V, ±5%	186A797H06
Z6, Z9, Z10	1N3688A, 24 V, ±20%	862A288H01

Channel - S# 202C471G01 - TCF
Trip Board - S# 202C472G01 - Tone

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	0.27 MFD, 200 V.	188A669H05
	DIODES	
D1	1N645A	837A692H03
	RESISTORS	
R1, R2, R5, R8, R11 R14, R17, R18, R21, R22, R25, R26, R29, R32, R33, R34, R37, R43	27 K, ½W, ±2%	629A531H66
R3, R6, R9, R12, R15, R19, R23, R27, R30, R35, R38, R39	10 K, ½W, ±2%	629A531H56
R4, R7, R10, R13, R16 R20, R24, R28, R31, R36 R40	6.8 K, ½W, ±2%	629A531H52

ELECTRICAL PARTS LIST

Channel - S# 202C471G01 - TCF - (Continued)
Trip Board - S# 202C472G01 - Tone

Circuit Symbol	Reference	Style
	RESISTORS - (continued)	
R41	82 K, ½W, ±2%	629A531H78
R42	150 ohm, 3 W, ±5%	762A679H01
	TRANSISTORS	
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11	2N3417	848A851H02
	ZENER DIODES	
Z1	1N3688A, 24 V, ±10%	862A288H01

TCF Channel
Supervision Board - S# 202C532G01

Circuit Symbol	Reference	Style
	RESISTORS	
R1, R2, R9, R22, R23, R26	27 K, ½W, ±2%	629A531H66
R3, R4, R10, R13, R24, R27	10 K, ½W, ±2%	629A531H56
R5, R11, R25, R28	6.8 K, ½W, ±2%	629A531H52
R12	1 K, ½W, ±2%	629A531H32
	TRANSISTORS	
Q1, Q4, Q8, Q9	2N3417	848A851H02
Q2	2N3645	849A441H01
Q5	2N3589	837A617H01
	ZENER DIODES	
Z1	1N3050B, 180 V.	187A936H17

ELECTRICAL PARTS LIST

Tone Channel - S# 202C474G01 - Elec-Mech Systems
Supervision Board - S# 202C533G01 - Solid State Systems

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	12 MFD, 35 V, ±10%	862A530H05
	DIODES	
D1, D2, D3	1N645A	837A692H03
	RESISTORS	
R1, R2, R3, R6, R15 R20, R23, R24, R25, R28, R29, R32	27 K, ½W, ±2%	629A531H66
R4, R7, R12, R13 R16, R19, R21, R26, R30, R33	10 K, ½W, ±2%	629A531H56
R5, R8, R14, R17, R22, R27, R31, R34	6.8 K, ½W, ±2%	629A531H52
R9 △	22 K, ½W, ±2%	629A531H64
R10 △	10 K, ½W, ±2%	629A531H56
R11	15 K, ½W, ±2%	629A531H60
R18	1 K, ½W, ±2%	629A531H32
	TRANSISTORS	
Q1, Q2, Q3, Q5, Q7 Q8, Q9, Q10	2N3417	848A851H02
Q4	2N3645	849A441H01
Q6	2N3589	837A617H01
	ZENER DIODES	
Z1	1N957B, 6.8 V, ±5%	186A797H06
Z2	1N3050B, 180 V.	187A936H17

△ - INDICATES TYPICAL VALUE

Transmitter - S# 202C534G01 - TCF Ch.
Key Board - S# 202C535G01 - Tone Ch.

	CAPACITORS	
C1, C2	0.27 MFD, 200 V DC	188A669H05

ELECTRICAL PARTS LIST

Transmitter - S# 202C534G01 - TCF Ch. - (continued)
Key Board - S# 202C535G01 - Tone Ch.

Circuit Symbol	Reference	Style
	DIODES	
D1, D2, D3, D4, D5, D6, D7	1N645A	837A692H03
	RESISTORS	
R1, R2, R3, R4, R5, R6, R7, R13	27 K, ½W, ±2%	629A531H66
R8, R9, R12, R14, R15, R20	10 K, ½W, ±2%	629A531H56
R10, R11, R16	6.8 K, ½W, ±2%	629A531H52
R17	82 K, ½W, ±2%	629A531H78
R18	150 ohm, 3 W, ±5%	762A679H01
R19	4.7 K, ½W, ±2%	629A531H48
	TRANSISTORS	
Q1, Q4	2N3417	848A851H02
Q2, Q5	2N3645	849A441H01
Q3, Q6	2N3589	837A617H01
	ZENER DIODES	
Z1, Z3	1N3688A, 24 V, ±10%	862A288H01
Z2, Z4	1N3050B, 180 V.	187A936H17

Checkback Board - S# 202C476G01

Circuit Symbol	Reference	Style
	CAPACITORS	
C1, C2, C4	150 MFD, 35 V.	849A007H01
C3	.047 MFD, 200 V DC	849A437H04
	DIODES	
D1, D2, D3, D4, D5, D6	1N645A	837A692H03
	RESISTORS	
R1, R4, R7, R8, R15, R23, R27	27 K, ½W, ±2%	629A531H66
R2, R5, R9, R12, R16, R21, R24, R28	10 K, ½W, ±2%	629A531H56

ELECTRICAL PARTS LIST

Checkback Board - S# 202C476G01 - (continued)

Circuit Symbol	Reference	Style
	RESISTOR - (continued)	
R3, R6, R17, R22, R29	6.8 K, ½W, ±2%	629A531H52
R10 Δ , R13 Δ , R25 Δ	33 K, ½W, ±2%	629A531H68
R11, R14, R26	470 ohm, ½W, ±2%	629A531H24
R18, R19	4.7 K, ½W, ±2%	629A531H48
R20	82 K, ½W, ±2%	629A531H78
	TRANSISTORS	
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	2N3417	848A851H02
	ZENER DIODES	
Z1, Z2, Z4, Z5	1N957B, 6.8 V, ±5%	186A797H06
Z3	1N3686B, 20 V, ±5%	185A212H06

Δ - INDICATES TYPICAL VALUE

Timing Board - S# 202C477G01

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	.047 MFD, 200 V	849A437H04
C2	12 MFD, 35 V, ±10%	862A530H05
C3	1.5 MFD, 35 V, ±5%	187A508H18
C4	150 MFD, 30 V, ±10%	849A007H01
C5	1.0 MFD, 35 V, ±10%	837A241H15
	DIODES	
D1, D2, D3, D4, D5	1N645A	837A692H03
	RESISTORS	
R1, R2	4.7 K, ½W, ±2%	629A531H48
R3	82 K, ½W, ±2%	629A531H78
R4, R7, R10, R13 R16, R19, R22, R25, R28, R33	10 K, ½W, ±2%	629A531H56
R5, R8, R14, R17, R23, R26, R34	6.8 K, ½W, ±2%	629A531H52
R6, R9, R15, R18, R24, R27, R31, R32, R35	27 K, ½W, ±2%	629A531H66
R11 Δ	30 K, ½W, ±2%	629A531H67

ELECTRICAL PARTS LIST

Timing Board - S# 202C477G01 - (continued)

Circuit Symbol	Reference	Style
	RESISTORS (continued)	
R12, R21, R30	470 ohm, ½W, ±2%	629A531H24
R20 Δ, R29 Δ	33 K, ½W, ±2%	629A531H68
	TRANSISTORS	
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10	2N3417	848A851H02
	ZENER DIODES	
Z1	1N3686B, 20 V, ±5%	185A212H06
Z2, Z3, Z4, Z5	1N957B, 6.8 V, ±5%	186A797H06

Δ - INDICATES TYPICAL VALUE

Arming Board - S# 202C478G01

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	22 MFD, 35 V, ±10%	184A661H16
C2	3.3 MFD, 35 V, ±5%	862A530H01
	DIODES	
D1, D2, D3, D4, D5	1N645A	837A692H03
	RESISTORS	
R1, R2, R5, R8, R9, R10, R16, R20, R23, R24, R25	27 K, ½W, ±2%	629A531H66
R3, R6, R11, R12, R18, R21, R26, R27, R32, R36	10 K, ½W, ±2%	629A531H56
R4, R7, R13, R19, R22, R28, R33	6.8 K, ½W, ±2%	629A531H52
R14	82 K, ½W, ±2%	629A531H78
R15	20 K, ½W, ±2%	629A531H63
R29, R34	1 K, ½W, ±2%	629A531H32
R30	100 ohm, ½W, ±2%	629A531H08
R31 Δ	15 K, ½W, ±2%	629A531H60
R35	12 K, ½W, ±2%	629A531H58

ELECTRICAL PARTS LIST

Arming Board - S# 202C478G01 - (continued)

Circuit Symbol	Reference	Style
	TRANSISTORS	
Q1, Q2, Q3, Q5, Q6, Q7, Q9, Q10	2N3417	848A851H02
Q4, Q8	2N3645	849A441H01

Δ - INDICATES TYPICAL VALUE

Output Board - S# 202C479G01

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	1.5 MFD, 35 V, +10%	187A508H18
C2, C4, C7	0.22 MFD, 100 V.	763A219H21
C3	3.3 MFD, 35 V, +10%	862A530H01
C6	0.047 MFD, 200 V	849A437H04
C8, C9	0.1 MFD, 200 V	188A669H03
C10	0.27 MFD, 200 V	188A669H05
	DIODES	
D1, D2, D3, D4, D5, D6, D7, D8	1N645A	837A692H03
	POTENTIOMETERS	
R1	50 K, $\frac{1}{4}$ W, +20%	629A430H01
R14	15 K, $\frac{1}{4}$ W, +20%	629A430H08
R20	1 K, $\frac{1}{4}$ W, +20%	629A430H02
	RESISTORS	
R2, R7, R9, R12, R18, R21, R23, R24, R25, R26, R30, R31, R34, R36, R37	10 K, $\frac{1}{2}$ W, +2%	629A531H56
R3	150 K, $\frac{1}{2}$W, +5%	629A531H84
R6	47 ohm, $\frac{1}{2}$W, +5%	187A290H17
R8, R35	27 K, $\frac{1}{2}$W, +2%	629A531H66
R10, R15	470 ohm, $\frac{1}{2}$W, +2%	629A531H24
R11	470 K, $\frac{1}{2}$W, +5%	184A763H91
R16, R28	4.7 K, $\frac{1}{2}$W, +2%	629A531H48
R4, R17, R19, R22, R29	22 K, $\frac{1}{2}$W, +2%	629A531H64
R5, R27, R32, R33, R38	6.8 K, $\frac{1}{2}$W, +2%	629A531H52
R39	82 K, $\frac{1}{2}$W, +2%	629A531H78
R40	150 ohm, 3W, +5%	762A679H01
R13	15 K, $\frac{1}{2}$W, +2%	629A531H60

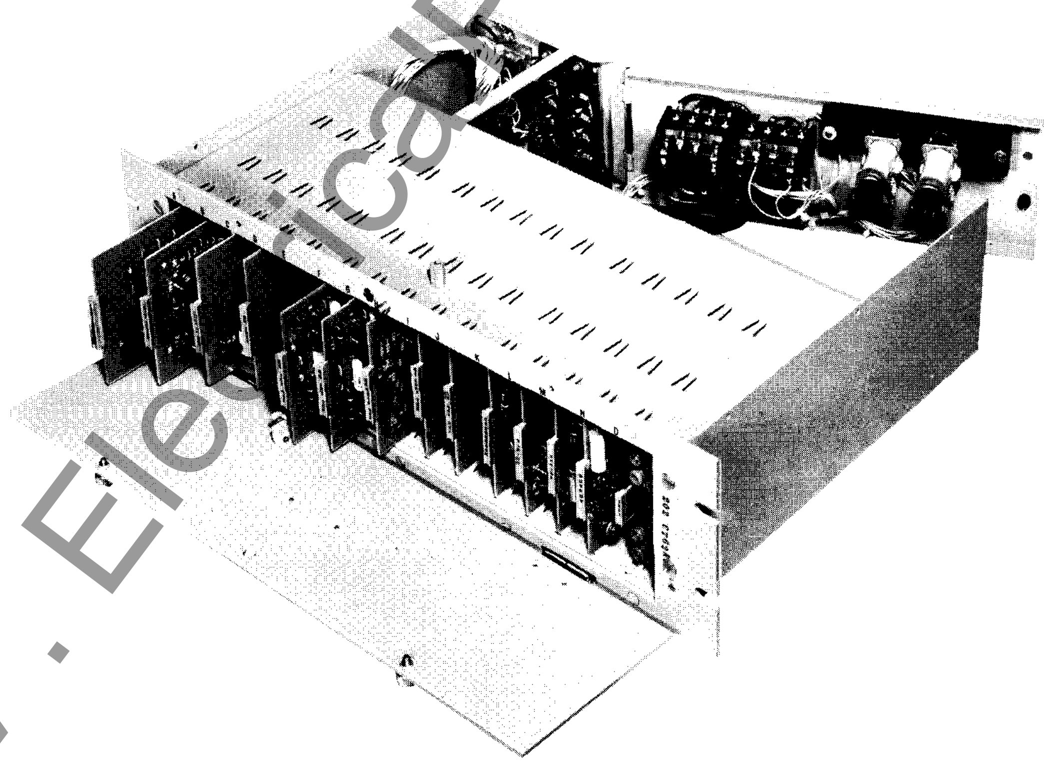
ELECTRICAL PARTS LIST

Output Board - S# 202C479G01 - (continued)

Circuit Symbol	Reference	Style
	TRANSISTORS	
Q1, Q4, Q5, Q6, Q8, Q11	2N3645	849A441H01
Q2, Q3, Q7, Q10	2N3417	848A851H02
Q9	2N3589	837A617H01
	ZENER DIODES	
Z1, Z7	1N3688A, 24 V, ±10%	862A288H01
Z2, Z3, Z4, Z5	1N957B, 6.8 V, ±5%	186A797H06
Z6	1N3050B, 180 V.	187A936H17

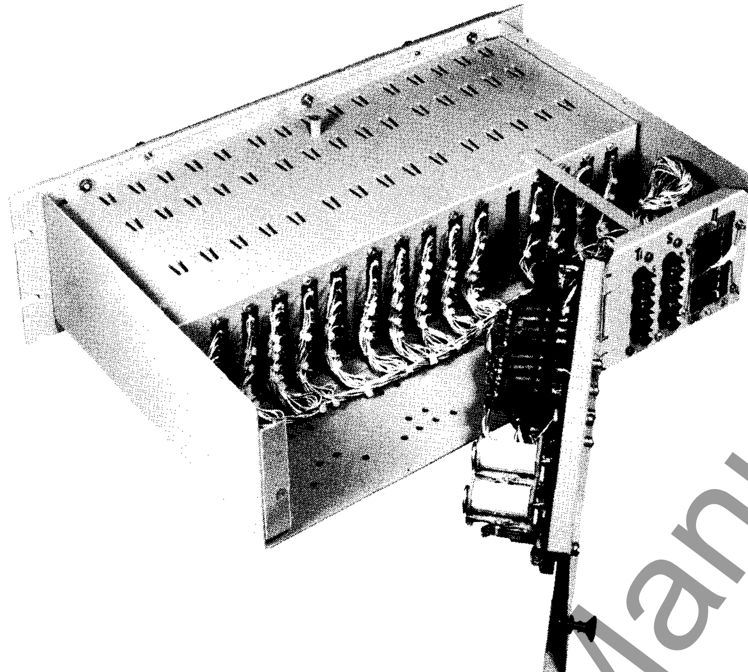
Test Board - S# 5490D87G01

Tip Jacks (Red) 1, 2, 3, 4, 5, 6, 7, 8, 9	187A332H01
Tip Jacks (Black) 10	187A332H02



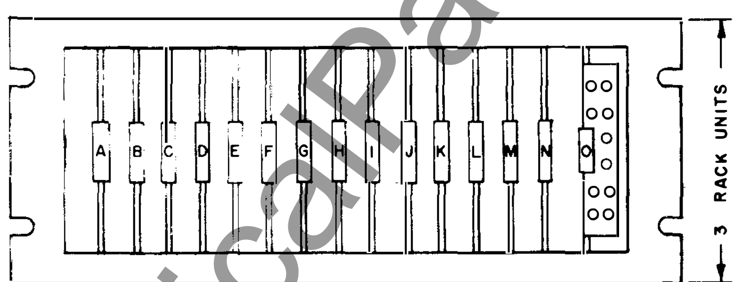
69-279

Fig. 1 Photograph (Front view with door open).



69-280

Fig. 2 Photograph (Rear view taken above relay with top cover off and door open)

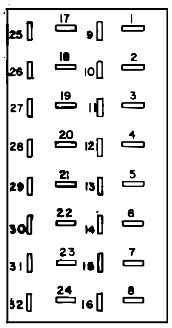


FRONT VIEW
(COVER REMOVED)

BOARD POSITION	BOARD DESCRIPTION
A	POWER SUPPLY
B	PROTECTIVE RELAY INTERFACE
C	LOSS OF POTENTIAL
D	ELEC. MECH. INTERFACE
E	———
F	CHANNEL I INTERFACE
G	CHANNEL 2 INTERFACE
H	CHANNEL TRIP
I	CHANNEL SUPERVISION
J	CHANNEL TRANSMITTER KEY
K	CHECK BACK
L	TIMING
M	ARMING
N	OUTPUT
O	TEST

876A611

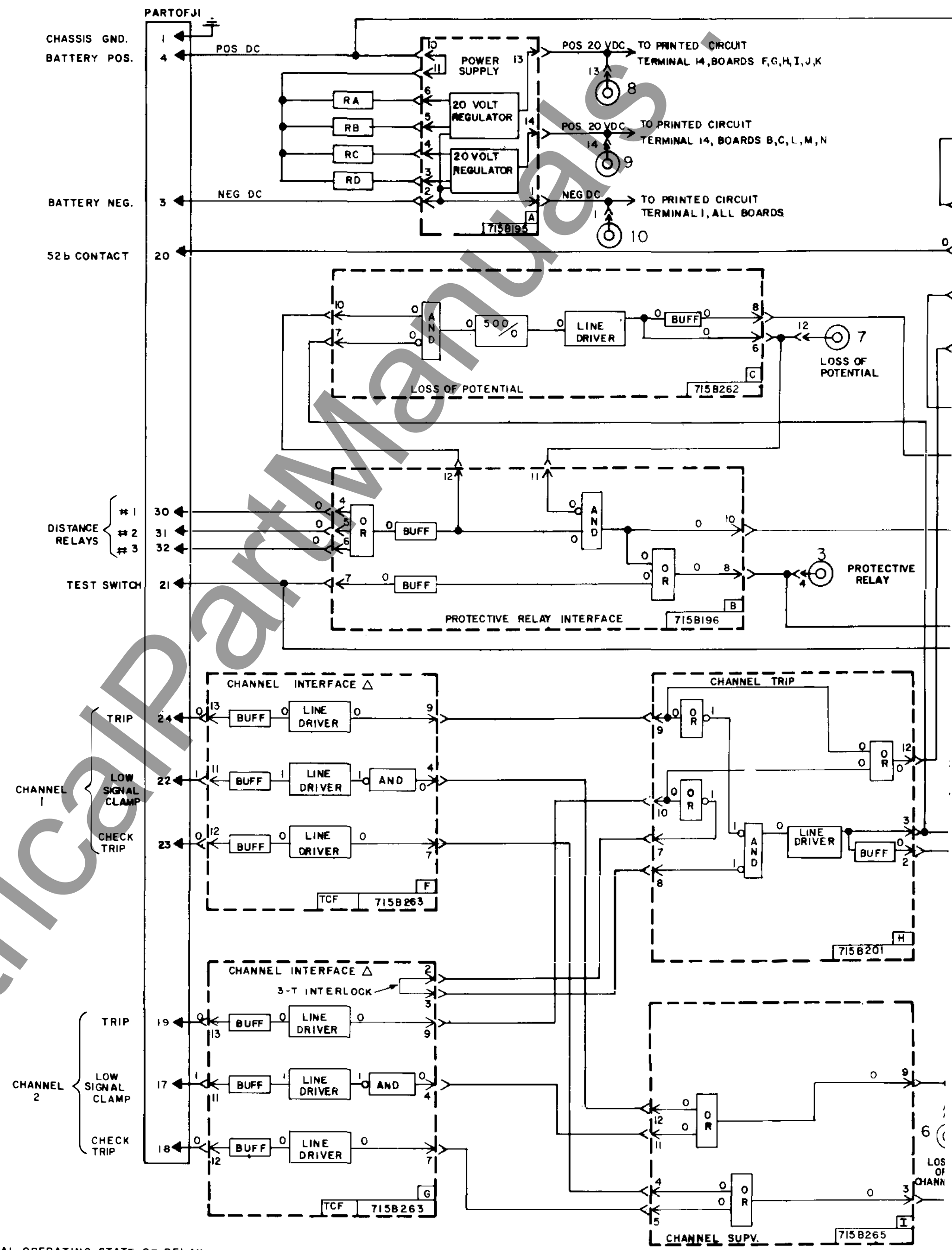
Fig. 3 Relay component Location.



CONNECTOR J1
AS VIEWED FROM
REAR OF RELAY

POWER SUPPLY RESISTORS		
VOLT	RA & RC	RB & RD
48VDC	150 OHMS S#-1267272	1800 OHMS S#-1201004
125 VDC	900 OHMS S#-1267287	5000 OHMS S#-1205214

AR RELAY	
VOLT	2M-2B CONTACTS
48VDC	S#-671B472 G11
125VDC	S#-408C845G26

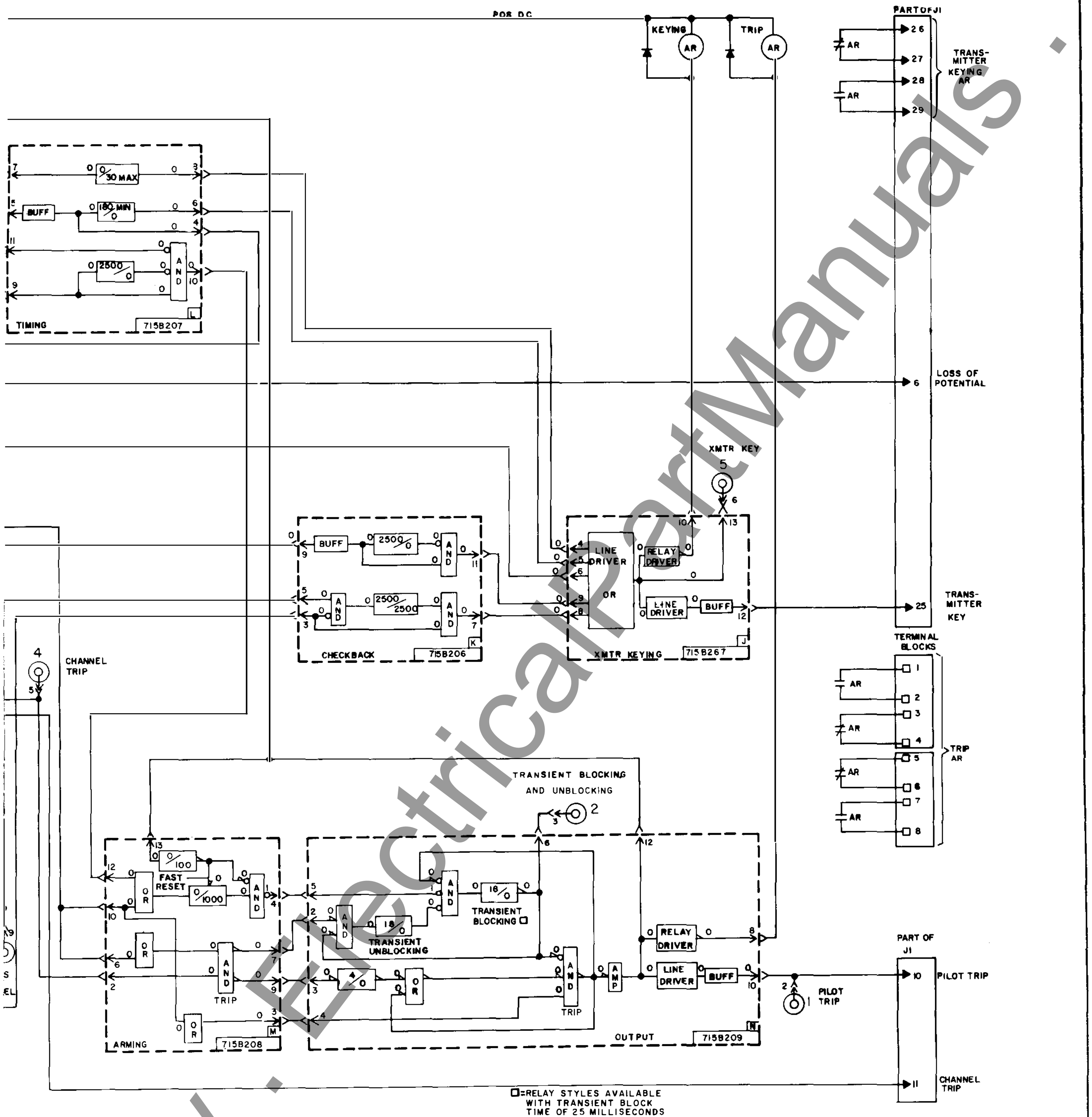


SYMBOL INDICATES POINT ON TEST BOARD (SLOT O)
SYMBOLS "O" AND "I" REPRESENT THE LOGIC VOLTAGE STATES FOR NORMAL OPERATING STATE OF RELAY

Δ FOR TWO TERMINAL LINE APPLICATIONS, CHANNEL TWO INTERFACE BOARD (SLOT G) MUST NOT BE USED IN THE RELAY

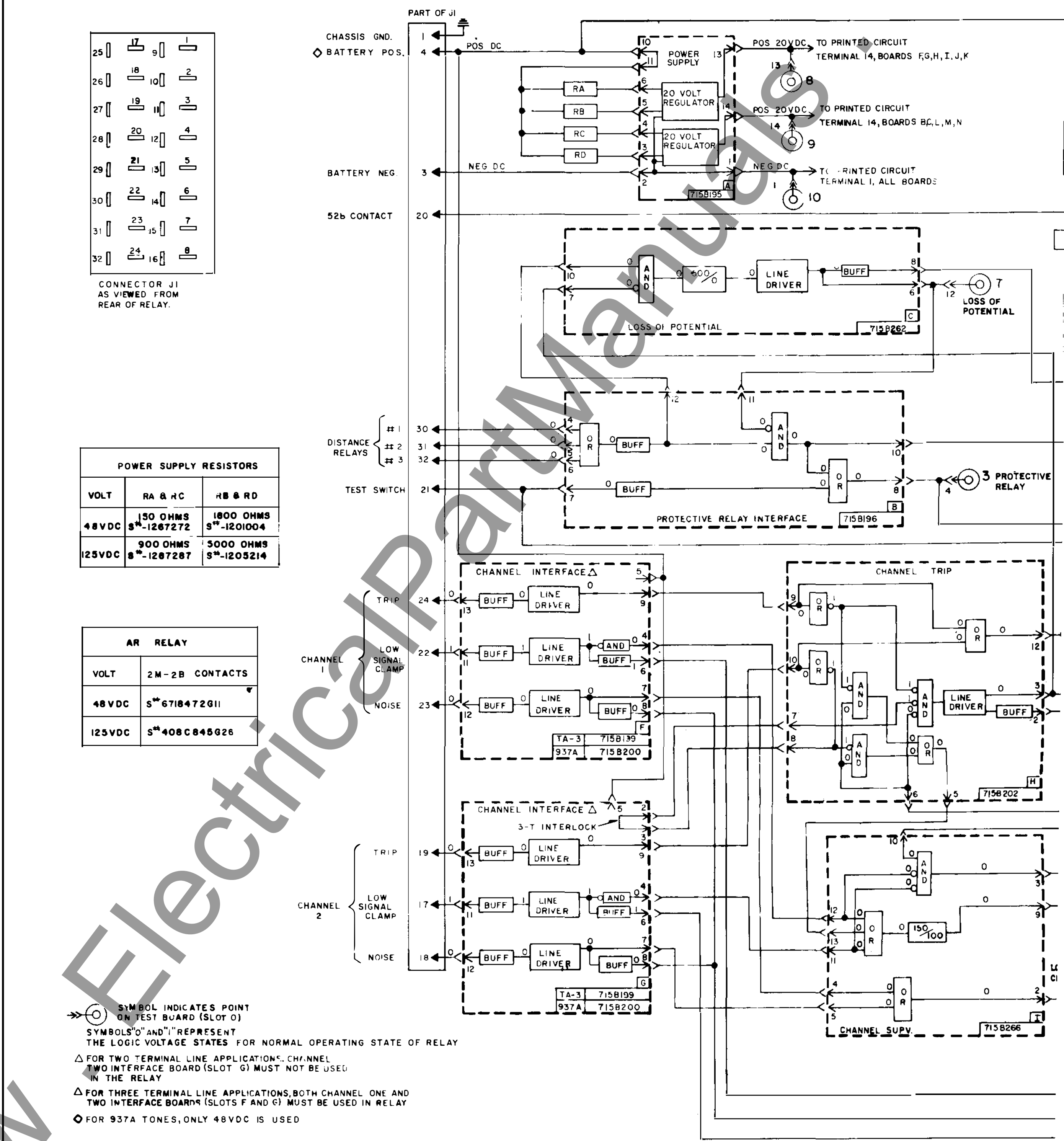
Δ FOR THREE TERMINAL LINE APPLICATIONS, BOTH CHANNEL ONE AND TWO INTERFACE BOARDS (SLOTS F AND G) MUST BE USED IN RELAY

Fig. 5 STU-12 logic - for use with solid s



5492D21

...ate distance relays and a TCF carrier channel.



POWER SUPPLY RESISTORS		
VOLT	RA & RC	RB & RD
48VDC	150 OHMS S#-1267272	1600 OHMS S#-1201004
125VDC	900 OHMS S#-1267287	5000 OHMS S#-1205214

AR RELAY	
VOLT	2M-2B CONTACTS
48VDC	S# 6718472G11
125VDC	S# 408C845G26

SYMBOL INDICATES POINT ON TEST BOARD (SLOT O)

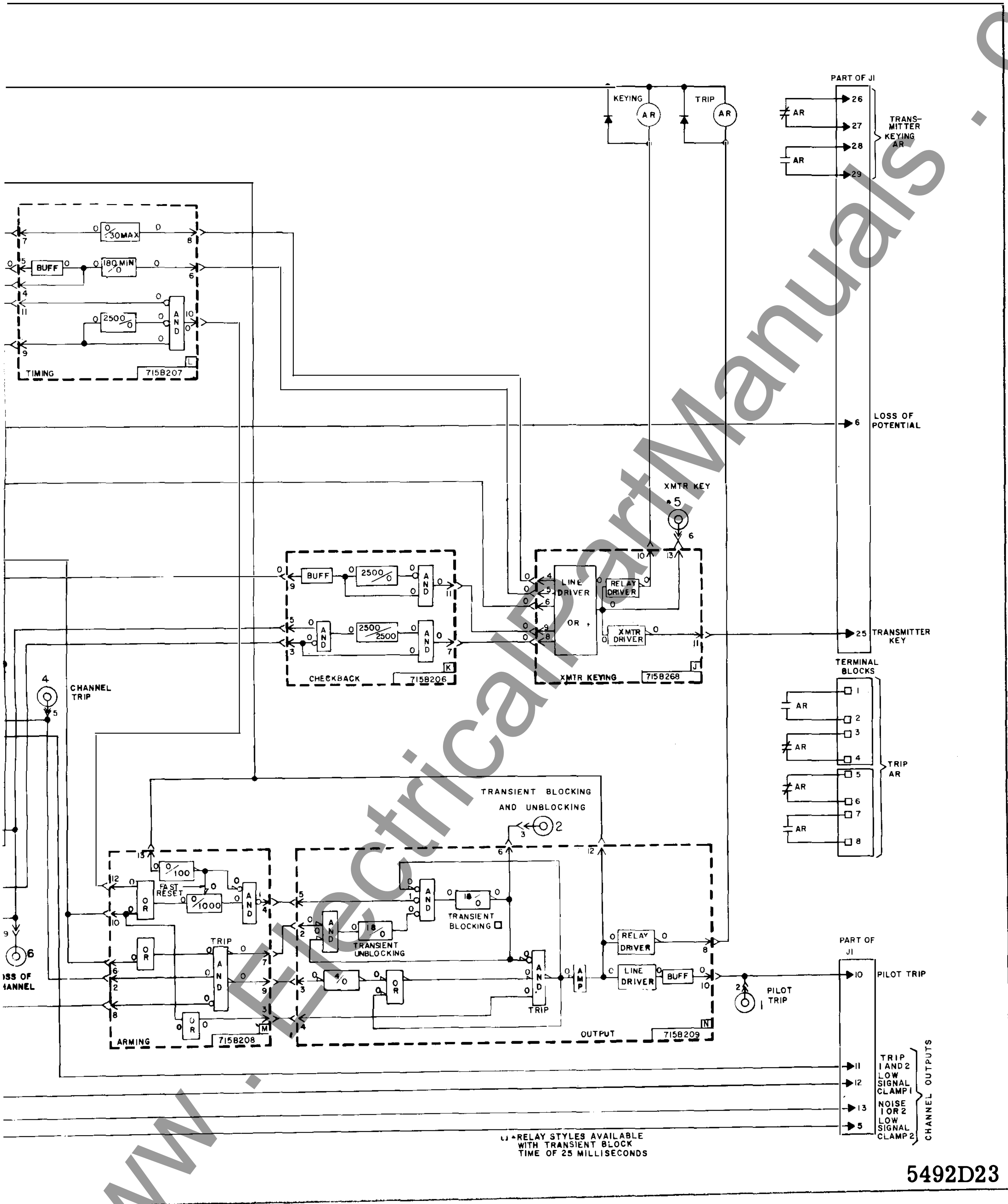
SYMBOLS "O" AND "I" REPRESENT THE LOGIC VOLTAGE STATES FOR NORMAL OPERATING STATE OF RELAY

△ FOR TWO TERMINAL LINE APPLICATIONS, CHANNEL TWO INTERFACE BOARD (SLOT G) MUST NOT BE USED IN THE RELAY

△ FOR THREE TERMINAL LINE APPLICATIONS, BOTH CHANNEL ONE AND TWO INTERFACE BOARDS (SLOTS F AND G) MUST BE USED IN RELAY

◇ FOR 937A TONES, ONLY 48VDC IS USED

Fig. 7 STU-12 logic - for use with solid



5492D23

state distance relays and a tone channel.

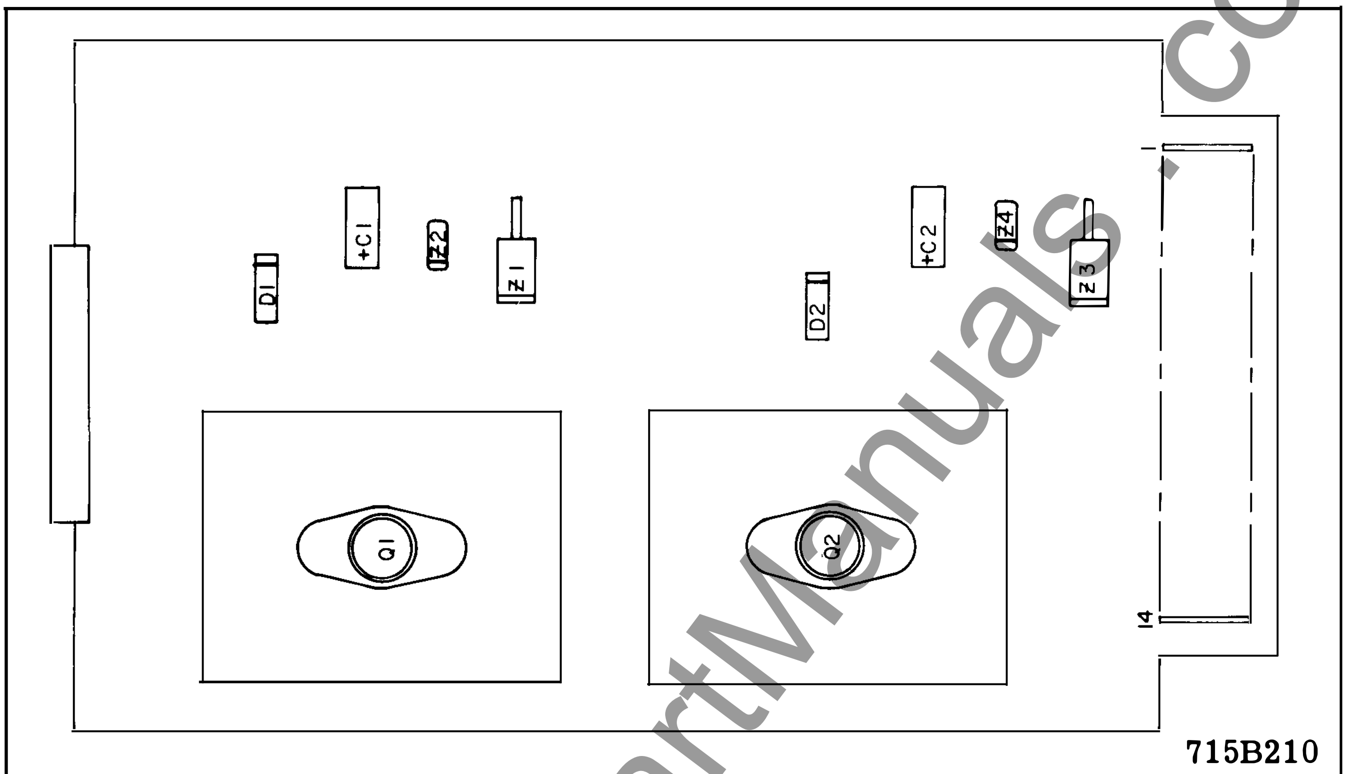


Fig. 8 Component Location Power Supply Bd.

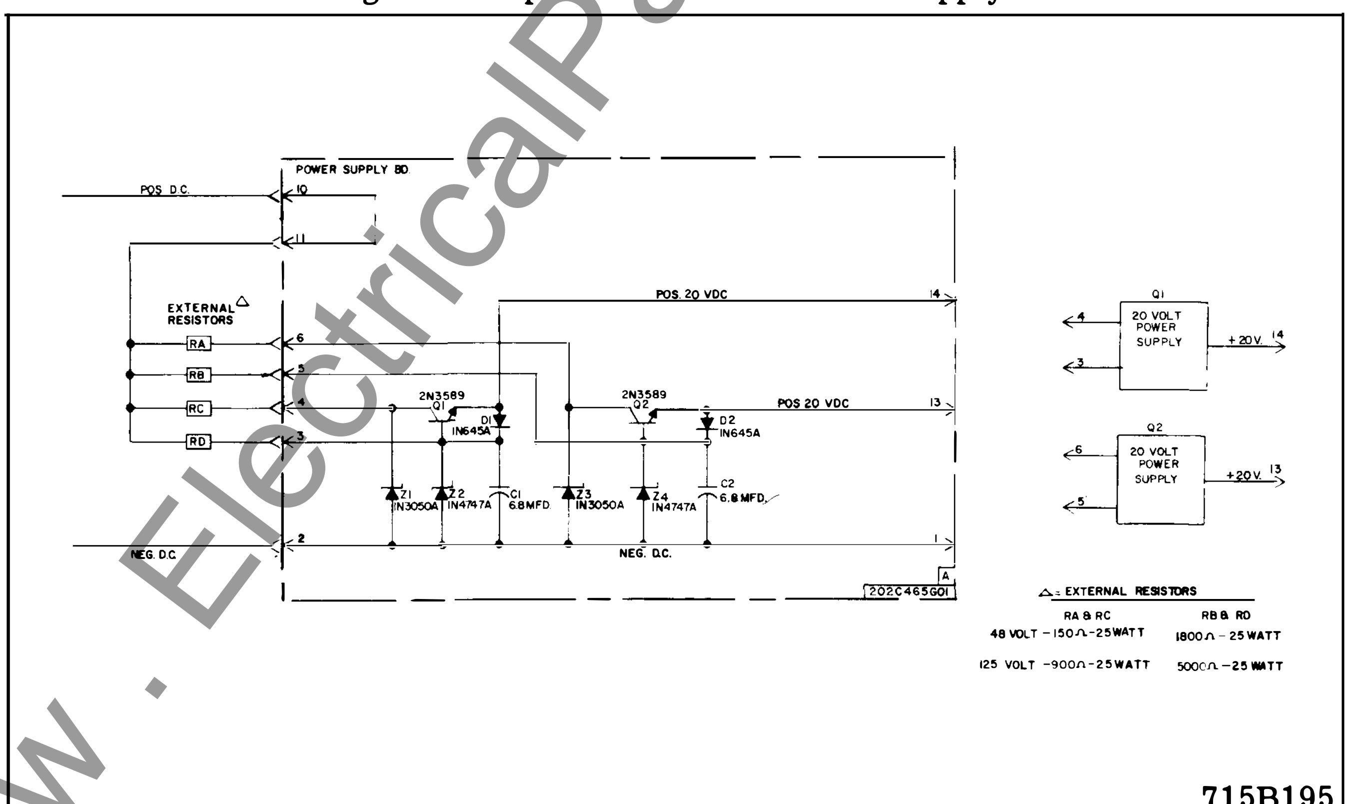


Fig. 9 Internal Schematic Power Supply Bd.

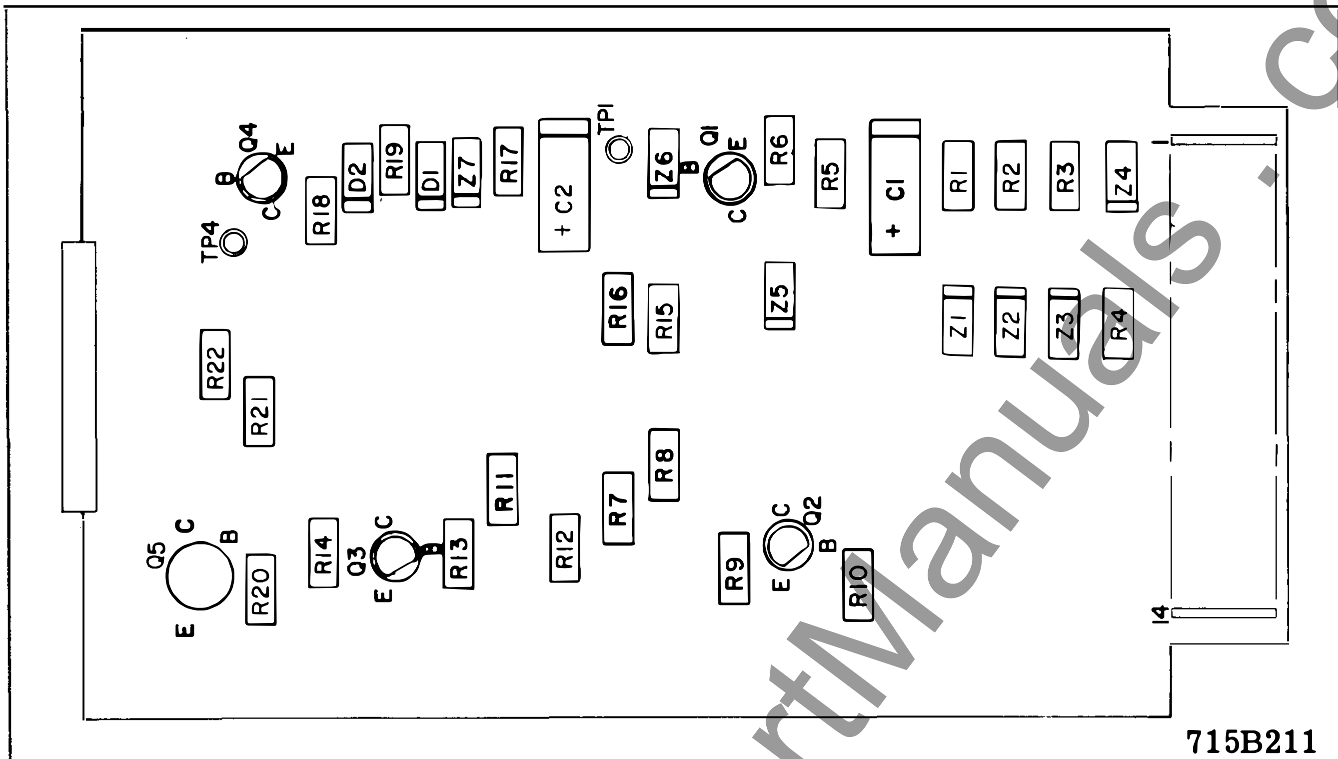


Fig. 10 Component Location Protective Relay Interface Bd.

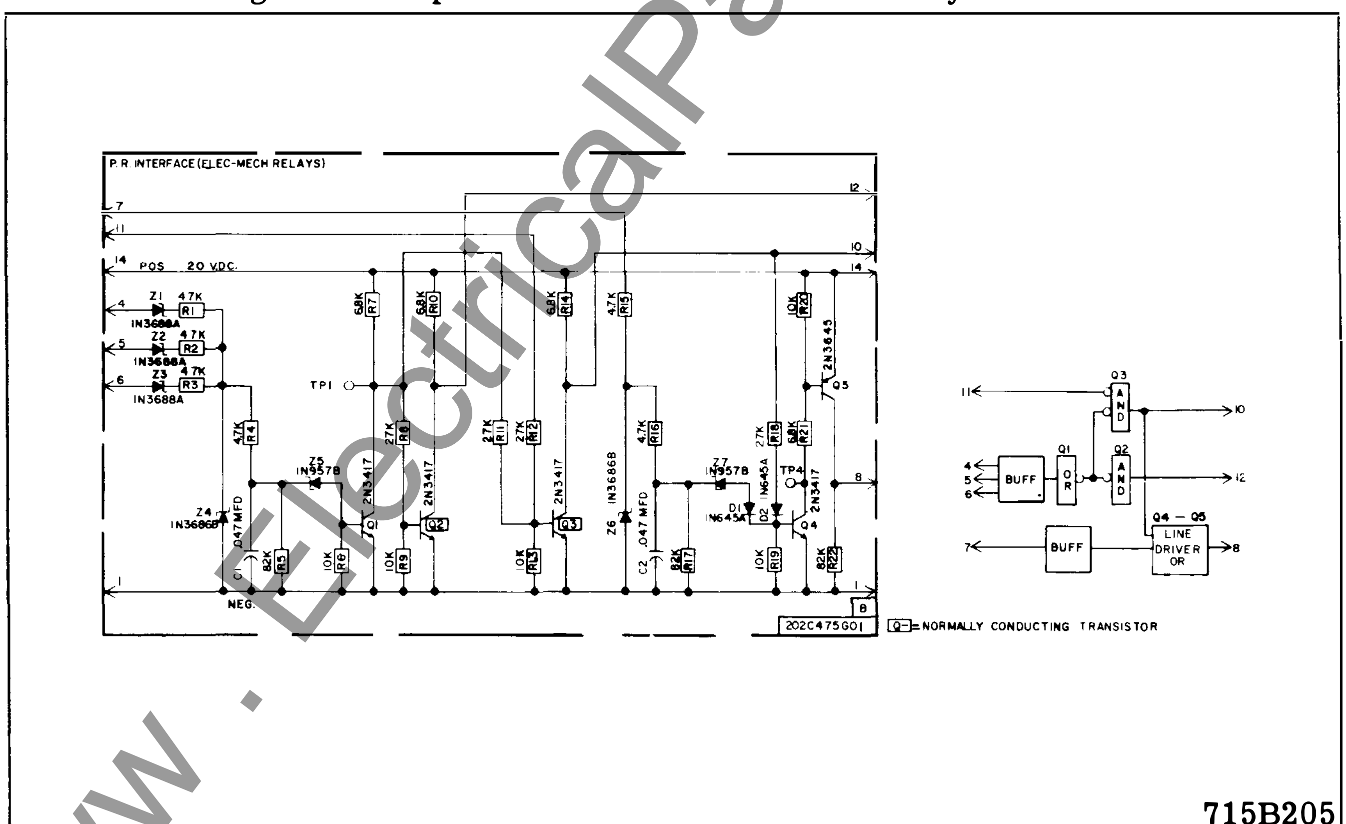


Fig. 11 Internal Schematic Protective Relay Interface Bd. for Elec.-Mech System.

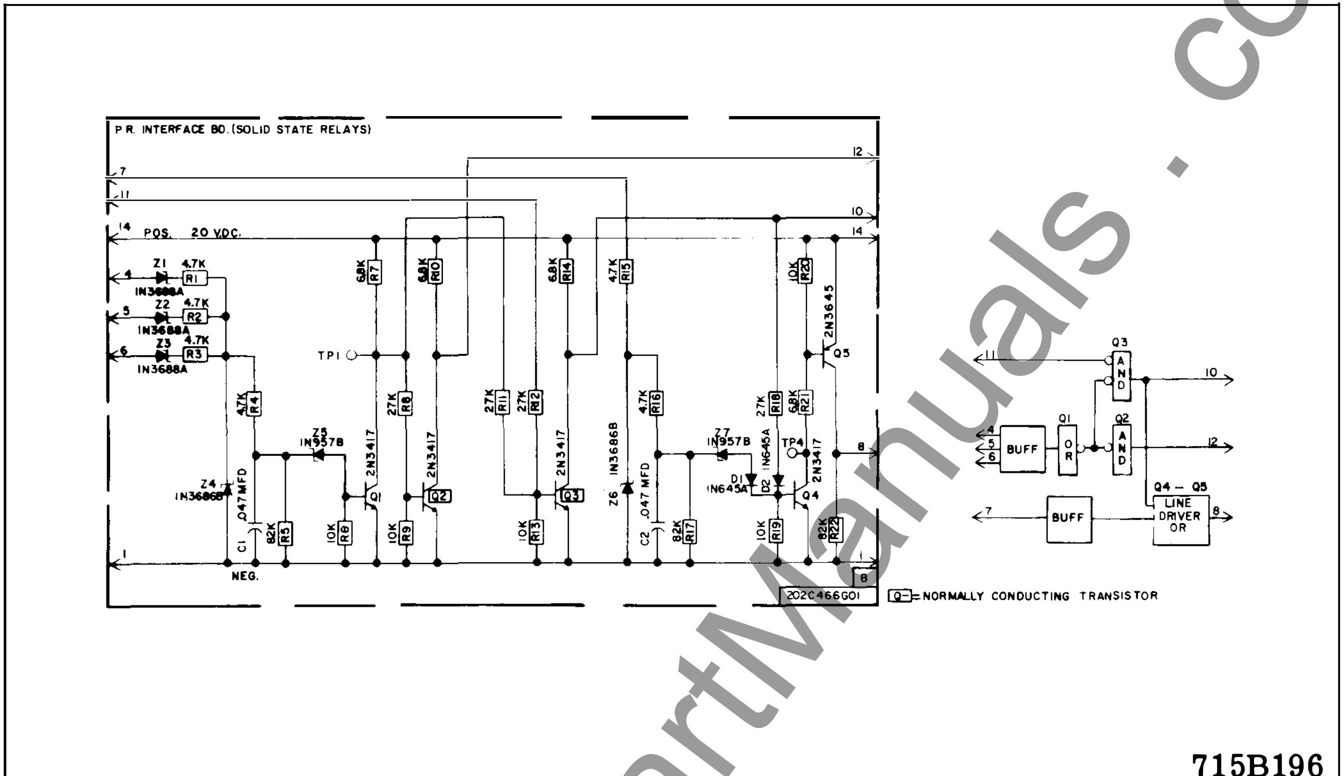


Fig. 12 Internal Schematic Protective Relay Interface Bd. for Solid State System.

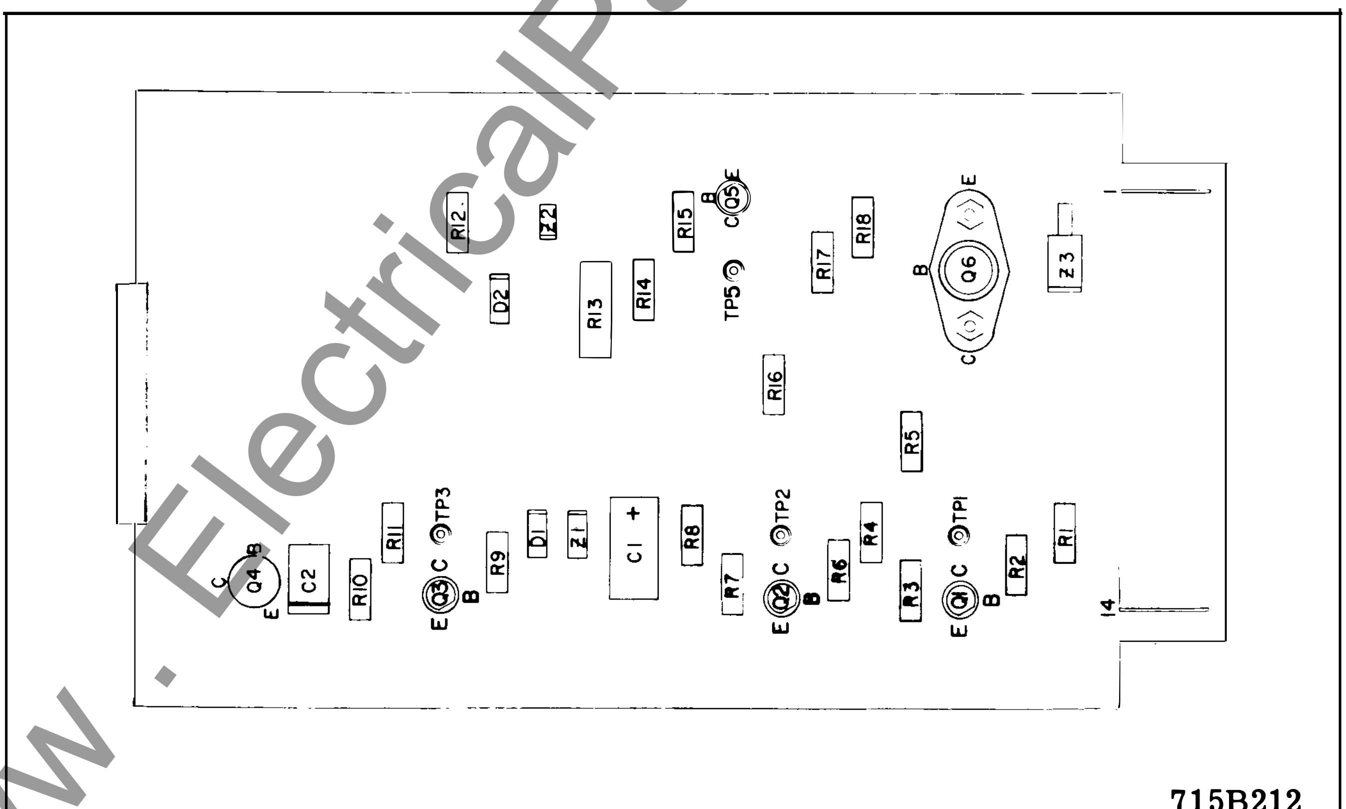


Fig. 13 Component Location Loss of Potential Bd.

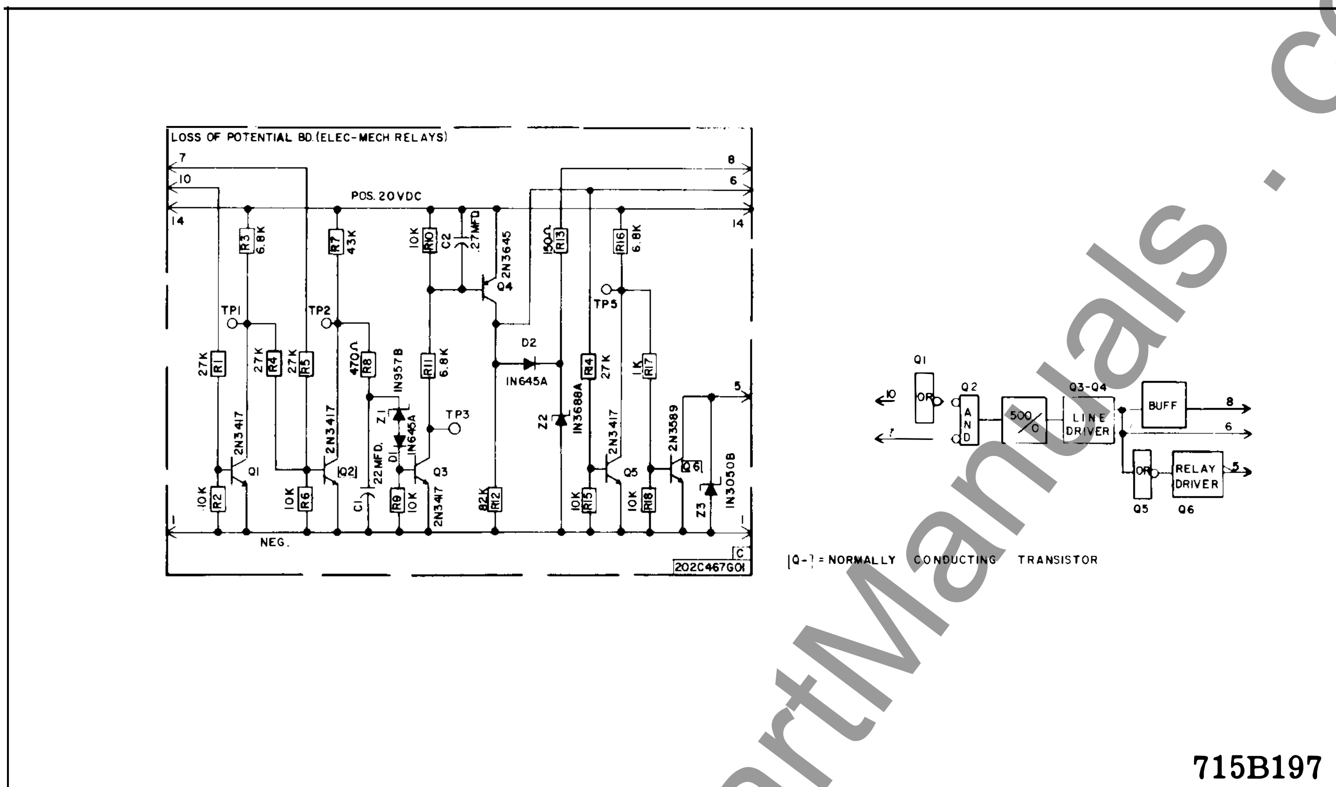


Fig. 14 Internal Schematic Loff of Potential Bd. for Elec-Mech Systems.

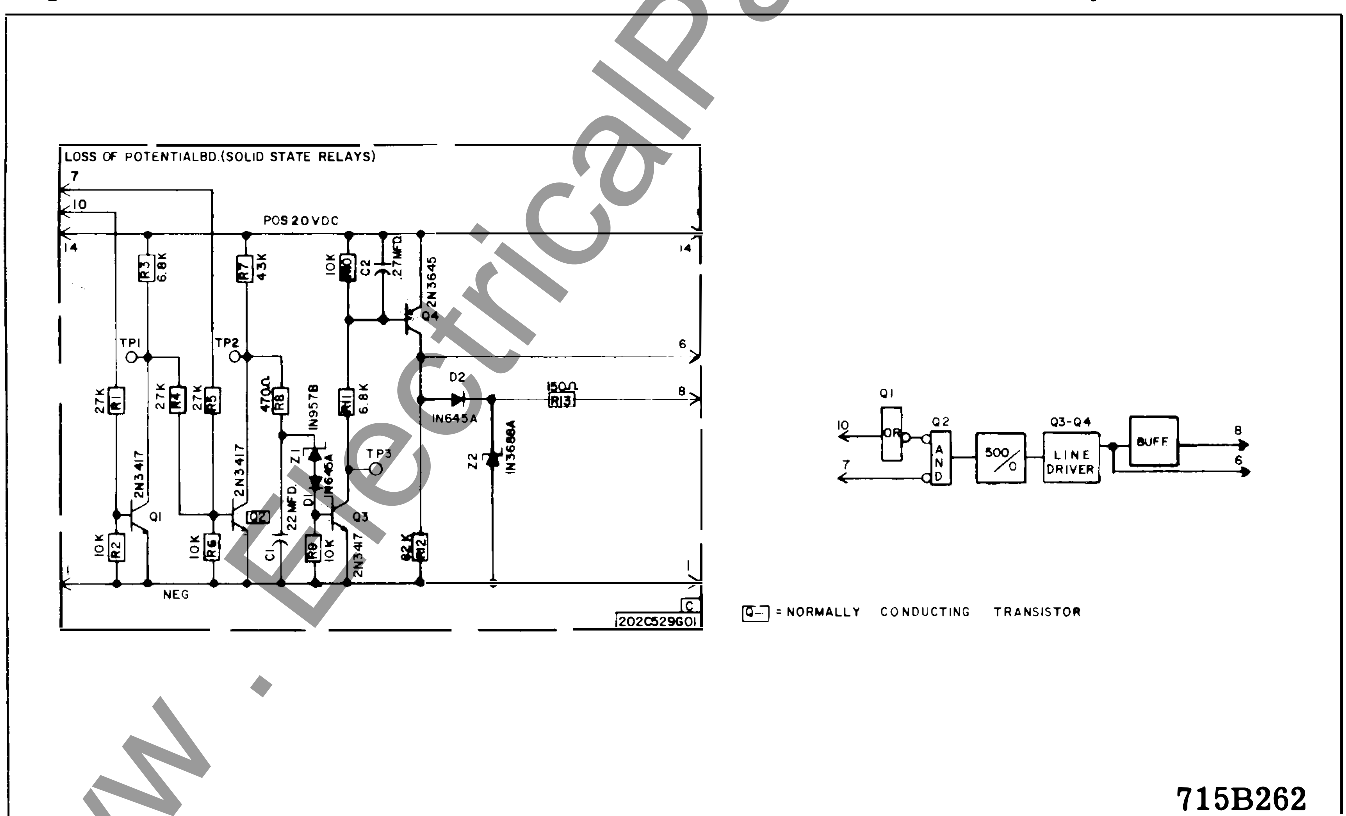


Fig. 15 Internal Schematic Loss of Potential Bd. for Solid State Systems.

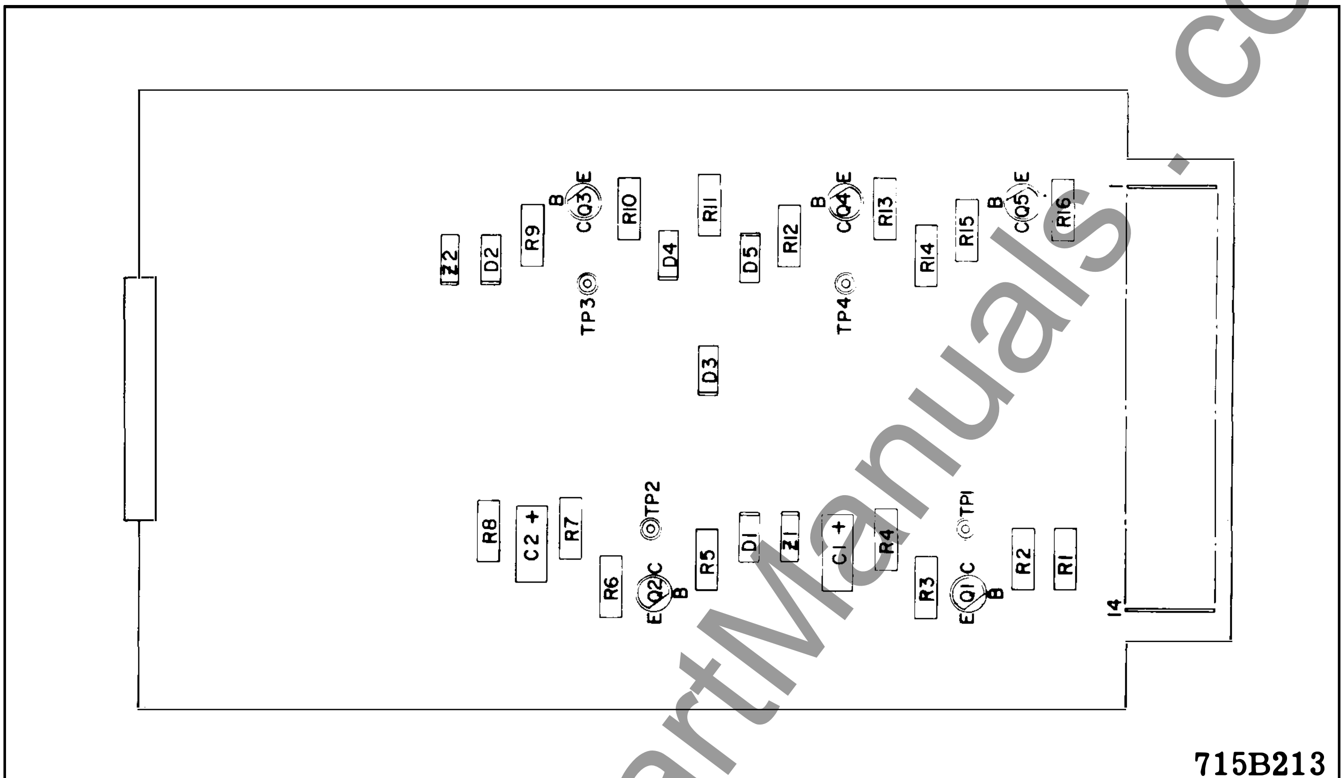


Fig. 16 Component Location Elec-Mech Interface Bd.

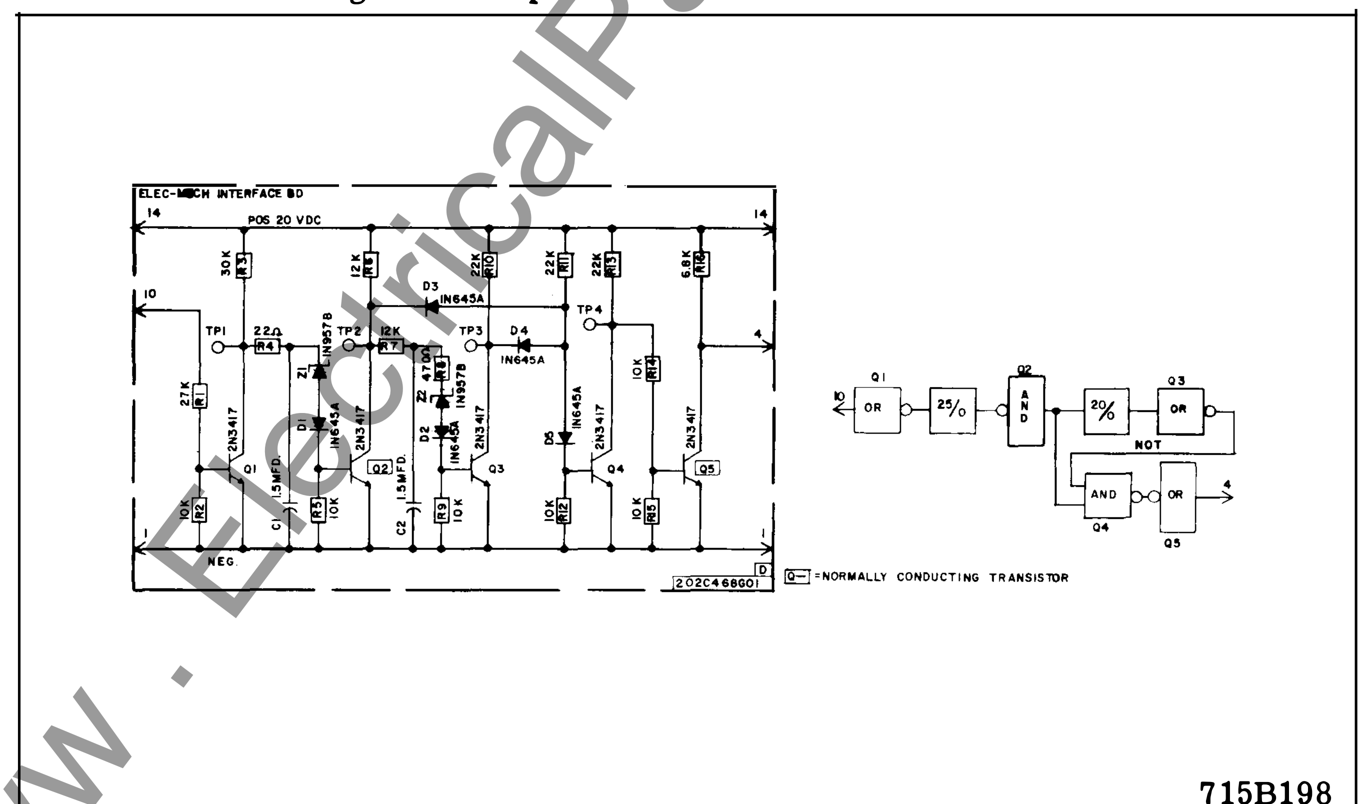


Fig. 17 Internal Schematic Elec-Mech Interface Bd.

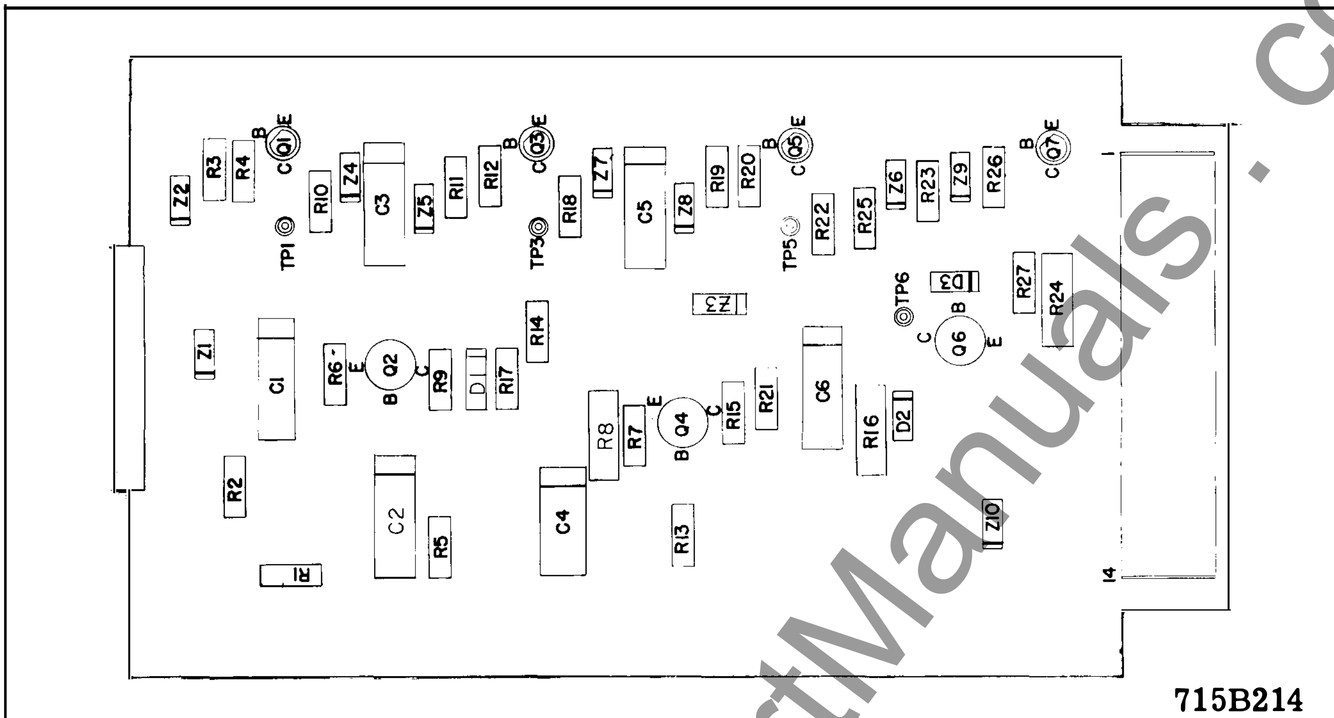


Fig. 18 Component Location Channel Interface Bd.

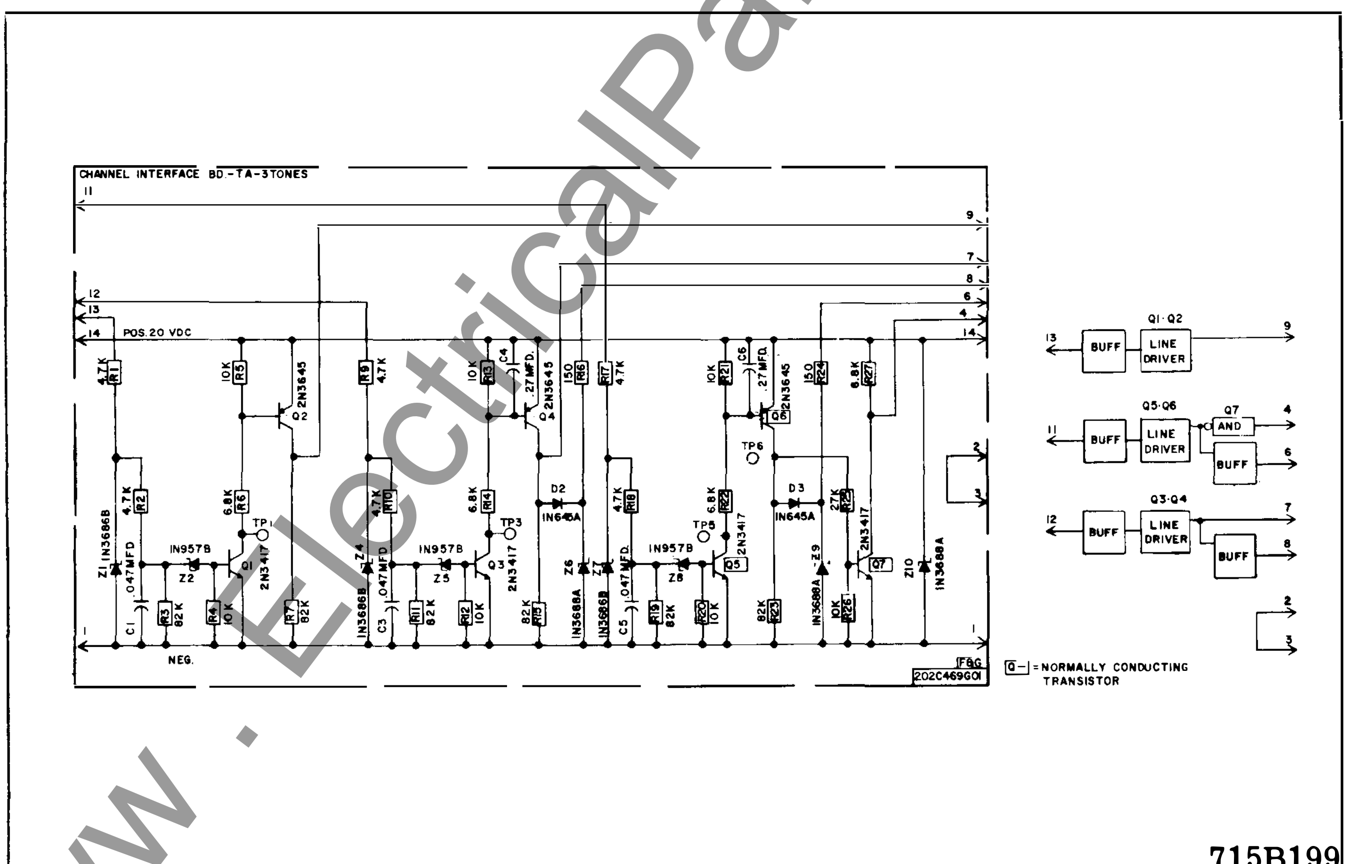


Fig. 19 Internal Schematic Channel Interface Bd. for TA-3 Tone.

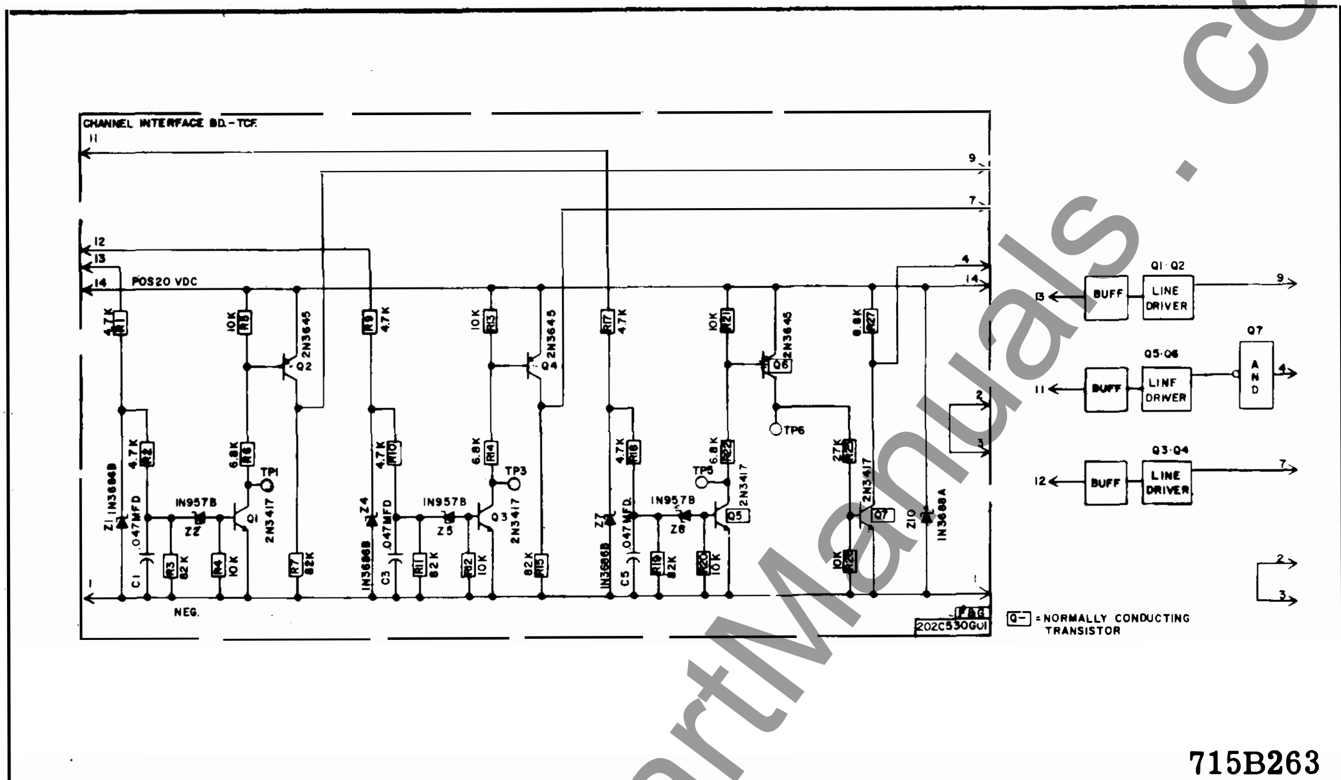


Fig. 20 Internal Schematic Channel Interface Bd. for TCF Carrier.

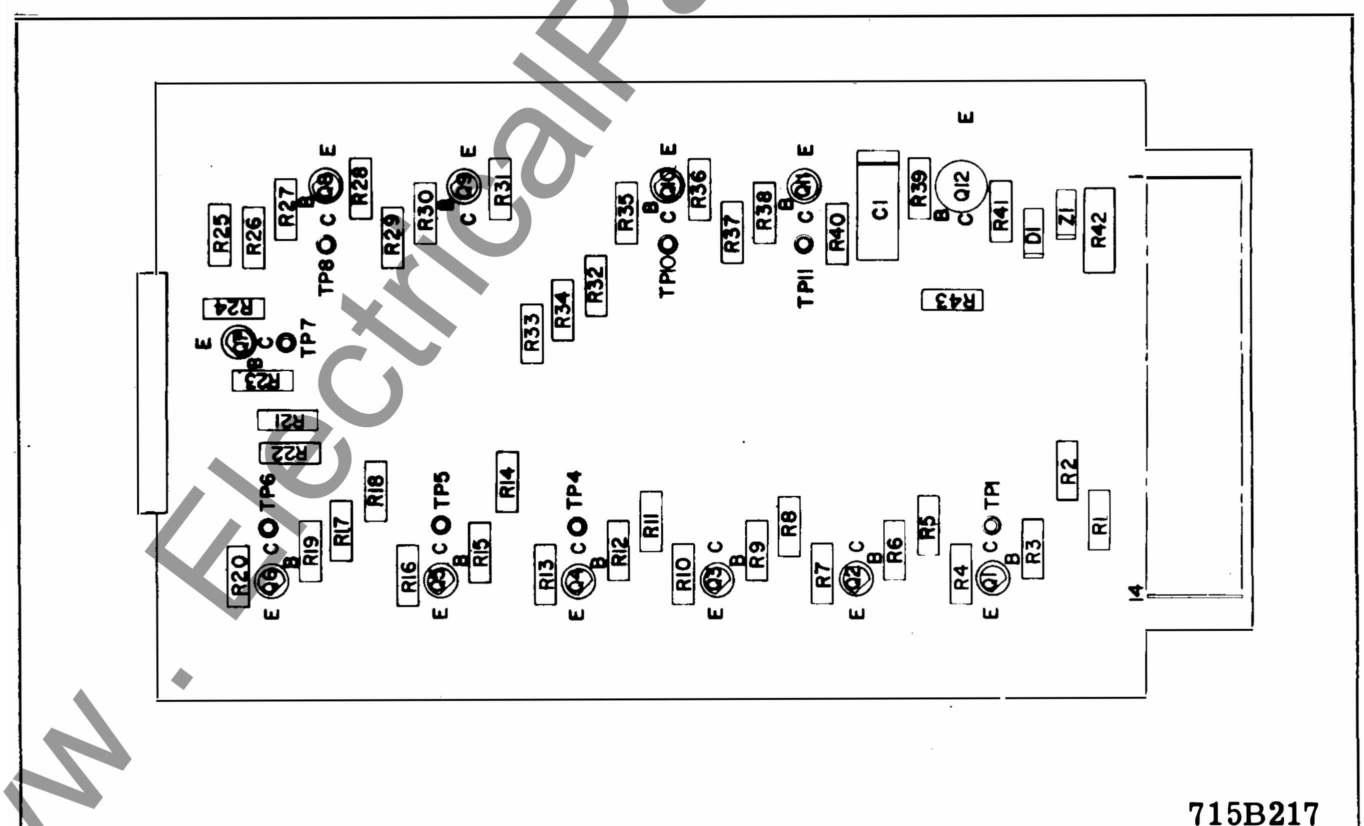


Fig. 21 Component Location Channel Trip Bd.

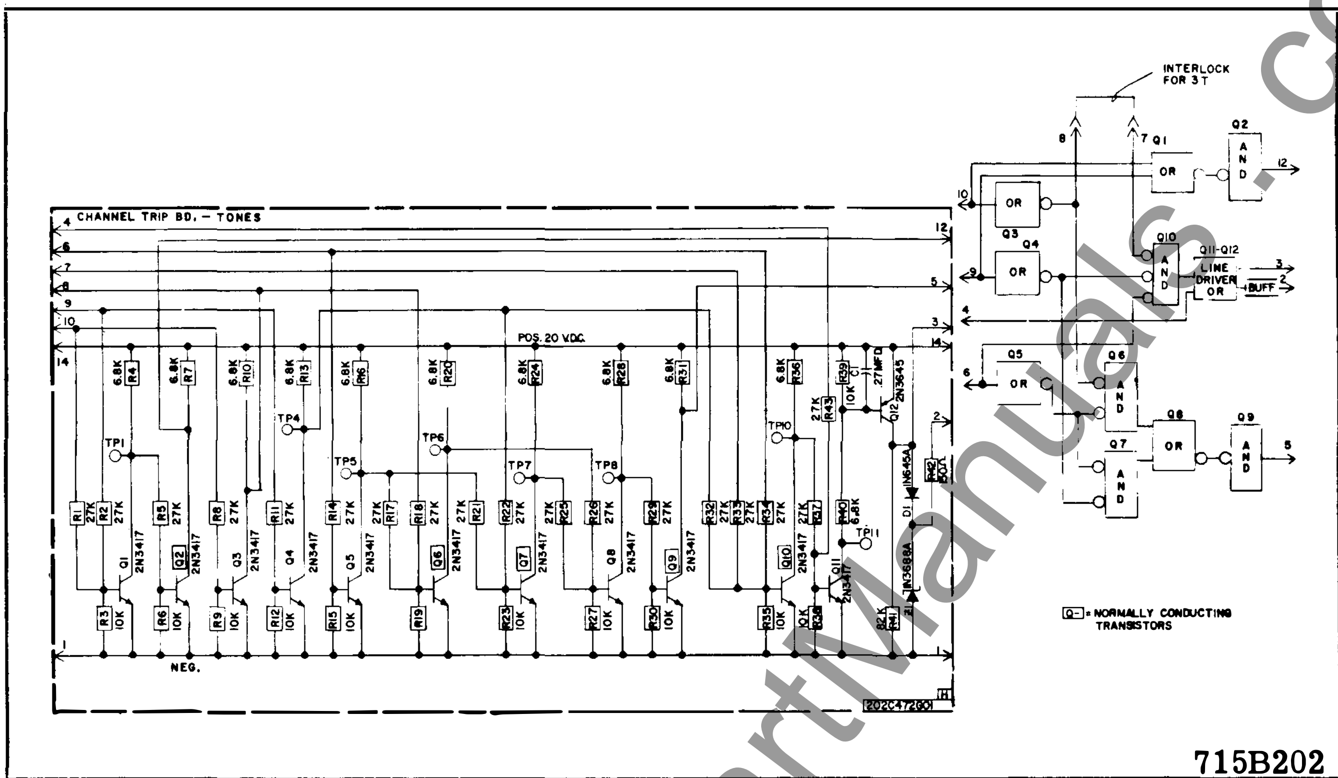


Fig. 22 Internal Schematic Channel Trip Bd. for Tones.

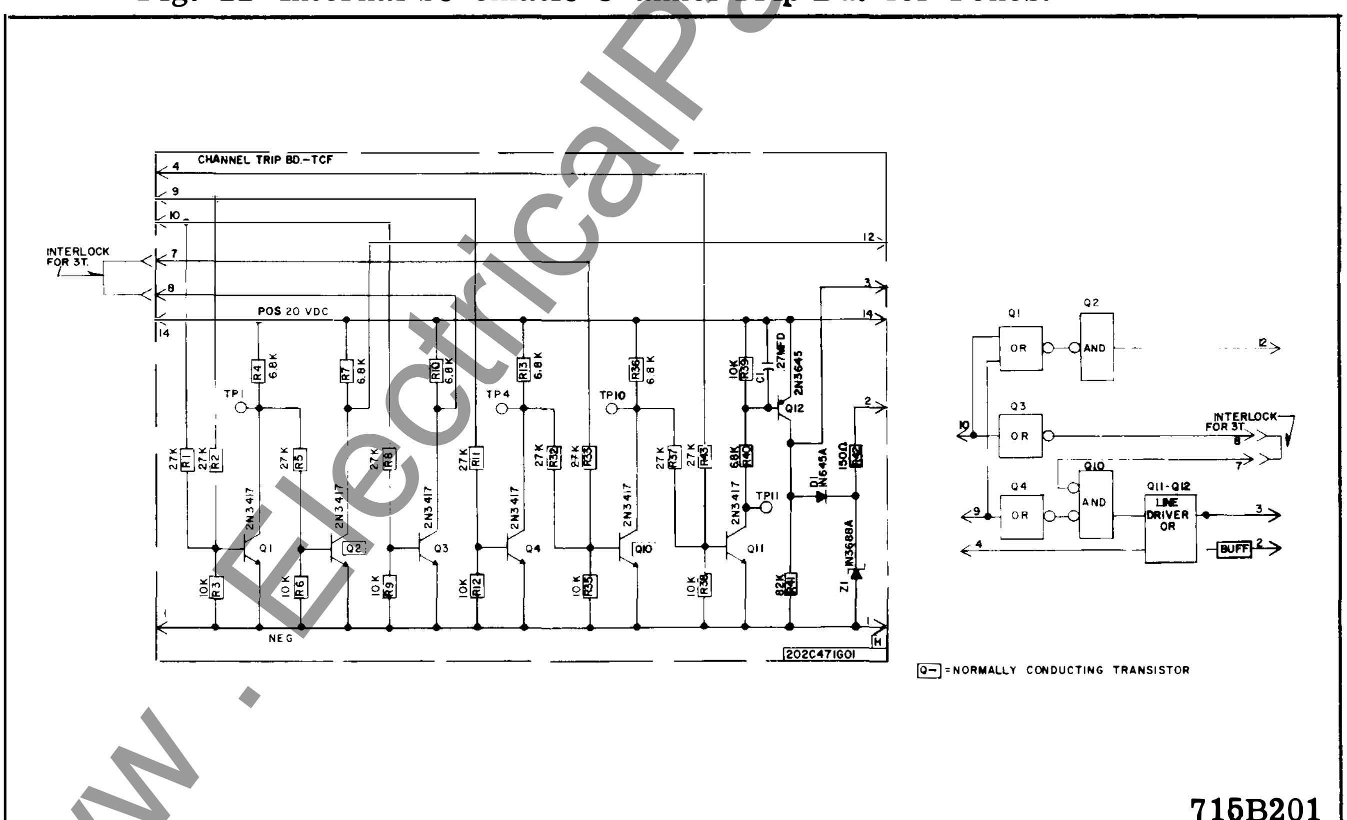


Fig. 23 Internal Schematic Channel Trip Bd. for TCF.

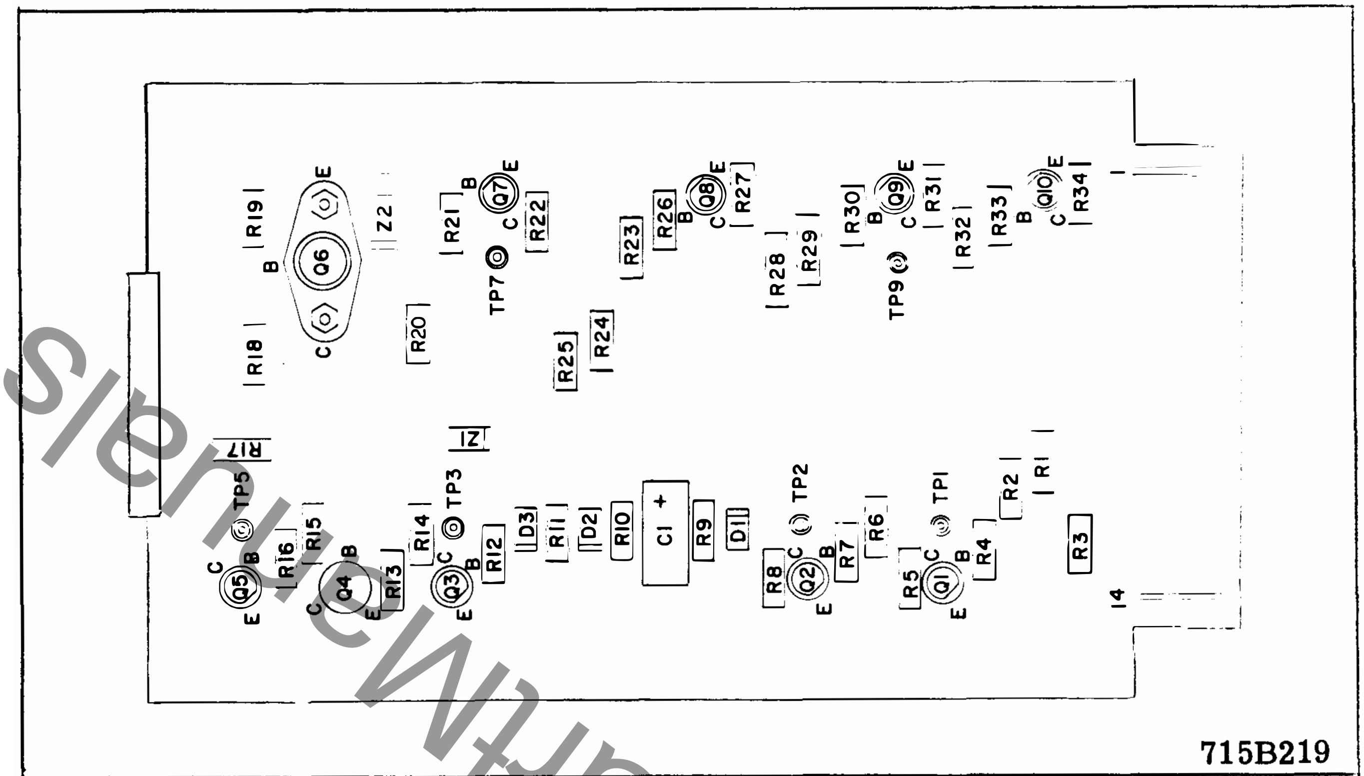


Fig. 24 Component Location Channel Supervision Bd. Tone Channel.

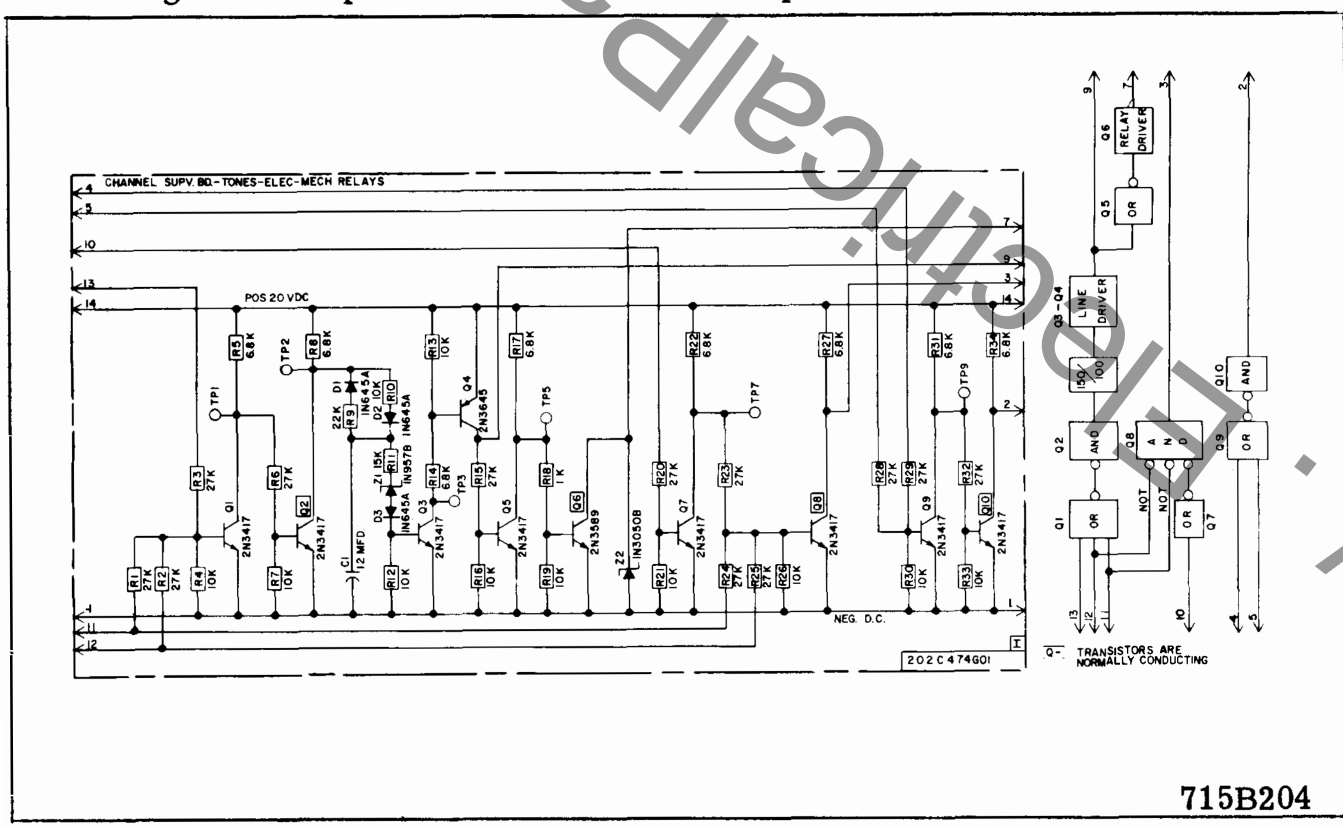


Fig. 25 Internal Schematic Channel Supv. Bd. for Tone Channel and Elec. Mech. System.

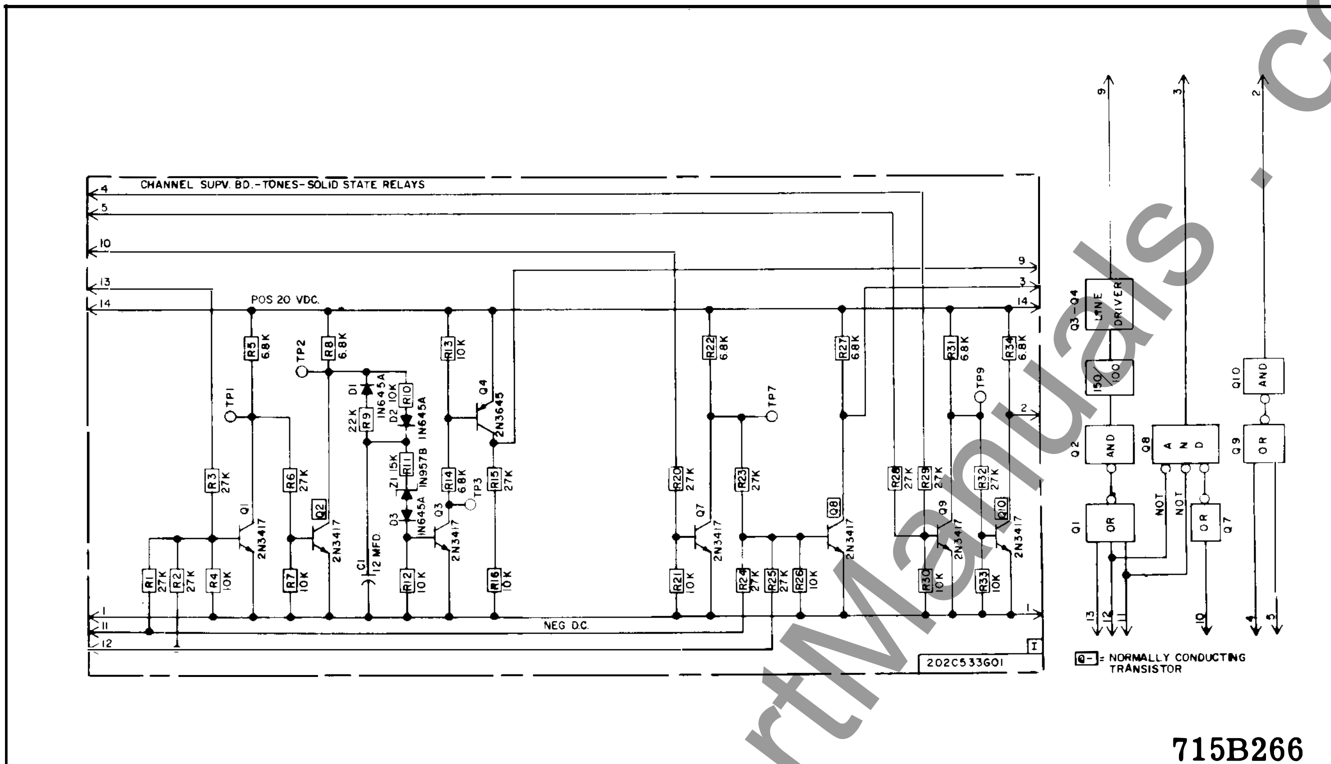


Fig. 26 Internal Schematic Channel Supv. Bd. for Tone Channel and Solid State System

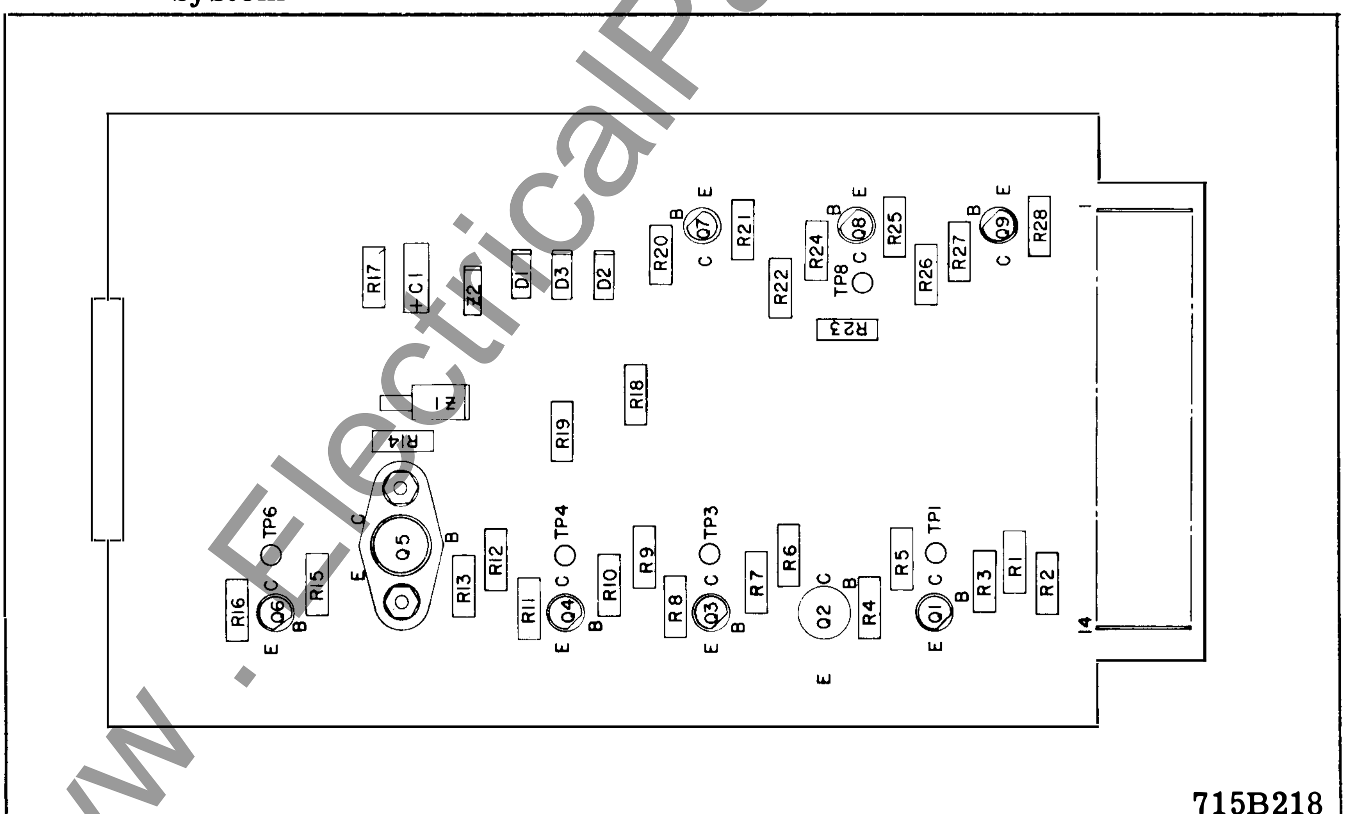


Fig. 27 Component Location Channel Supervision Bd. TCF Channel.

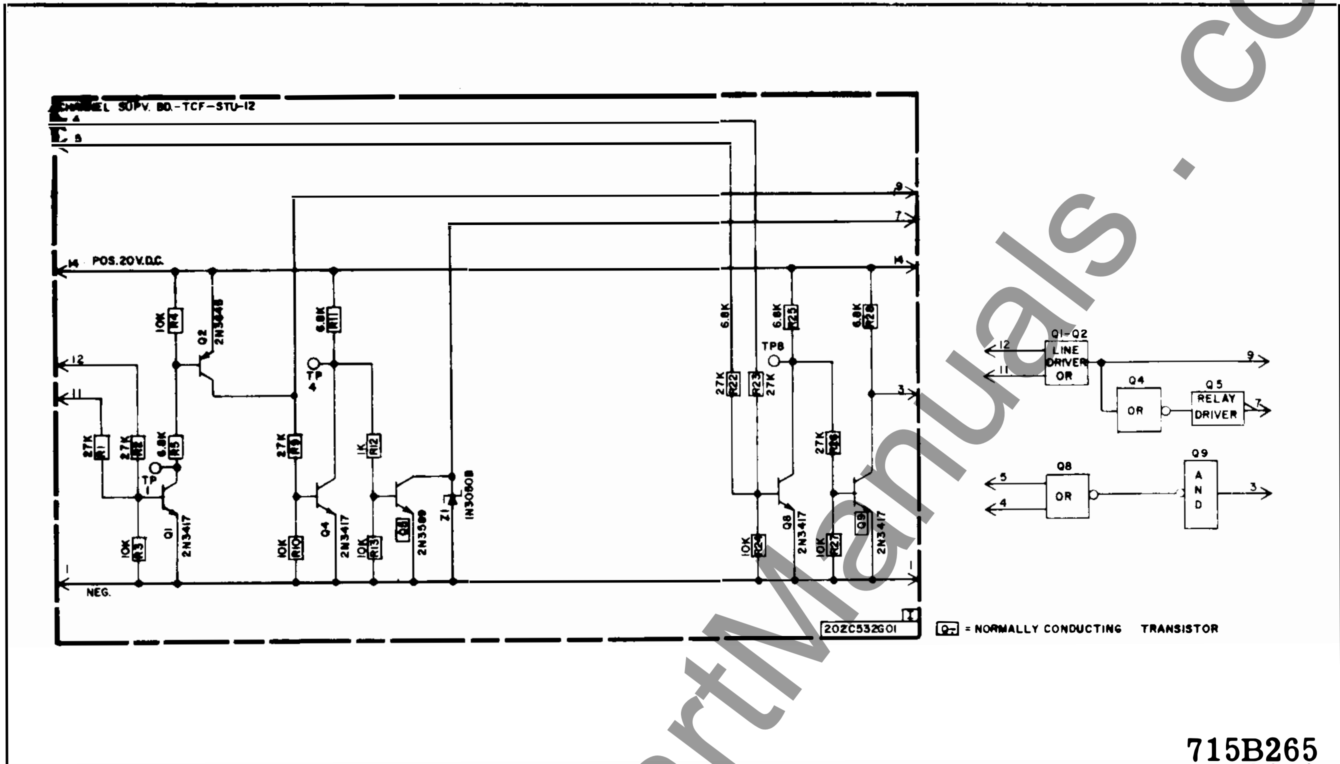


Fig. 28 Internal Schematic Channel Supv. Bd. for TCF Channel.

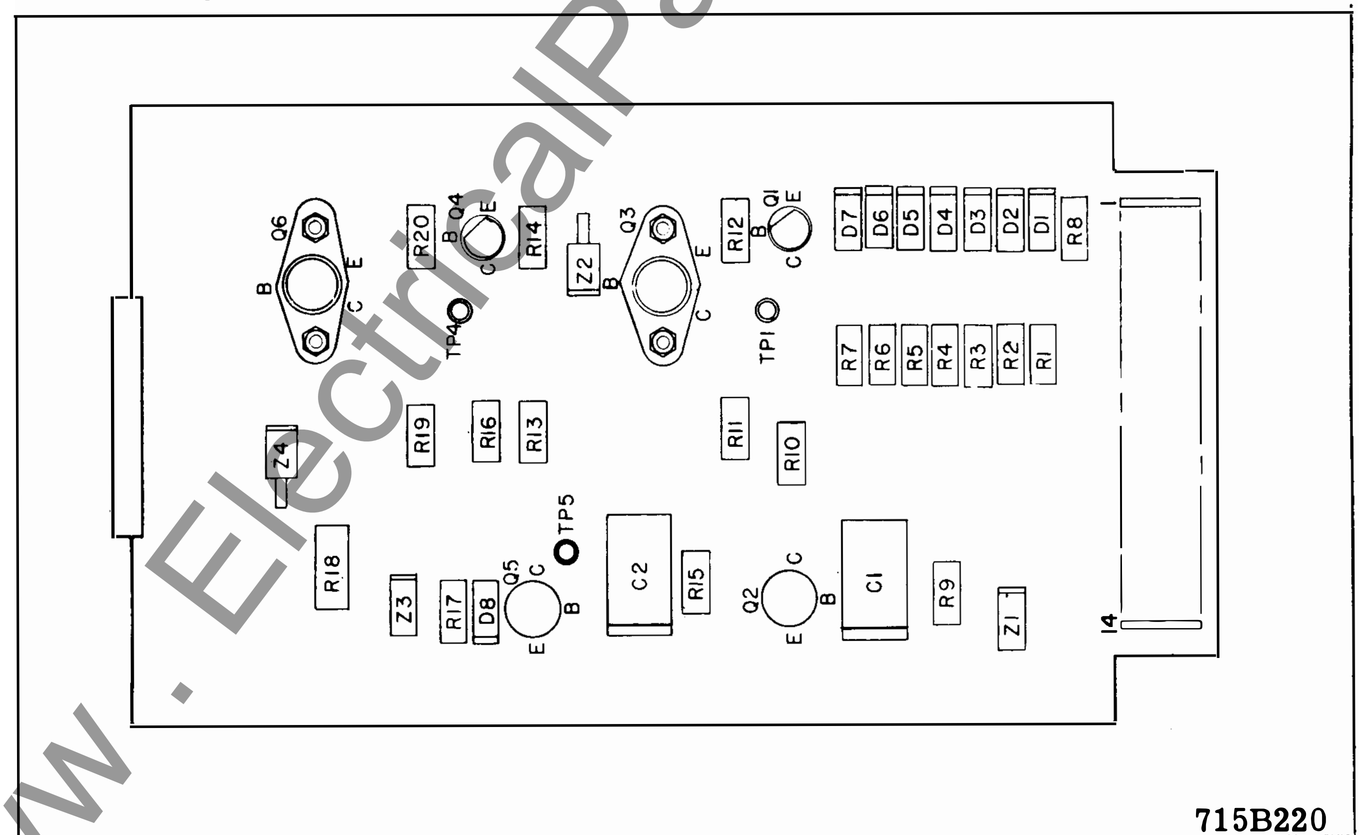
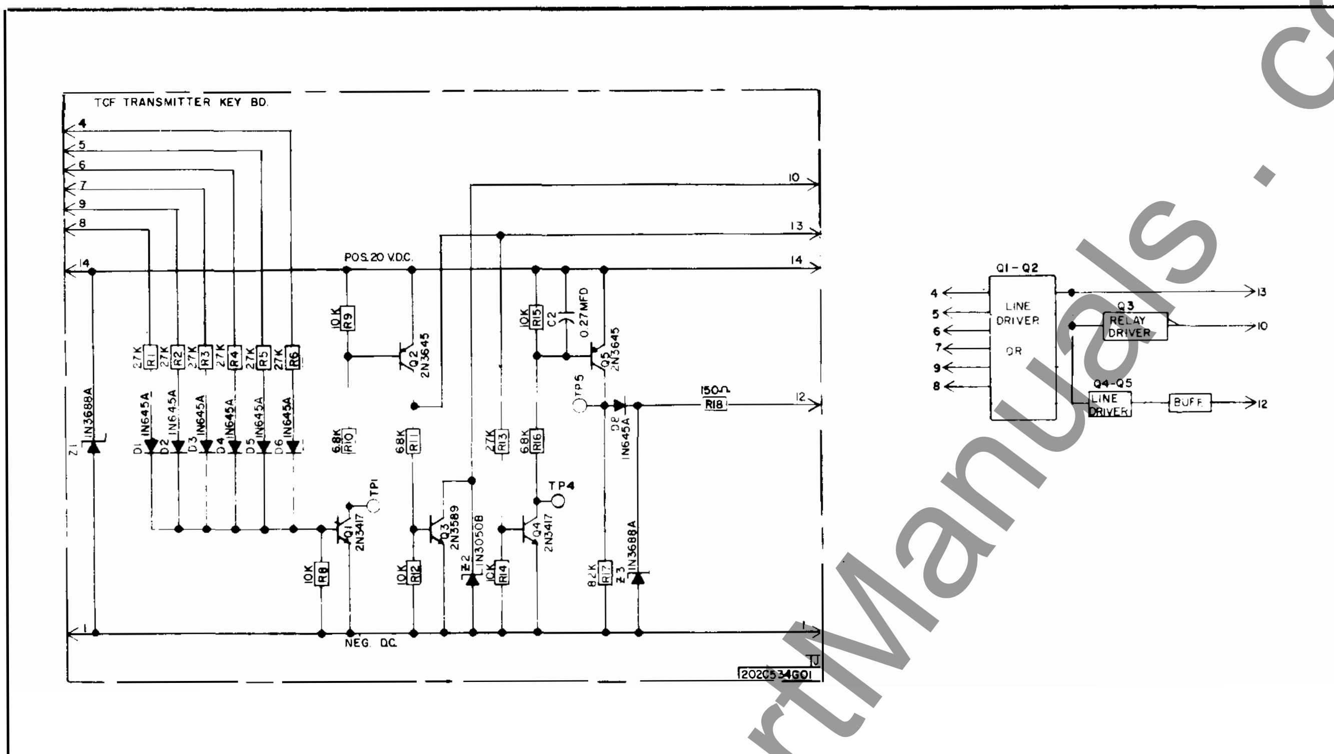
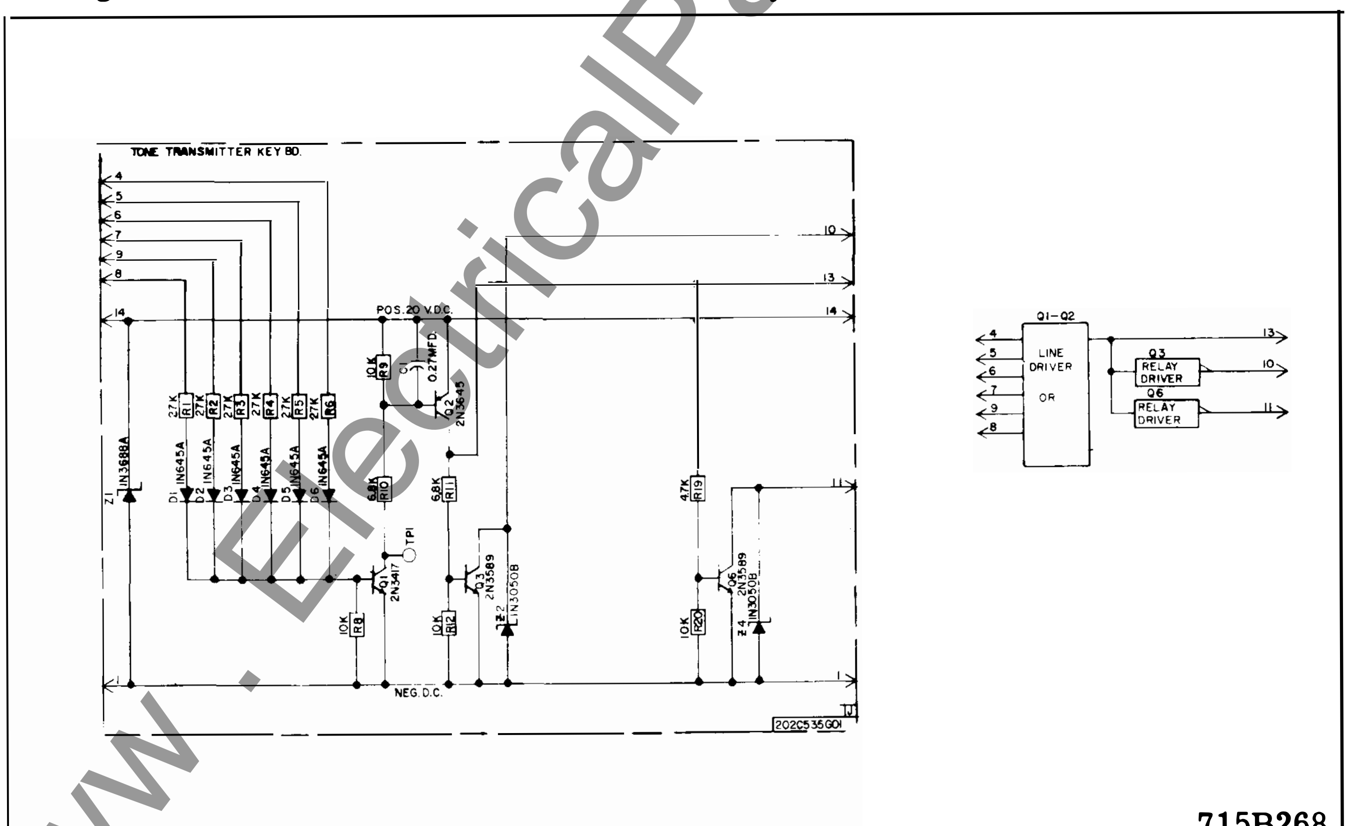


Fig. 29 Component Location Transmitter Key Bd.



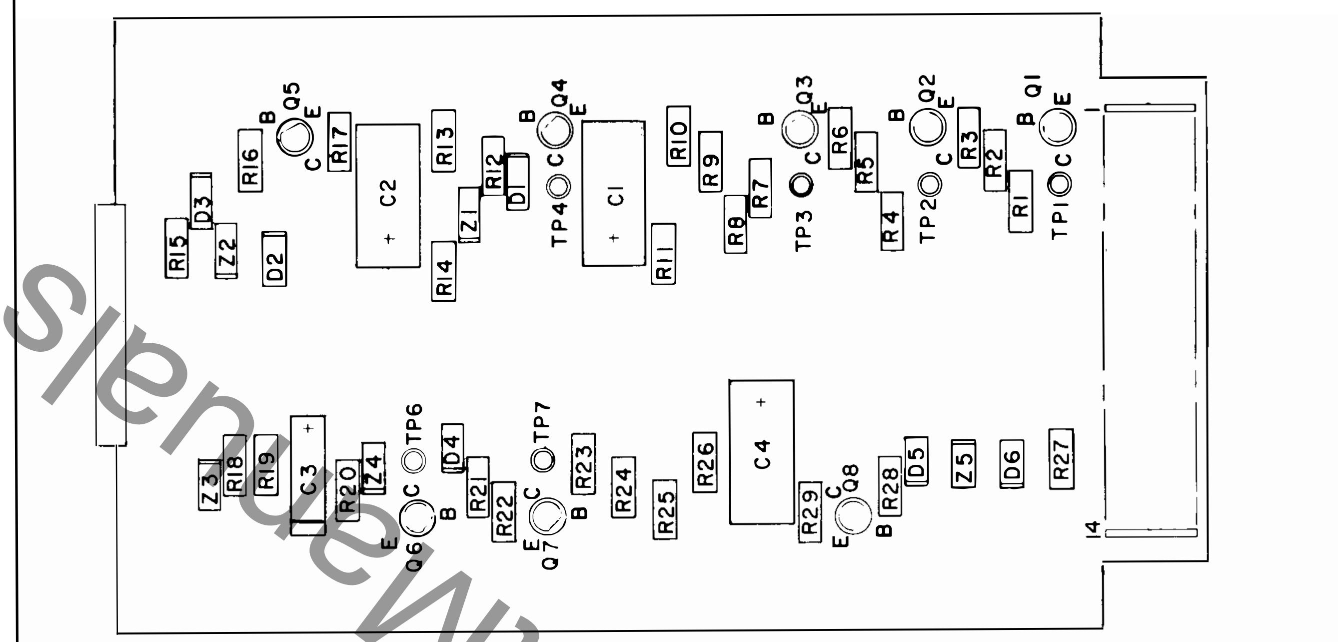
715B267

Fig. 30 Internal Schematic Transmitter Key Bd. for TCF Channel.



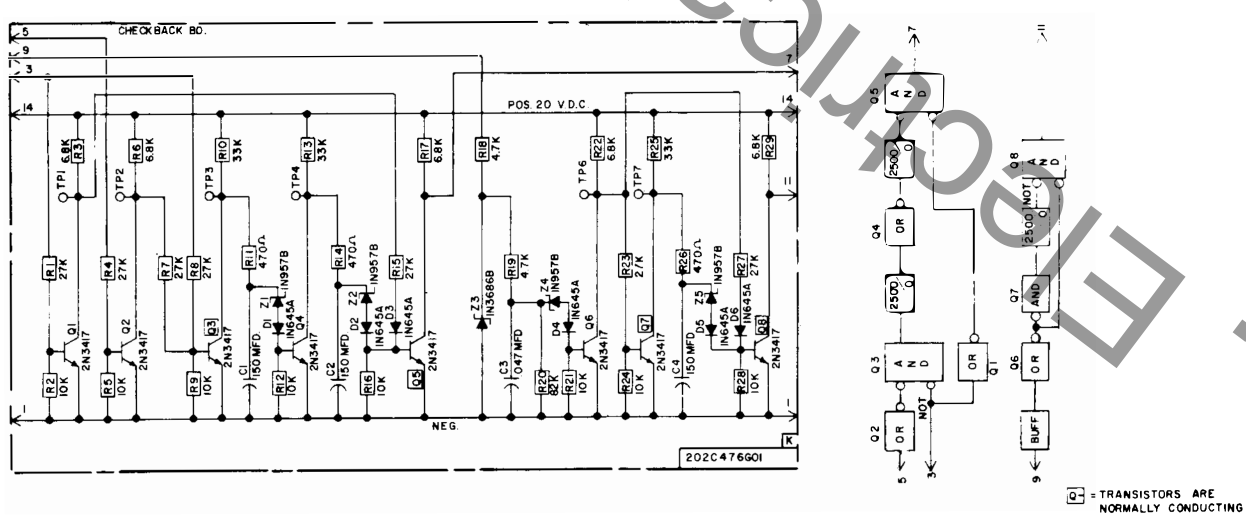
715B268

Fig. 31 Internal Schematic Transmitter Key Bd. for a Tone Channel.



715B221

Fig. 32 Component Location Checkback Bd.



715B206

Fig. 33 Internal Schematic Checkback Bd.

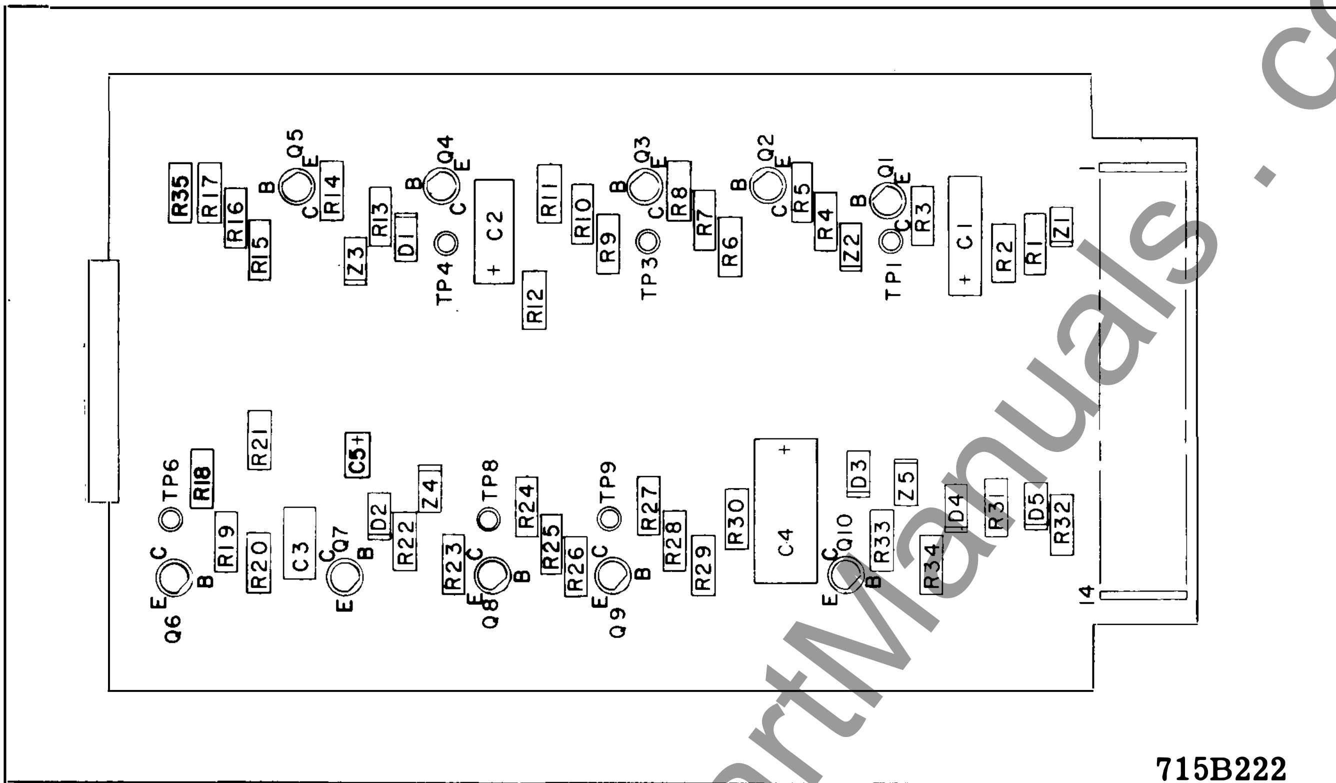


Fig. 34 Component Location Timing Bd.

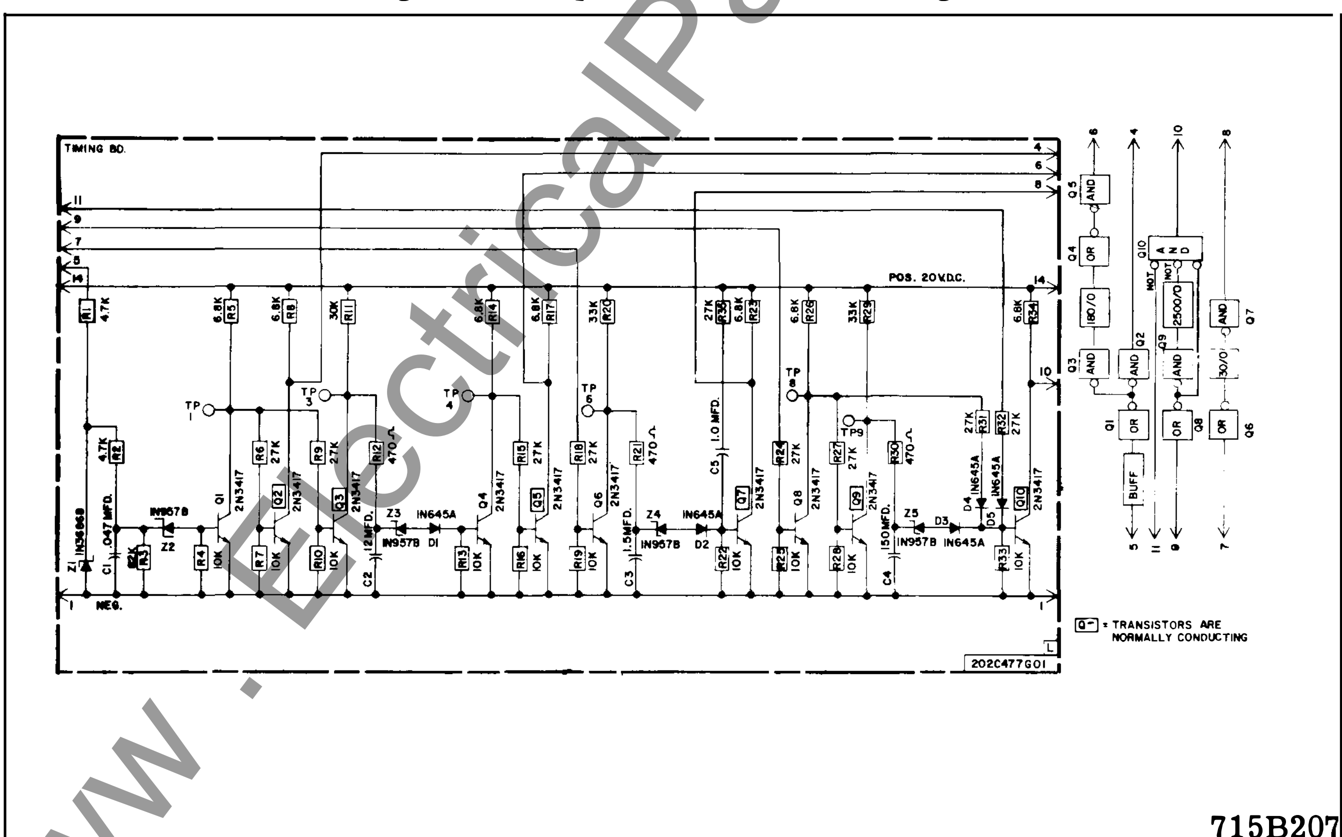


Fig. 35 Internal Schematic Timing Bd.

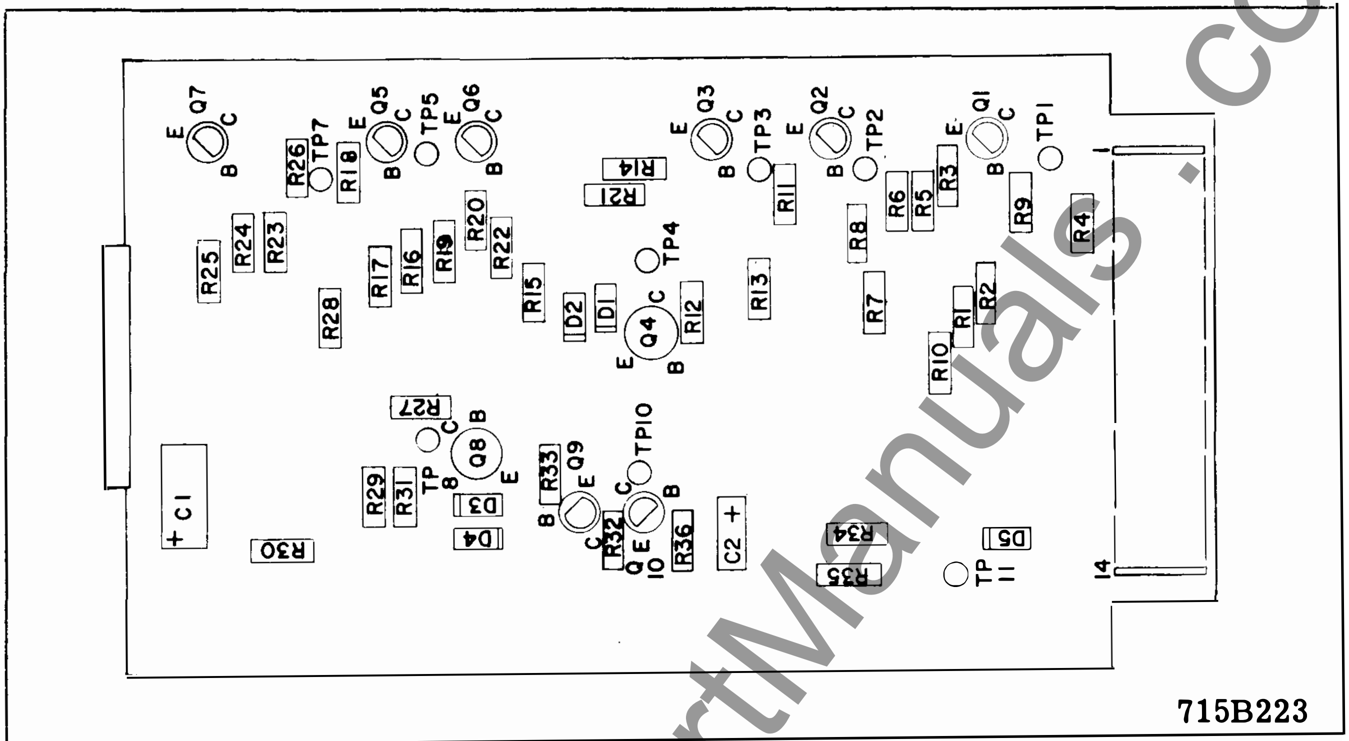


Fig. 36 Component location Arming Board.

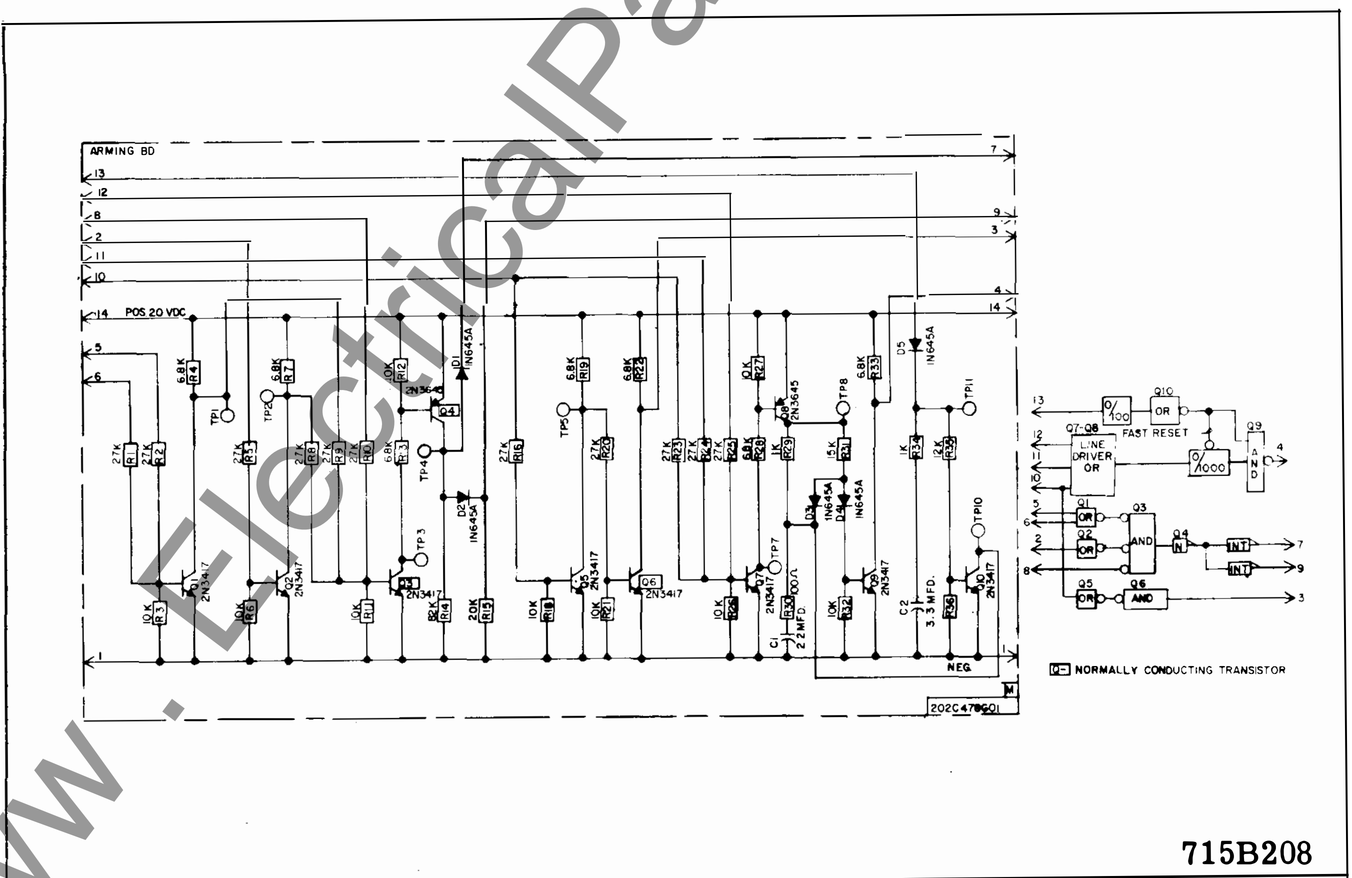


Fig. 37 Internal Schematic Arming Board.

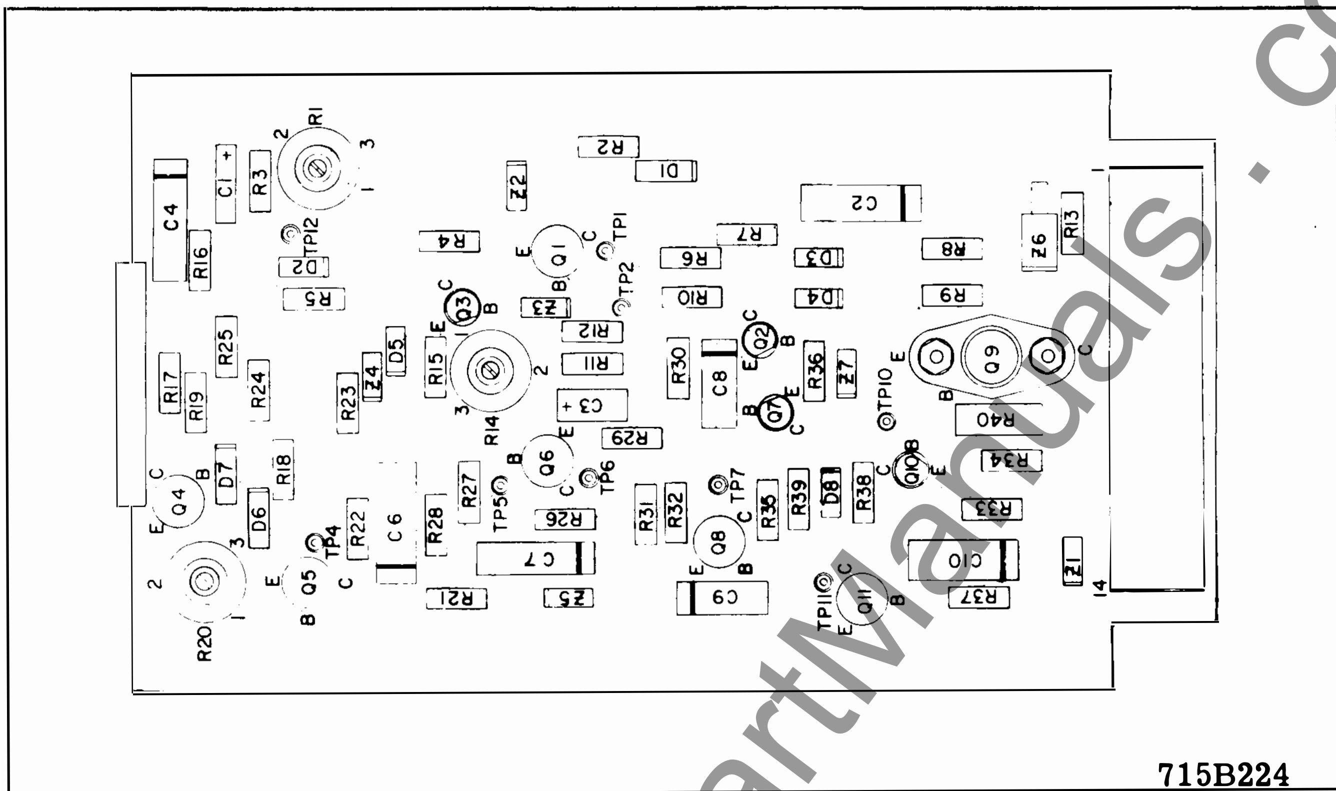


Fig. 38 Component location Output Board.

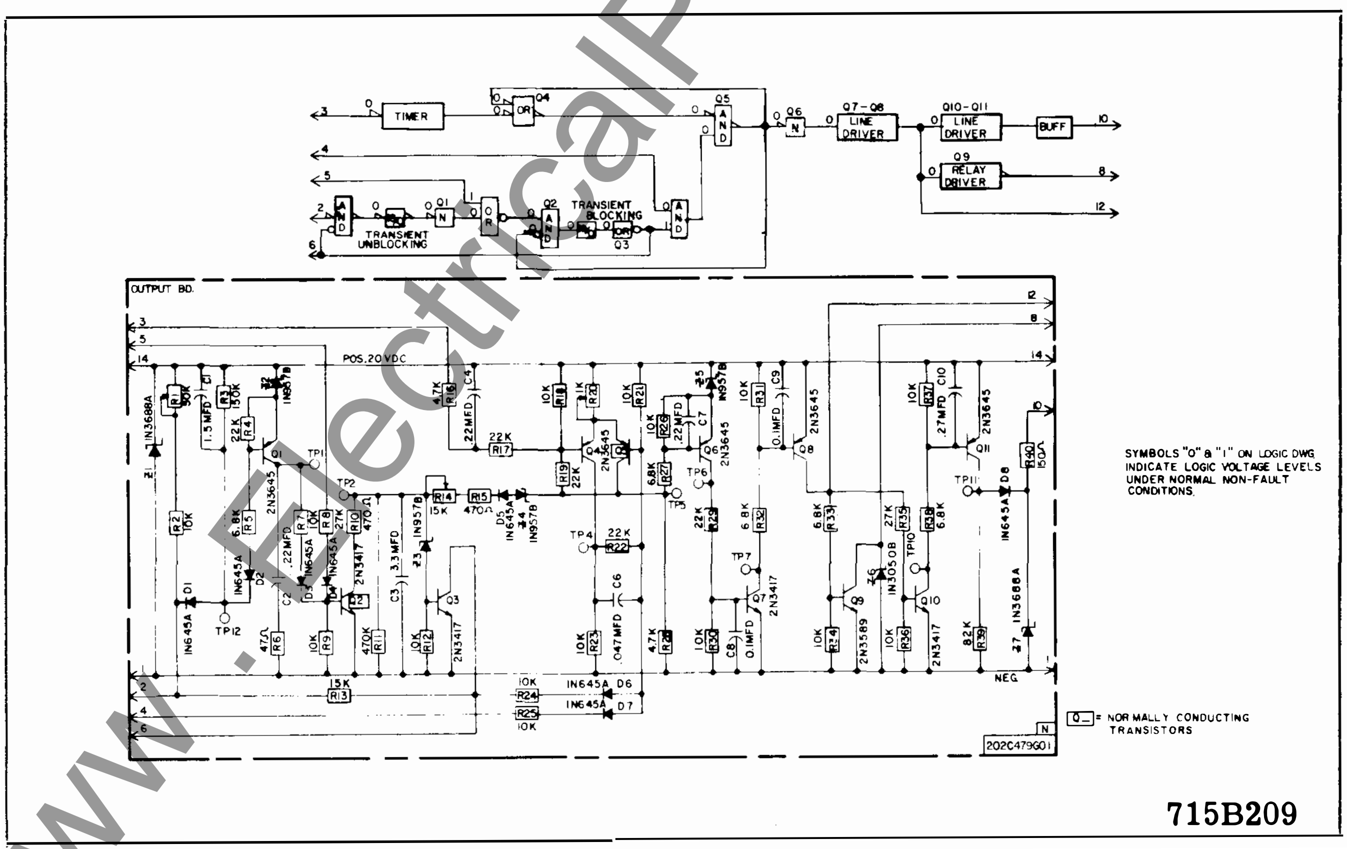


Fig. 39 Internal Schematic Output Board.

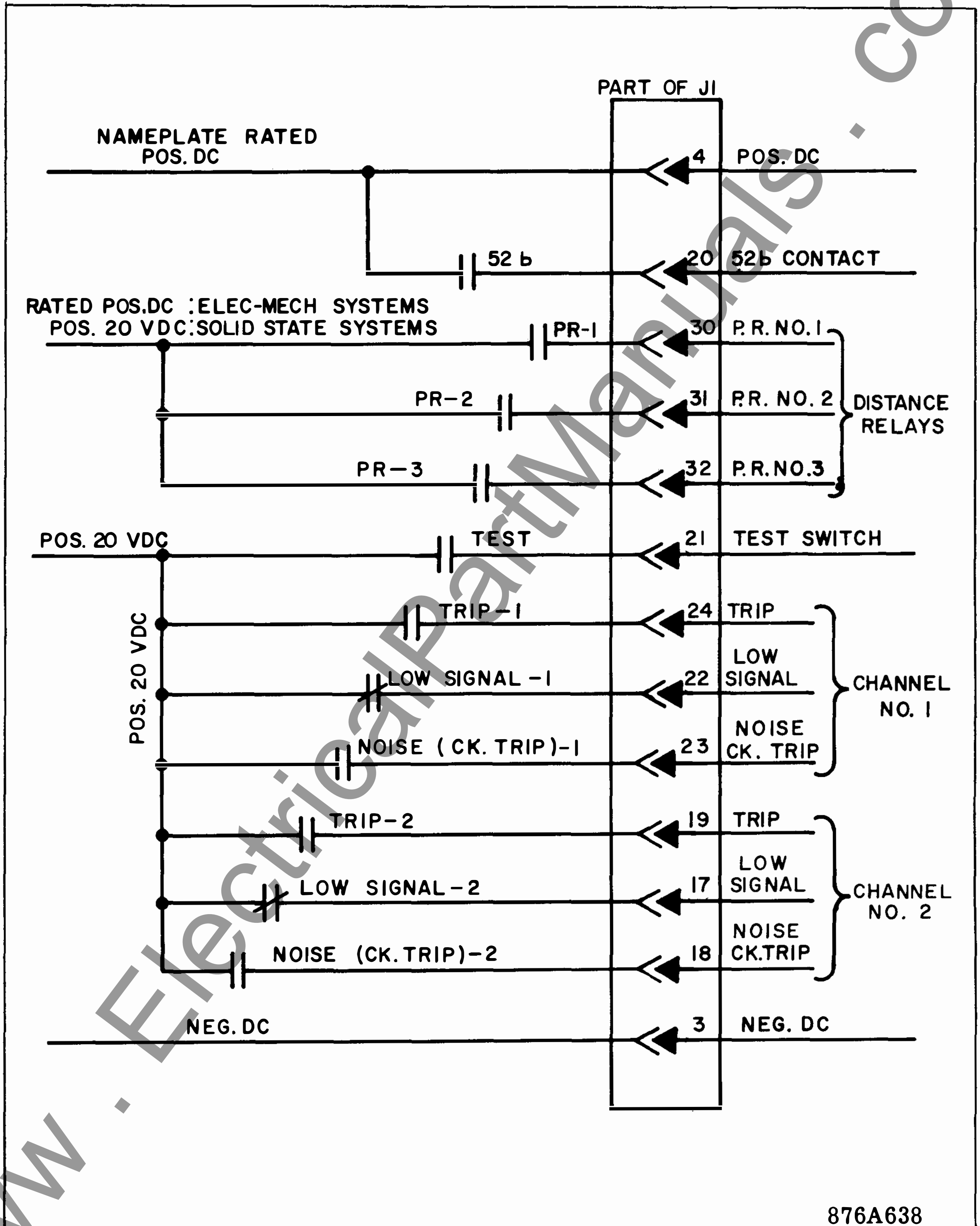


Fig. 40 Test Circuit.

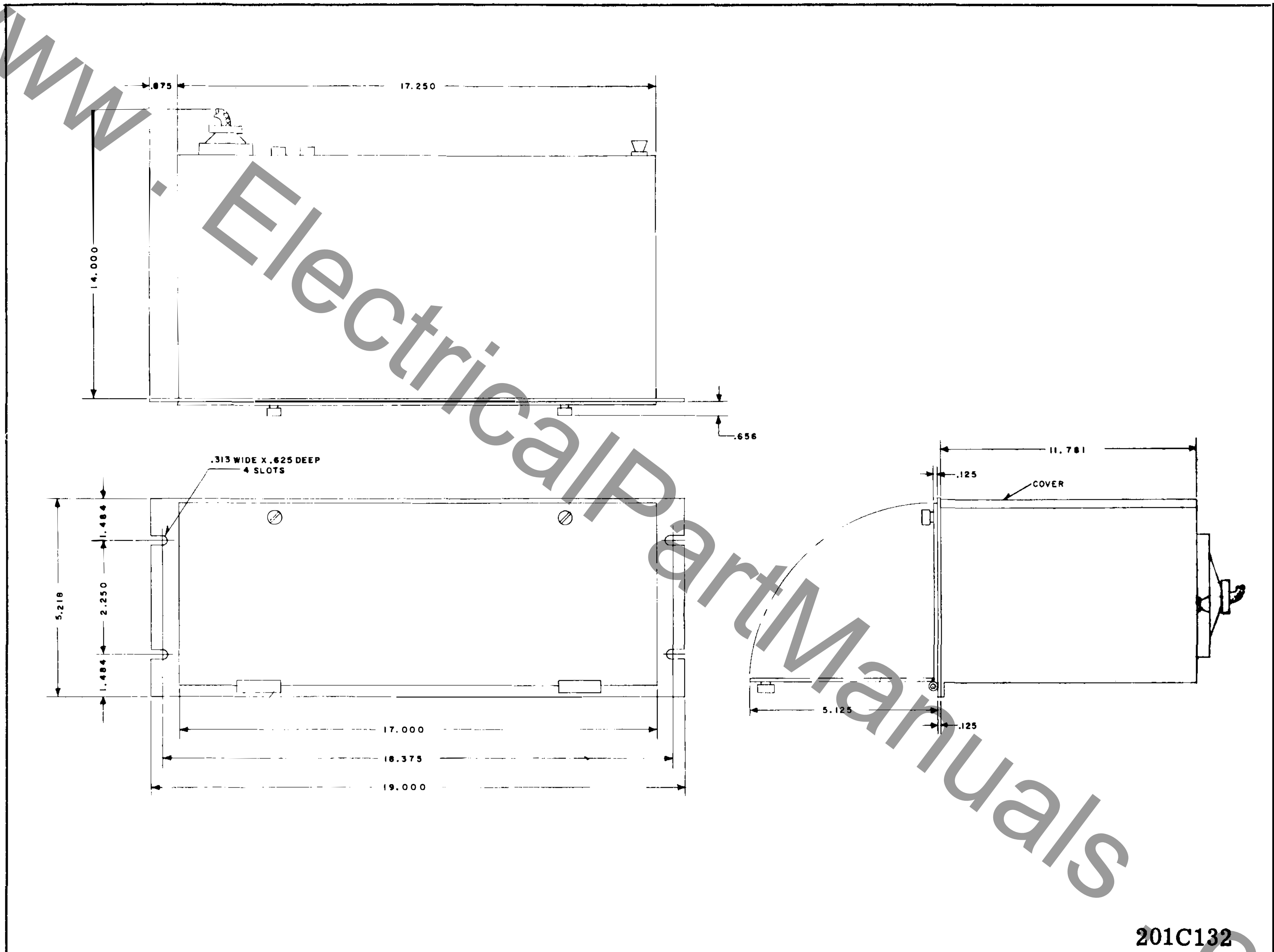


Fig. 41 Outline and Drilling Plan.

WESTINGHOUSE ELECTRIC CORPORATION

RELAY-INSTRUMENT DIVISION **NEWARK, N. J.**

Printed in U.S.A.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE STU UNBLOCK RELAY

CAUTION: It is recommended that the user of this equipment become acquainted with the information in either these instructions or the systems instruction leaflet 40-204 before energizing this relay. Failure to observe this precaution may result in damage to the equipment. Before putting the relay into service, operate the relay to check the electrical connections.

Do not remove or insert printed circuit boards while the STU relay is energized.

APPLICATION

The type STU relay is a solid state directional comparison unblocking auxiliary relay for use with solid state or electromechanical distance relays, and a frequency shift type TCF carrier or TA-3 tone channel. This relay will prevent tripping for faults external to the protected line section to which it is applied and permit high speed simultaneous tripping for internal faults. The relay will respond to indications of fault direction and distance provided by the phase and ground distance relays, thereby controlling the transmission of an unblocking signal and the initiation of high speed tripping for internal faults. Either two or three terminal line applications may be used where all line terminals provide adequate fault current to operate the overreaching distance relays.

CONSTRUCTION

The STU relay is mounted on a standard 19" wide panel 5-$\frac{1}{4}$" high (3 rack units) with edge slots for mounting on a standard relay rack or panel. For the outline and drilling plan, refer to Fig. 41.

A hinged and removable door on the front of the chassis covers the printed circuit boards. The photograph in Fig. 1 shows the front view of the relay with door open. A sealing post at the top center in front may be used to lock and seal the relay when in service.

The rear panel consists of a hinged door which may be opened to expose various components mounted inside. Mounted on the hinged door are two AR type auxiliary relays and, when used, two AL telephone type relays. The AR relay is a small high-speed attracted armature type of unit. An insulated member, fastened to the free end of the armature, draws down four moving-contact springs to close or open the contacts when the relay coil is energized. This relay is mounted on the rear hinged door, is available for inspection by removing the locking screw and swinging the hinged door outward. In the AL relays, an electromagnet attracts a right-angle iron bracket which in turn operates a set of make or break contacts. Four power supply resistors are mounted in the rear housing of the chassis. In addition, one 32 terminal connector, J1, and two, four (4) terminal, terminal blocks are mounted on the rear of the panel. The photo in Fig. 2 shows the rear view of the STU relay with the top cover off and rear door open.

All of the circuitry suitable for mounting on printed circuit boards is contained in an enclosure behind the front door. The printed circuit boards slide into position in slotted guides at the top and bottom of the enclosure, and engage a terminal block at the rear of the compartment. Each board and terminal block are keyed so that they cannot be accidently inserted into the wrong slot location. A handle mounted on the front end of the board is used for identification, and for removing and inserting the circuit. In addition the handles also serve as a bumper with the front door to prevent the board from becoming disconnected from its terminal block. The boards may be removed for replacement purposes or for use in conjunction with a board extender (Style No. 849A534G01) which permits access to the boards test points and terminals for making measurements while the relay is energized.

Either 13 or 14 printed circuit boards are used in the STU chassis. The location and title of the printed circuit boards are shown on the relay component location drawing, Fig. 3.

PRINTED CIRCUIT BOARDS

Following is a description of all the printed circuit boards used in the STU relay. Refer to the functional relay logic shown in Fig. 4, 5, 6, & 7. The internal schematics associated with the printed circuit boards contain a detailed NOR/NAND logic diagram to simplify understanding of the transistor logic.

For those users not generally acquainted with logic circuit notation or with device symbols of those components used in the STU drawings, it is recommended that a copy of Westinghouse instruction leaflet I.L. 41-000.1 entitled SYMBOLS FOR SOLID STATE PROTECTIVE RELAYING be consulted.

Power Supply Board

The Power Supply board located in slot A contains two 20 volt transistor regulators: These voltage regulators will operate from a nominal battery supply of 48 or 125 volts dc by varing resistors RA, RB, RC, & RD mounted in the rear of the chassis.

The location of components on this board is shown in Fig. 8, and the internal schematic is Fig. 9.

Protective Relay (P.R.) Interface Boards

The Protective Relay (P.R.) Interface board located in slot B contains the buffered interface logic for the distance relays and the functional test switch. Other logic associated with the protective relays is included.

Location of components on this board is shown in Fig. 10. Two internal schematics are used: Fig. 11 - For use with electromechanical distance relays and Fig. 12 - For use with solid state distance relays. The difference in the two schematics is the buffered distance relay input; 48/125 VDC input for electromechanical systems, 20 VDC input for solid state systems.

Loss of Potential Boards

The Loss of Potential board located in slot C contains a 500/0 millisecond time delay and logic to cause an alarm and voltage output if a distance relay inadvertantly operates on a blown ac potential fuse or has an sustained output for greater than 500 milliseconds. An input AND prevents operation of the timer if both channel trip signals are obtained.

In relays for use with electromechanical systems, a relay driver is provided on this board to energize the Loss of Potential AL telephone relay mounted in the rear of the chassis.

Location of components on this board is shown in Fig. 13. Two internal schematics are used: Fig. 14 - For use with electromechanical systems and Fig. 15 - For use with solid state systems.

ELEC-MECH (E.M.) Interface Board

The ELEC-MECH (E.M.) Interface board located in slot D is used only in systems using electromechanical distance relays. Upon receipt of a distance relay signal, this circuit of two timers (0/25 and 20/0 millisecond) and associated logic will immediately simulate a protective relay signal for 20 milliseconds, thereby overriding any contact bounce in the electromechanical relays.

Location of components on this board is shown in Fig. 16, and the internal schematic in Fig. 17.

Channel Interface Boards

The Channel Interface boards located in slot F (Channel 1) and slot G (Channel 2 - when used) contain the buffered interface logic for connection with the channel equipment and provide the outputs to work into the Channel Trip and Supv. boards. In addition, the TA-3 Channel Interface board contains buffered outputs.

An interlock feature is also included in order to convert from a 2 to 3 terminal line relay and conversely. CHANNEL TWO INTERFACE in slot G must be used in the relay for THREE TERMINAL LINE applications, but MUST BE REMOVED for TWO TERMINAL LINE systems.

A conversion kit may be ordered to change a 2 TERM LINE relay to 3 TERM LINE. This kit includes instructions, nameplate and a CHANNEL INTERFACE board. The location of components for both the TA-3 and TCF - CHANNEL INTERFACE boards is shown in Fig. 18. Internal schematics are shown in Fig. 19 for the TA-3 CHANNEL and Fig. 20 for the TCF CHANNEL.

Channel Trip Boards

The Channel Trip board located in slot H contains the connecting logic between the channel unblock trip signals and the remainder of the relay logic. A buffered output for channel 1 and 2 trip is included on this board.

The Tone Channel Trip board also has additional logic comprised of two AND'S and an OR for a block return function. This logic is inherent to the TCF channel equipment, therefore it is not required in this relay.

Location of components on this board is shown in Fig. 21. Two internal schematics are used: TONE CHANNEL TRIP BOARD - Fig. 22, TCF CHANNEL TRIP BOARD - Fig. 23.

Channel Supervision Boards - TCF Channel

The Channel Supv. Board for a TCF channel is located in slot I and contains the connecting logic between the supervisory functions of the channel equipment and the remainder of the relay logic. Both LOW SIGNAL CLAMP OUTPUTS work into an OR, as do both CHECK TRIP outputs.

In addition, there is a circuit comprised of an AND circuit and a 0/150 millisecond time delay to allow tripping when reclosing into a fault.

For electromechanical systems, a relay driver is used for energizing a loss of channel AL telephone relay.

Location of components for this board is shown in Fig. 26. Two internal schematics are used: Fig. 27 for electromechanical systems and Fig. 28 for solid state systems.

Channel Supervision Board - Tone Channel

The Channel Supv. board for a tone channel is located in slot I and contains the connecting logic between the supervisory functions of the channel equipment and the remainder of the relay logic. A 150/100 millisecond time delay and associated logic is used to monitor the LOW SIGNAL CLAMP outputs for loss of channel and to provide unblock time. For electromechanical systems, a relay driver is used for energizing a Loss of Channel AL telephone relay. The NOISE outputs work into OR logic on this board.

In addition, there is a circuit comprised of an AND circuit and a 0/150 millisecond time delay to allow tripping when reclosing into a fault.

Location of components for this board is shown in Fig. 24 and the internal schematic in Fig. 25.

Transmitter Key Boards

The transmitter Key board located in slot J contains OR logic to combine all inputs required to key the transmitter, and interface circuitry to key the particular channel equipment. A relay driver circuit is connected to the output of the OR in order to operate an AR relay mounted in the rear of the chassis.

For the channel interface with the TCF transmitter, a positive going (0 to 20 volt) buffered output represented by transistors Q4 and Q5 is shown on the internal schematic, Fig. 30. When the relay is used with tone channels, the transmitter interface is a negative going output similar to the relay driver and is shown by transistor Q6 on internal schematic, Fig. 31.

Location of components for the XMTR KEY board is shown in Fig. 29.

Checkback Board

The Checkback board located in slot K contains logic used to functionally test the channel in both directions. Two separate circuits are included on the board. One circuit comprised of a buffered input, AND circuit and a 2500/0 millisecond time delay is used for keying the transmitter for 2.5 seconds after the TEST switch is operated. The other circuit consisting of two AND circuits and a 2500/2500 millisecond time delay is operated from the CHANNEL SUPV. BD. and is required as part of the channel checkback scheme.

The location of components for this board is shown in Fig. 32 and the internal schematic in Fig. 33.

Timing Board

The Timing board located in slot L contains logic, a buffered input, and three time delays used in conjunction with the remainder of the relay.

After a pilot trip operation, the 0/30 millisecond timer maintains the transmitter keying for 30 milliseconds. The 180/0 millisecond timer delays keying of the transmitter for 180 milliseconds after opening of the local breaker. Input to this timer is a 48/125 VDC buffer circuit.

The 2500/0 millisecond timer and associated logic is used to permit transient blocking for 2.5 seconds if a unblock trip output is obtained from the channel receiver. This circuit is also controlled by the 52b contact input.

The location of components on this board is shown in Fig. 34, and the internal schematic in Fig. 35.

Arming Board

The Arming board located in slot M contains the connecting logic between the Channel, Protective Relay, Elec-Mech and Timing boards for the OUTPUT board. Logic on this board interfaces with, and sets up arming of the trip AND, the transient blocking and unblocking timers and the 4/0 millisecond trip timer.

In addition, two time delays, 0/1000 and 0/100 milliseconds, are included on this board. The 0/1000 MS timer holds transient blocking on for an additional 1000 MS to protect against fault power reversals due to unequal breaker reclosing times into a permanent external fault. After a pilot trip operation, the 0/100 MS timer picks up and immediately resets the 0/1000 MS timer to de-energize the transient blocking timer. The 100 MS dropout time is greater than the time it takes to reset the distance relays and remove the input to the 0/1000 MS timer, therefore transient blocking will remain off after the pilot trip signal is removed.

The location of components for this board is shown in Fig. 36, and the internal schematic in Fig. 37.

Output Board

The Output board located in slot N contains the final logic of the relay. This board utilizes the intelligence supplied by the Arming board to set up either a pilot trip output for internal faults, transient blocking on external faults or transient unblocking for sequential faults.

Three timers are used on this board: a 4/0 millisecond timer to delay the pilot trip output and two 18/0 millisecond timers for transient blocking and unblocking. NOTE: Relays may be supplied with the transient block time calibrated for 25 milliseconds instead of 18 ms. to coordinate with the time delay of the channel equipment. The pilot trip output is comprised of and AND circuit whose output works into a logic inverting amplifier. There are two final pilot trip outputs; a buffered positive going (0 to 20 volt) output and a relay driver to activate an AR relay mounted in the rear of the chassis.

Fig. 38 shows location of components on this board, and Fig. 39 shows the internal schematic and detailed logic.

Test Board

The Test board located in slot O is used for facilitating test measurements and routine checks of the relay. This board consists of 10 test terminals mounted on a panel attached to a printed circuit board.

OPERATION

The type STU unblock relay is used in a directional comparison unblocking relay system for power line protection. High speed tripping is obtained for two or three terminal line applications for faults anywhere on the protected line, providing all terminals contribute adequate fault current to operate the distance fault detectors.

System Operation

In a directional comparison unblocking system, a continuous blocking signal is normally transmitted from each line terminal and received at all other terminals. The phase or ground protective relays key the channel transmitters to the unblock frequency to remove blocking at the remote terminals during a fault. Tripping is accomplished when both the local protective relay operates, and the blocking signal has been removed. The unblocking signal does not have to be received to allow tripping.

Some features included in this system are a functional test channel checkback scheme, lockout of tripping after 500 milliseconds for abnormal protective relay operation, channel logic to force a block return, and coordination for bus fault tripping, breaker failure and fault power flow reversal. The description of the preceding features are further explained under the Relay

Operation section.

Refer to system I.L. 40-204 on the unblocking system for further system operation.

Relay Operation

Refer to the logic diagrams shown in Fig. 4, 5, 6, and 7 to understand the operation of the STU unblock relay.

1. Normal Condition

In Fig. 4, 5, 6, and 7 the logic voltage "0" and "1" states shown refer to the normal operating condition of the STU relay.

2. Internal Fault

For an internal fault, one or more of the protective distance relays will operate and perform the following:

a. Start the 500/0 MS loss of potential timer
b. Produce a logic "1" at TEST TERM 3 (Protective Relay)
c. Key the transmitter to the unblock frequency
d. Pickup the 0/1000 MS timer on the ARMING BD. and produce a logic "0" at terminal 5 of the OUTPUT BD. This will start the transient blocking timer.
e. Arm the trip AND on the OUTPUT BD. through the one input OR on the ARMING BD.
f. Satisfy one input of the trip AND on the ARMING BD.

The channel transmitter will also be keyed at the remote terminal, thus causing the unblock trip outputs of the local channel 1 and 2 receivers to become a logic "1". This will make TEST TERM 4 (CHANNEL TRIP) a logic "1" signal through logic on the CHANNEL INTERFACE and CHANNEL TRIP BDS. This "1" output will satisfy the trip AND on the ARMING BD. causing energization of the 4/0 MS timer on the OUTPUT BD. Four milliseconds later the trip AND on the OUTPUT BD. will be satisfied and produce a PILOT TRIP output before transient blocking becomes effective.

In addition, when a receiver unblock trip output (logic "1") is received as an input to the STU the 2500/0 MS timer on the TIMING BD. will be energized to start transient blocking. This will not affect the initial pilot trip, and once the local breaker opens, then the 52b contact will block the output of this AND on the TIMING BD.

Once a pilot trip signal is obtained for an internal fault, the 0/100 MS timer on the ARMING BD. will rapidily reset the 1000 millisecond dropout time of the 0/1000 MS timer. Therefore, when reclosing into a permanent internal fault, the only time delay will be the 4/0 MS timer.

3. External Fault

If no unblock trip signal is received from the remote terminal when the local distance relays operate, then the trip AND on the ARMING BD. will not be satisfied and the 18/0 MS transient blocking timer will time out. TEST TERM 2 (Transient Blocking) will then become a negative logic "1" and block the trip AND of the OUTPUT BD. thereby preventing possible undesirable tripping during transients occuring at the clearing of an external fault.

If an external fault occurs behind the protected line such that the local distance relays do not operate, but either one or both of the channel receivers are keyed to the unblock frequency at the remote terminal then transient blocking will also be set up. When either channel unblock trip output assumes a logic "1" state, the 2500/0 MS timer on the TIMING BD. is energized and a logic "1" is obtained at TIMING BD. terminal 10 for 2.5 seconds. This output will activate the 0/1000 MS timer on the ARMING BD. and set up transient blocking 18 milliseconds later.

In addition, for external faults, transient blocking is established to insure against any misoperation due to fault power flow reversals caused by unequal circuit breaker clearing time on parallel lines. The 1000 millisecond reset time of the 0/1000 MS timer on the ARMING BD. prevents misoperations when reclosing into an external fault where fault power flow reversals occur on parallel lines due to unequal breaker reclosing times. In addition, the 1000 millisecond reset time also prevents transient blocking from resetting when short holes appear in the input.

4. Sequential Fault

Occasionally an external fault will be followed by an internal fault before the former is cleared. In order to prevent a long delay in clearing a sequential fault, a transient unblocking 18/0 MS timer is included. Although transient blocking has been initiated by the external fault, the presence of an internal fault will produce a negative logic "1" signal from the trip AND on the ARMING BD. This "1" signal will energize the 4/0 MS timer and satisfy the AND to energize the 18/0 MS transient unblocking timer on the OUTPUT BD. In 18 milliseconds the transient unblocking timer will drop out the transient blocking timer thus satisfying the trip AND on the OUTPUT BD. and causing a pilot trip output.

5. Loss of Potential

Distance relays may tend to operate if the input from the potential device is momentarily interrupted. Since tripping of circuit breakers is undesirable for this loss of ac potential, or any other abnormal protective relay operation, the STU relay will lockout tripping and provide alarm. This is accomplished by the 500/0 MS timer on the LOSS OF POTENTIAL BD. In 500 milliseconds after a distance relay operation, providing both receiver unblock trip signals are not present, a logic "1" signal will be produced at TEST TERM 7 (Loss of Potential). This "1" signal will block the AND on the PROTECTIVE RELAY INTERFACE BD. thereby simulating no distance relay signal. Output of the 500/0 MS timer will also provide a buffered "1" signal at the J1 connector.

For electromechanical systems, an AL telephone relay will drop out for indication purposes.

6. Channel Transmitter Control

The transmitter may be keyed to the unblock frequency by any one of the following six inputs:

a. Distance relay operation
b. 0/30 MS timer after pilot trip
c. 180/0 MS timer from 52b contact
d. Checkback circuit from test switch
e. Checkback circuit from channel logic
f. Output from E.M. Interface Bd. for electromechanical systems only.

When the transmitter is keyed, TEST TERM 5 (XMTR KEY) becomes a logic "1" signal, the keying AR picks up, and the interface with the transmitter becomes a logic "1" as described under the operation of the XMTR KEYING BD.

After a pilot trip operation the 0/30 MS timer on the TIMING BD. will maintain keying of the unblock frequency for 30 milliseconds in order to insure that the remote breaker has tripped before the transmitter returns to normal condition.

After the local circuit breaker opens, the 52b contact will close and energize the 180/0 MS timer on the TIMING BD. to cause initiation of the unblock frequency transmission after 180 milliseconds and until such time as the circuit breaker is reclosed. This 180 millisecond delay allows coordination for bus fault tripping of the local breaker, where tripping of the remote breaker would be incorrect and might cause undesired interruption to tapped transformer terminals. Transmission of the unblocking frequency is necessary to permit tripping of the remote terminal should the remote circuit breaker be closed into a fault, or should a fault develop in the protected line while the local circuit breaker is open.

7. Channel Logic

a. TCF frequency shift carrier channel.
   Refer to CHANNEL-INTERFACE, TRIP, and SUPERVISION BDS. in logic logic drawings Fig. 4 and 5.

Two TCF CHANNEL INTERFACE boards are shown; both boards must be used for three terminal line systems utilizing two receivers. However, for two terminal line application, the interface board in board slot G must not be used in the relay. An interlock shown on the Channel 2 interface board connects the Channel 2 unblock trip output as one input to the channel trip AND on the CHANNEL TRIP BD.

For three terminal line application, both receiver unblock trip signals are required to produce a logic "1" signal at TEST TERM 4. This output will satisfy one input of the ARMING BD. trip AND, block operation of the 500/0 MS Loss of Potential timer, and produce a buffered "1" output. Either receiver unblock trip signal will produce a "1" signal at terminal 12 of the CHANNEL TRIP BD. to start transient blocking. For two terminal line applications, the one receiver unblock trip signal will produce a "1" output at TEST TERM 4 (CHANNEL TRIP), and terminal 12 of the CHANNEL TRIP BD.

Operation of either or both low signal clamp inputs ("1" to "0") will cause a "1" signal at TEST TERM 6 (Loss of Channel) for use in the channel checkback scheme. For electromechanical systems, an AL telephone relay will dropout for indication of loss of channel. In addition, operation of either Check Trip output will produce a "1" output at terminal 7 of the CHANNEL SUPV. BD. This signal is used for the channel checkback scheme.

If the carrier channel is lost for an internal fault condition then the TCF receiver will convert to an unblock trip signal for 150 milliseconds to allow tripping before lockout. However, it is still desirable to have this system operative if reclosing into a permanent fault. This is accomplished by the 0/150 MS timer and AND circuit on the CHANNEL SUPV. BD. After the initial opening of the breaker, the 52b contact will close and pickup the 0/150 MS timer. Upon reclosure the 52b contact opens and starts dropout of the 0/150 timer, therefore with a loss of channel signal from the TCF, a "1" output will be obtained from the AND. This "1" produces a "1" at TEST TERM 4 to permit tripping if a distance relay operates.

b. Frequency shift tone channel.
Refer to CHANNEL INTERFACE, TRIP and SUPERVISION BDS. in logic drawings Fig. 6 and 7.

Two tone CHANNEL INTERFACE bds. are shown; both boards must be used for three terminal line systems utilizing two receivers. However, for two terminal line applications, the interface board in board slot G must not be used in the relay. An interlock shown on the Channel 2 interface board connects the Channel 2 unblock trip output as one input to the three input channel trip AND on the CHANNEL TRIP BD.

For three terminal line applications, both receiver unblock trip signals and no low signal clamp are required to produce a logic "1" signal at TEST TERM 4 (CHANNEL TRIP). This output will satisfy one input of the ARMING BD. trip AND, block operation of the 500/0 MS Loss of Potential timer, and produce a buffered output. Either receiver unblock trip signal will produce a "1" signal at terminal 12 of the CHANNEL TRIP BD. to start transient blocking and to energize an AND circuit on the CHANNEL SUPV. BD.

For two terminal line applications, the one receiver unblock trip signal will produce a "1" output at TEST TERM 4, and terminal 12 of the CHANNEL TRIP BD.

When a tone channel is used with the STU unblock relay, the tone receivers must be internally strapped to clamp to an unblock trip output when a low signal condition occurs. Therefore, if during an internal fault condition the channel is lost, tripping will be allowed until the 150/100 MS timer on the CHANNEL SUPV. BD. picks up and blocks the channel trip AND on the CHANNEL TRIP BD. However, it is still desirable to have this system operative if reclosing into a permanent fault. This is accomplished by the 0/150 MS timer and AND circuit on the CHANNEL SUPV. BD. After the initial opening of the breaker, the 52b contact will close and pickup the 0/150 MS timer. Upon reclosure the 52b contact opens and starts dropout of the 0/150 timer, therefore with a loss of channel signal from the tones, a "1" output will be obtained from the AND. This "1" produces a "1" at TEST TERM 4 to permit tripping if a distance relay operates.

Either low signal clamp operation ("1" to "0") will pickup the 150/100 MS timer and produce a "1" signal at TEST TERM 6 (LOSS OF CHANNEL) for use in channel checkback as well as blocking channel trip. For electromechanical systems, an AL telephone relay will dropout for indication of loss of channel. Both low signal clamp outputs on the CHANNEL INTERFACE BDS. are buffered and separately brought out to the J1 connector.

One AND circuit on the CHANNEL SUPV. BD. is used for channel checkback. When a receiver trip signal from either channel is received, a logic "1" will be produced at terminal 3 of the CHANNEL SUPV. BD. providing both low signal clamps have not operated.

When the noise output operates on either one or both channel receivers, a logic "1" output is produced from the noise OR on the CHANNEL SUPV. BD. to block the trip AND of the ARMING BD. Therefore, the STU relay will not trip on receipt of channel noise. Both noise outputs on the CHANNEL INTERFACE BD. are buffered, connected together, and brought out to the J1 connector.

A block return circuit is included on the CHANNEL TRIP BD., and is comprised of two AND'S and an OR. The principle of block return is to insure that after a loss of channel condition is cleared up, the receiver unblock trip signal returns in the "0" logic state, not "1". When a low signal clamp operation ("1" to "0") is received from the tone channel, then the 150/100 MS timer picks up and applies a "1" signal to one input of each of the two block return AND'S on the CHANNEL TRIP BD. Now, if either or both receiver unblock trip signals are a "1" or become a "1" within the 100 millisecond dropout time of the 150/100 MS timer, then a "1" output will be produced at the output of the block return AND and the OR in works into. Terminal 5 of the CHANNEL TRIP BD. will become a "1" and hold the 150/100 MS timer picked up by applying a "1" input to the 3 input loss of channel OR on the CHANNEL SUPV. BD. By inspecting the logic, it can be seen that both receiver unblock trip signals (one for two terminal line applications) must return to block, logic "0", to make the channel operative after a loss of channel condition.

8. Channel Checkback Test

   a. TCF frequency shift carrier channel.
      Refer to logic drawings, Fig. 4 and 5. Information in this section does not cover the complete test, but only that portion concerning the STU relay.

At the local terminal, the carrier transmitter will be disconnected from the line thus causing a loss of channel condition at the remote terminal. This will cause the loss of channel OR on the CHANNEL SUPV. BD. (Remote Terminal) to assume a "1", and satisfy the two input AND (preceding the 2500/2500 MS timer), and in 2500 milliseconds pickup the 2500/2500 MS timer on the CHECKBACK BD. The "1" output of the 2500/2500 MS timer will satisfy one input of the AND following it. Next, the test switch will be operated at the local terminal and the following will happen: a protective relay signal will be simulated through the OR on the protective relay interface bd., the transmitter will be reconnected to the line to restore the channel, and the local transmitter will be keyed to the unblock frequency for 2500 milliseconds through the 2500/0 MS timer and AND circuit on the CHECKBACK BD. At the remote terminal, the TCF receiver logic will not give a trip output since the channel was not restored to the blocking frequency. However, there will be a "1" signal obtained from the CHECK TRIP output of the receiver. This check trip output will satisfy the other input to the AND on the CHECKBACK BD. causing the transmitter to be keyed to the unblock frequency. Since the check trip signal also applies a "1" input to the negated input of the AND energizing the 2500/2500 MS timer, it will no longer be satisfied and the timer will drop out causing keying to stop in 2.5 seconds. However within the 2.5 seconds of keying, the STU relay at the local terminal will trip because of reception of both a received unblock trip signal and a simulated protective relay signal.

b. Frequency shift tone channel.
Refer to logic drawings, Fig. 6 and 7.
Information in this section does not cover the complete test, but only that portion concerning the STU relay.

At the local terminal, the tone transmitter will be disconnected from the line thus causing a loss of channel condition at the remote terminal. This will cause the loss of channel OR on the CHANNEL SUPV. BD. (Remote Terminal) to assume a "1" output to pick up the 150/100 MS timer. This satisfies the two input AND on the CHECKBACK BD. and in 2500 milliseconds the 2500/2500 MS timer will pick up. The "1" output of the 2500/2500 MS timer will satisfy one input of the AND following it. Next, the test switch will be operated at the local terminal and the following will happen: a protective relay signal will be simulated through the OR on the protective relay INT BD, the transmitter will be reconnected to the line to restore the channel, and the local transmitter will be keyed to the unblock frequency for 2500 milliseconds through the 2500 MS timer and AND circuit on the CHECKBACK BD. At the remote terminal, the tone receiver unblock trip signal will be a "1" thus causing the three input AND on the CHANNEL SUPV. BD. to operate and produce a "1" at terminal 3 of this board. This "1" will satisfy the other input to the AND on the CHECKBACK BD. causing the transmitter to be keyed to the unblock frequency. Since at the same time, the input to the 2500/2500 MS timer is lost, then the keying signal to the local terminal will only last 2.5 seconds. However, within this time of keying, the STU relay will trip because of the reception of both a received trip (unblock) signal and a simulated protective relay signal.

9. Electromechanical Interface

When the STU relay is used in an electromechanical system the ELEC-MECH (E.M.) INTERFACE BD. is used only for the purpose of preventing additional tripping delay because of contact bounce. When a distance relay operates, the 0/25 MS time delay on the E.M. INTERFACE BD. will immediately pickup to satisfy the AND thereby simulating a protective relay operation. The 25 millisecond drop-out time of the 0/25 MS timer will hold the "1" input to the AND in the event that bouncing contacts interrupt the timer input signal. The 20/0 timer will time out and remove the simulated protective relay signal after 20 milliseconds.

CHARACTERISTICS

CONTROL VOLTAGE:	48 V DC (42 to 56 volts) 125 V DC (105 to 140 volts)
CURRENT DRAIN:	SOLID STATE SYSTEMS Normal - 130 MA Pilot Trip - 240 MA Maximum - 280 MA ELEC-MECH SYSTEMS Normal - 170 MA Pilot Trip - 280 MA Maximum - 320 MA
TEMPERATURE RANGE:	$-20^{o}C$ to $+55^{o}C$ around chassis
INPUTS:	
52b Contact -	48/125 Control Voltage Buffered 48 V - 1.5 MA MAX Current 125 V - 2.5 MA MAX Current
DISTANCE RELAYS 1, 2, and 3:	
Solid State Systems -	15 to 20 V DC Buffered 2 MA MAX Current
Elec-Mech Systems -	48/125 Control Voltage Buffered 48 V - 1.5 MA MAX Current 125 V - 2.5 MA MAX Current
All Other Inputs Are Buffered and Require 2 MA MAX Current	15 to 20 V DC
OUTPUTS:	
TRAMITTER KEY:	
TCF Frequency Shift Carrier Channel	15 to 20 V DC Buffered 10 MA MAX Current
Frequency Shift Tone Channel	"0" State - Open Circuit "1" State - Short Circuit to Battery Neg. 140 V DC MAX Voltage 40 MA MAX Current

All other outputs are 15 to 20 V DC buffered and provide 10 MA MAX Current

CHARACTERISTICS

TIME:

TRIP TIME (4/0)	4.0 to 4.5 Milliseconds (adjustable from 2.0 to 6.0 MS)
TRANSIENT BLOCK and TRANSIENT UNBLOCK TIME (18/0)	18 to 20 Milliseconds (adjustable from 12 to 30 MS) (Relay may be ordered with a transient blocking time of 24 to 27 milliseconds)
LOW SIGNAL LOCKOUT TIME 150/100 & 0/150	130 to 180 Milliseconds
LOSS OF POTENTIAL TIME (500/0)	400 to 600 Milliseconds
DIMENSIONS:	Relay Height - 5.25" (3 rack units) Relay Width - 19" Relay Depth - 14"
WEIGHT:	Approximately 12 lbs.

SETTINGS

No setting is required on the STU relay.

INSTALLATION

The STU relay is generally supplied in a cabinet or on a relay rack as part of a complete system. The location must be free from dust, excessive humidity, vibration, corrosive fumes or heat. The maximum temperature around the chassis must not exceed 55°C.

The outline and drilling plan of the STU relay is shown in Fig. 41.

ADJUSTMENTS AND MAINTENANCE

Acceptance Check

It is recommended that an acceptance check be applied to the STU relay to verify that the circuits are functioning properly. The following procedure can be used for this purpose.

Connect the STU relay to the test circuit of Fig. 40. Apply rated dc to J1 terminals 3 and 4 as shown, and use an auxiliary 20 volt regulator or the internal 20 volts of the STU relay for the inputs to the switches. On STU relays for use with electromechanical distance relays, rated positive dc must be applied to the PR 1, 2, and 3 switches. Note that the low signal switches for channels 1 and 2 are normally closed and all other switches are open.

Since the STU relay varies in logic depending on the channel equipment, insure that it is checked per the proper channel. When reference is made to AL relays, this refers to STU relays for use only with electromechanical systems utilizing ELEC-MECH distance relays.

When reference is made to TEST TERM, this means one of the 10 test terminals on the TEST BD. in board slot 0. All voltages are to be measured with respect to negative, TEST TERM 10. Voltage measurements may vary by ±10%. Information in this acceptance test applies to a relay with a transient blocking time of 18 MS for relays with a transient blocking time of 25 MS, limits are 24 to 27 milliseconds.

A. Normal Condition

TEST TERM 1: 0 Volts
" " 2: 20 Volts
" " 3: 0 Volts
" " 4: 0 Volts
" " 5: 0 Volts
" " 6: 0 Volts
" " 7: 0 Volts
" " 8: 20 Volts
" " 9: 20 Volts

Keying AR - not picked up

Trip AR - not picked up

Loss of Channel AL - picked up (Elec-Mech system)

Loss of Potential AL - picked up - (Elec-Mech System)

B. Channel Logic - 2 Term Line Relays Only

(For 3 term. line relays, disregard this section and continue on section C)

1. TCF Carrier Channel

a. Channel Trip - 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer

Close Trip-1 switch

TEST TERM 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds, then rise from 0 to 20 volts in 3100 to 4100 milliseconds.

TEST TERM 4: Voltage rise from 0 to 20 volts.

Open Trip 1 switch

b. Loss of Channel

Open Low Signal - 1 Switch

TEST TERM 6: Voltage rise from 0 to 20 volts

Loss of Channel AL will drop out

Close LOW SIGNAL - 1 Switch

2. Tone **Channel**

a. Channel Trip - 2500/MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer

Close Trip-1 switch

TEST TERM 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds, then rise from 0 to 20 volts in 3100 to 4100 milliseconds

TEST TERM 4: Voltage rise from 0 to 20 volts

Open Trip-1 switch

b. Loss of Channel - 150/100 MS timer (CH. SUPV. BD.)

Open LOW SIGNAL - 1 switch

TEST TERM 6: Voltage rise from 0 to 20 volts in 130 to 180 milliseconds

Loss of Channel AL will drop out

Close LOW SIGNAL - 1 switch

TEST TERM 6: Voltage drop from 20 to 0 volts in 75 to 125 milliseconds.

c. Block return

Open LOW SIGNAL - 1 switch, then close Trip-1 switch

TEST TERM 4: Voltage must remain at zero.

Close LOW SIGNAL - 1 switch

TEST TERM 6: Voltage must remain at 20 volts

Open Trip-1 switch

TEST TERM 6: Voltage must drop from 20 to 0 volts

C. Channel Logic - 3 Term Line Relays Only

(For 2 term line relays, the preceding section was used and this part may be disregarded)

1. TCF Carrier Channel

a. Channel 1 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer

Close Trip-1 switch

TEST TERM 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds.

TEST TERM 4: Voltage remains at zero

Open Trip - 1 switch

b. Channel 2 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer.

Close Trip-2 switch

TEST TERM 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds

TEST TERM 4: Voltage remains at zero

Open Trip - 2 switch

c. Channel 1 and 2 Loss of Channel

Open LOW SIGNAL - 1 switch

TEST TERM 6: Voltage rise from 0 to 20 volts

Loss of Channel AL must drop out.

Close LOW SIGNAL - 1 switch, then open LOW SIGNAL 2 switch

TEST TERM 6: Voltage rise from 0 to 20 volts

Loss of Channel AL must drop out

Close LOW SIGNAL - 2 switch

d. Channel 1 and 2 trip

Close Trip-1 and Trip-2 switches

TEST TERM 4: Voltage rise from 0 to 20 volts

Open Trip-1 and Trip-2 switches

2. Tone Channel

a. Channel 1 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer

Close Trip-1 switch

TEST TERM 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds.

TEST TERM 4: Voltage remain at zero.

Open Trip-1 switch

b. Channel 2 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer.

Close Trip-2 switch

TEST TERM 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds.

TEST TERM 4: Voltage remain at zero.

Open Trip-2 switch

c. Block Return - Channel 1 - Trip and Low Signal - 150/100 MS Timer

Open LOW SIGNAL - 1 switch

TEST TERM 6: voltage rise from 0 to 20 volts in 130 to 180 milliseconds.

Loss of Channel AL must drop out

Close TRIP-1 switch, then close LOW SIGNAL - 1 switch

TEST TERM 6: voltage must remain at 20 volts

Open TRIP-1 switch

TEST TERM 6: voltage must drop from 20 to 0 volts in 75 to 125 milliseconds.

d. Block Return - Channel 2 - Trip and Low Signal - 150/100 MS Timer

Open LOW SIGNAL - 2 switch

TEST TERM 6: voltage rise from 0 to 20 volts in 130 to 180 milliseconds

Loss of Channel AL must drop out

Close TRIP-1 switch, then close LOW SIGNAL - 1 switch

TEST TERM 6: voltage must remain at 20 volts

Open TRIP-1 switch

TEST TERM 6: voltage must drop from 20 to 0 volts in 75 to 125 milliseconds.

e. Channel 1 and 2 - TRIP and LOW SIGNAL

Close TRIP-1 and TRIP-2 switches

TEST TERM 4: voltage rise from 0 to 20 volts

Open LOW SIGNAL - 1 switch

TEST TERM 4: voltage drop from 20 to 0 volts

◆ Open TRIP-1 and TRIP-2 switches, then close LOW SIGNAL-1 switch

D. Distance Relay Operation

a. Distance relay operation loss of potential 500/0 MS timer

Close PR-1 switch

TEST TERM 7: voltage rise from 0 to 20 volts in 400 to 600 milliseconds

Loss of Potential AL must drop out

TEST TERM 3 & 5: voltage rise from 0 to 20 volts immediately, and then drop from 20 to 0 volts in 400 to 600 milliseconds

XMTR KEY AR picks up immediately then drops out in 400 to 600 milliseconds

Open PR-1 switch

The same as the preceding must happen by closing either the PR-2 or PR-3 switch

b. Distance Relay Operation - no Loss of Potential

Close TRIP-1 and TRIP-2 switches
(TRIP-2 switch not required for 2 TERM LINE relays)

Close either PR-1, PR-2, or PR-3 switches

TEST TERM 7: voltage must remain at zero, the Loss of Potential timer must not pickup.

Open TRIP-1, TRIP-2, and PR switches.

E. Test Switch Operation - 2500/0 MS timer (CHECK BACK BD.)
0/1000 MS timer (ARMING BD.)
18/0 transient Blocking timer (OUTPUT BD.)

Close TEST Switch

TEST TERM 3: voltage must rise from 0 to 20 volts

TEST TERM 2: voltage must drop from 20 to 0 volts in 18 to 20 milliseconds

TEST TERM 5: voltage must rise from 0 to 20 volts immediately, then drop from 20 to 0 volts in 2000 to 3000 milliseconds

Also, XMTR KEY AR must pickup for 2 to 3 seconds

Open TEST Switch

TEST TERM 2: voltage must rise from 0 to 20 volts in 900 to 1300 milliseconds

F. 52b Contact Operation - 180/0 MS timer (TIMING BD.)

Close 52b switch

TEST TERM 5: voltage must rise from 0 to 20 volts in 180 to 230 milliseconds

Open 52b switch

G. Channel Checkback **Operation**

1. TCF Carrier Channel
2500/2500 MS timer (CHECKBACK BD.)
Check Trip Inputs

Open LOW SIGNAL - 1 switch

TP4 on CHECKBACK BD: voltage must drop from 8 to 0 volts in 2000 to 3000 milliseconds

Close CK TRIP-1 switch

TEST TERM 5: voltage must rise from 0 to 20 volts immediately, then drop from 20 to 0 volts in 2000 to 3000 milliseconds

XMTR KEY AR must pickup for 2 to 3 seconds

Close LOW SIGNAL - 1 switch, then open CK TRIP-1 switch

For relay used for 3 TERM LINE, also do the following

Open LOW SIGNAL-2 switch and wait for 3 seconds, then close CK TRIP-2 switch

TEST TERM 5: voltage must rise from 0 to 20 volts immediately, then drop from 20 to 0 volts in 2 to 3 seconds.

Close LOW SIGNAL - 2 switch, then open CK TRIP-2 switch

2. Tone Channel
2500/2500 MS timer (CHECKBACK BD.)

Open LOW SIGNAL - 1 switch

TP4 on CHECKBACK BD: voltage must drop from 8 to 0 volts in 2000 to 3000 milliseconds

Close TRIP-1 switch, then close LOW signal-1 switch

TEST TERM 5: voltage must rise from 0 to 20 volts immediately then drop from 20 to 0 volts in 2000 to 3000 milliseconds.

XMTR KEY AR must pickup for 2 to 3 seconds

Open TRIP-1 switch

For relays used for 3 TERM LINE, also do the following:

Open both LOW SIGNAL-1 and LOW SIGNAL-2 switches then close TRIP-2 switch. Wait for 3 seconds, then close both LOW SIGNAL 1 and LOW SIGNAL 2 switches.

TEST TERM 5: voltage must rise from 0 to 20 volts immediately after closing both the LOW SIGNAL switches, then drop from 20 to 0 volts in 2 to 3 seconds

Open TRIP-2 switch

H. PILOT TRIP 4/0 MS timer (OUTPUT BD.)

Close 52b switch in order to prevent the 2500/0 timer from starting transient blocking

Close TRIP-1 switch, and also, for 3 TERM LINE relays, close TRIP-2 switch

Then, close TEST switch

TEST TERM 1: voltage must rise from 0 to 20 volts in 4.0 to 4.5 milli-seconds.

TRIP AR must pick up

Open TRIP-1 and TRIP-2 switches

TEST TERM 1: voltage must remain at 20 volts

Open TEST switch and TRIP AR must drop out.
Open 52b switch

I. Pilot Trip after Transient Unblocking 18/0 MS timer (OUTPUT BD)

Close TEST switch

Then, close TRIP-1 switch, and also for 3 TERM LINE relays, close TRIP-2 switch.

TEST TERM 1: voltage rise from 0 to 20 volts in 18 to 20 milliseconds

Open TEST switch

TEST TERM 1: voltage drop from 20 to 0 volts

Open TRIP-1 and TRIP-2 switches

J. Continue Key after Pilot Trip - 0/30 MS timer (TIMING BD.)

Close TEST switch, then wait until XMTR KEY AR drops out.

Then close TRIP-1 switch and for 3 TERM LINE relays, also close TRIP-2 switch

As soon as the voltage on TEST TERM 1 rises from 0 to 20 volts, then the 0/30 MS timer will pickup in less than 1 millisecond and the voltage at TEST TERM 5 will rise from 0 to 20 volts.

Then open TEST switch

TEST TERM 5: voltage must drop from 20 to 0 volts in 24 to 30 milliseconds.

Open TRIP-1 and TRIP-2 switches

K. Fast reset of 0/1000 MS timer after pilot trip. 0/100 MS timer (ARMING BD.)

For checking this 0/100 MS timer, it will be necessary to use a jumper.

Close TEST switch, then close TRIP-1 switch and also for 3 TERM LINE relays close TRIP-2 switch

Terminal 4 (ARMING BD.): voltage must rise from 0 to 16 volts in less than 2 milliseconds after the voltage at TEST TERM 1 rises from 0 to 20 volts.

In order to check the 100 millisecond reset time, it is necessary to connect a jumper from TP-8 to terminal 14 on the ARMING BD.

Open TEST switch

Terminal 4 (ARMING BD.) voltage must drop from 16 to 0 volts in 70 to 170 milliseconds

Open TRIP-1 and TRIP-2 switches, and remove the jumper.

L. Elec-Mech Interface 0/25 and 20/0 MS timers (Elec-Mech (E.M.)INTERFACE BD.)

This section is to be used only for those STU relays which are for use with electromechanical distance relays.

Close PR-1, PR-2 or PR-3 switches

Terminal 4 (E.M. INTERFACE BD.): voltage must rise from 0 to 11 volts immediately then drop back to zero in 16 to 24 milliseconds

Open PR-1, PR-2, and PR-3 switches

Terminal 4 (E.M. INTERFACE BD.): voltage must remain at zero

M. Unblock timer for Reclosure 0/150 MS timer (CH. SUPV. BD.)

Close 52b switch, and open LOW SIGNAL-1 switch. This will set up the AND on the CH. SUPV. BD.

Now, open 52b switch

TEST TERM 4: voltage must rise from 0 to 20 volts immediately, then drop back to zero in 130 to 180 milliseconds

Close LOW SIGNAL-1 switch

N. NOISE operation - (Tones Only)

This section is to be used only for those STU relays which are for use with a frequency shift tone channel.

Close NOISE-1 switch

Then close TEST switch and TRIP-1 switch, and also for 3 TERM LINE relays close TRIP-2 switch

TEST TERM 1: voltage must remain at zero

Open NOISE-1 switch

TEST TERM 1: voltage must rise from 0 to 20 volts

Trip AR must pickup

Open TEST, TRIP-1, and TRIP-2 switches

For 3 TERM LINE relays, repeat above test using NOISE-2 switch instead of NOISE-1 switch

Recommended Routine Maintenance

Periodic checks of the relay system are desirable to indicate impending failure so that the equipment can be taken out of service for correction. Any accumulated dust should be removed at regular maintenance intervals.

All contacts should be periodically cleaned. A contact burnisher, style No. 182A836H01, is recommened. The use of abrasive material is not recommended because of the danger of embedding small particles in the face of the soft silver and thus impairing the contact.

CALIBRATION

The proper adjustments to insure correct operation of the relay have been made at the factory and should not be disturbed after receipt by the customer. However, if the adjustments or if the components or printed circuit boards which affect calibration have been changed, then the STU relay should be rechecked per the acceptance check information.

All time delays are fixed except for the three timers on the OUTPUT BD.:

18/0 MS trandient blocking timer, 18/0 MS transient unblocking timer, and the 4/0 MS trip timer. These adjustable timers can be recalibrated as follows using an auxiliary timer or oscilloscope.

Transient block 18/0 MS timer - OUTPUT BD.

(NOTE: For relays having a transient blocking timer of 25/0 MS limits are 24 to 27 milliseconds)

Start timer on TEST switch (positive pulse)
End timer on TEST TERM 2 (negative pulse)

Close TEST switch and the voltage on TEST TERM 2 must drop from 20 to 0 volts in 18 to 20 milliseconds (24 to 27 MS)

This time can be adjusted by turning potentiometer R14 on the OUTPUT BD. clockwise for more time or counter-clockwise for less time.

Pilot trip 4/0 MS time - OUTPUT BD.

Start timer on TEST SWITCH
End timer on TEST TERM 1

For this calibration, close 52b switch

Close TRIP-1 switch and also TRIP-2 switch for 3 TERM LINE relays.

Then close TEST switch and the voltage on TEST TERM 1 must rise from 0 to 20 volts in 4.0 to 4.5 milliseconds

This time can be adjusted by turning potentiometer R20 on the OUTPUT BD. clockwise for more time or counter-clockwise for less time.

Transient unblocking 18/0 MS timer - OUTPUT BD.

Start timer on TRIP-1 switch
End timer on TEST TERM 1

Close TEST switch, and also close TRIP-2 switch for 3 TERM LINE relays

Then close TRIP-1 switch and the voltage on TEST TERM 1 must rise from 0 to 20 volts in 18 to 20 milliseconds

This time can be adjusted by turning potentiometer R1 on the OUTPUT BD. clockwise for more time and counter-clockwise for less time.

Tripping Relay (AR)

The type AR tripping relay unit has been properly adjusted at the factory to insure correct operation and should not be disturbed after receipt by the customer. If, however, the adjustments are disturbed in error, or it becomes necessary to replace some part in the field, use the following adjustment procedure. This procedure should not be used until it is apparent that the AR unit is not in proper working order, and then only if suitable tools are available for checking the adjustments.

a. Adjust the set screw at the top of the frame to obtain a 0.009 inch gap at the rear end of the armature air gap.

b. Adjust each contact spring to obtain 4 grams pressure at the very end of the spring. This pressure is measured when the spring moves away from the edge of the slot in the insulated crosspiece.

c. Adjust each stationary contact screw to obtain a contact gap of 0.020 inch. This will give 15-30 grams contact pressure.

Trouble Shooting

The components of the STU relay are operated well within their ratings and normally will give long and trouble-free service. However, if a relay has given an indication of trouble in service or during routine checks, then using "0" and "1" logic notation, the faulty, printed circuit board can be traced to using the diagrams in Fig. 4, 5, 6, or 7. In turn, the faulty component or circuit can be found using the individual schematics of the printed circuit boards, which show the detailed transistor NOR/NAND logic.

Each NOR/NAND logic block represents a transistor on the schematic. The output of each individual logic block is the collector of the transistor which represents that block. The collector of each transistor is either connected to a test point or printed circuit terminal. A box around the transistor indicates that it is conducting for the normal condition of the relay.

Following is an explanation of the voltage levels for the "0" and "1" logic notation as shown for the normal relay condition in Figures 4, 5, 6, and 7. This logic notation will also apply to the detailed logic on the printed circuit board internal schematics.

For positive logic - represented by logic blocks, with no arrows.

"0" is equivalent to less than 0.5 volts with respect to negative, TEST TERM 10.

"1" is equivalent to 8 to 20 volts with respect to negative, TEST TERM 10.

For negative logic - represented by logic blocks with open arrow heads

"0" is equivalent to 8 to 20 volts with respect to negative, TEST TERM 10, except for the output of the relay driver, where a "0" is rated positive dc.

"1" is equivalent to less than 0.5 volts with respect to negative, TEST TERM 10.

A board extender, style No. 849A534G01, is available for facilitating circuit voltage measurements. After withdrawing any one of the circuit boards, the extender is inserted into that slot. The board is then inserted into the terminal block on the front of the extender to restore all circuit connections.

The TEST TERMINAL'S on the TEST BD. in the board position to the extreme right are helpful in checking the overall relay operation. Following are the voltages that will occur at these TEST TERM's under various conditions:

NOTE: All voltages referred to are taken from respect to negative, TEST TERM 10

TEST TERM 1: PILOT TRIP

Normal Condition - 0 volts

Internal Fault - 20 volts

For an internal fault, either a distance relay or test switch operation and both receiver trip signals (one receiver trip signal for 2 TERM LINE relays) are required.

TEST TERM 2: TRANSIET BLOCKING & UNBLOCKING

Normal Condition - 20 volts

External Fault - 0 volts

The following will simulate an external fault:

- Distance relay operation
- Test switch operation
- Either channel receiver trip operation

TEST TERM 3: PROTECTIVE RELAY

Normal Condition - 0 volts

Distance relay operation - 20 volts

Test Switch Operation - 20 volts

TEST TERM 4: CHANNEL TRIP

Normal Condition - 0 volts

Operation of Channel 1 and 2 receiver trip

Outputs - (for 2 TERM Line Relays, only Channel 1 required) - 20 volts

TEST TERM 5: XMTR KEY

Normal Condition - 0 volts

Distance relay operation - 20 volts

52b contact operation - 20 volts

Internal Fault
(pilot trip signal) - 20 volts

Test Switch Operation - 20 volts for 2.5 seconds

Channel checkback scheme - 20 volts for 2.5 seconds

TEST TERM 6: LOSS OF CHANNEL

Normal Condition - 0 volts

Operation of either Channel 1 or 2
Low Signal Clamp - 20 volts

TEST TERM 7: LOSS OF POTENTIAL

Normal Condition - 0 volts

Distance Relay Operation - 20 volts after 500 MS time delay

Distance relay and both receiver trip signal
Operation (one receiver trip signal for 2 TERM LINE relays) - 0 volts

TEST TERM 8 and 9: POS. 20 V DC

Normal Condition: 18 to 21 volts

TEST TERM 10: NEGATIVE DC

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing the repair work. When ordering parts, always give the complete nameplate data, and the component style no. given in the Electrical Parts List.

ELECTRICAL PARTS LIST

Power Supply Board (S# 202C465G01)

Circuit Symbol	Reference	Style
	CAPACITORS	
C1, C2	6.8 MFD, 35 V, ±20%	184A761H10
	DIODES	
D1, D2	1N645A	837A692H03
	RESISTORS	
None on PCB	None	
	TRANSISTORS	
Q1, Q2	2N3589	837A617H01
Heat Sink for Q1, Q2		849A517H01
	ZENER DIODE	
Z1, Z3	1N3050A (180 V - 1W)	187A936H16
Z2, Z4	1N4747A (20 V - 1W)	849A487H01

Protective Relay (S# 202C466G01) - Solid State Systems
Interface Board (S# 202C475G01) - Elec-Mech Systems

Circuit Symbol	Reference	Style
	CAPACITORS	
C1, C2	.047 MFD, 200 V DC	849A437H04
	DIODES	
D1, D2	1N645A	837A692H03
	RESISTORS	
R1, R2, R3 △	4.7 K, ½W, ±2%	629A531H48
R1, R2, R3 #	47 K, ½W, ±2%	629A531H72
R4, R15, R16	4.7 K, ½W, ±2%	629A531H48
R5, R17, R22	82 K, ½W, ±2%	629A531H78
R6, R9, R13, R19, R20	10 K, ½W, ±2%	629A531H56
R7, R10, R14, R21	6.8 K, ½W, ±2%	629A531H52
R8, R11, R12, R18	27 K, ½W, ±2%	629A531H66
	TRANSISTORS	
Q1, Q2, Q3, Q4	2N3417	848A851H02
Q5	2N3645	849A441H01

ELECTRICAL PARTS LIST

Protective Relay (S# 202C466G01) - Solid State Systems
Interface Board (S# 202C475G01) - Elec-Mech Systems

Circuit Symbol	Reference	Style
	ZENER DIODES	
Z1, Z2, Z3	1N3688A, 29 V, ±10%	862A288H01
Z4, Z6	1N3686B, 20 V, ±5%	185A212H06
Z5, Z7	1N957B, 6.8 V, ±5%	186A797H06

Δ - Solid State Systems
\# - Elec-Mech Systems

Loss of Potential Board (S# 202C467G01) - Elec-Mech Systems
(S# 202C529G01) - Solid State Systems

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	22 MFD, 35 V	184A661H16
C2	.27 MFD, 200 V DC	188A669H05
	DIODES	
D1, D2	1N645A	837A692H03
	RESISTORS	
R1, R4, R5, R14	27 K, ½W, ±2%	629A531H66
R2, R6, R9, R10 R15, R18	10 K, ½W, ±2%	629A531H56
R3, R11, R16	6.8 K, ½W, ±2%	629A531H52
R7 Δ	43 K, ½W, ±2%	629A531H71
R8	470 ohm, ½W, ±2%	629A531H24
R12	82 K, ½W, ±2%	629A531H78
R13	150 ohm, 3W, ±5%	762A679H01
R17	1 K, ½W, ±2%	629A531H32
	TRANSISTORS	
Q1, Q2, Q3, Q5	2N3417	848A851H02
Q4	2N3645	849A441H01
Q6	2N3589	837A617H01
	ZENER DIODES	
Z1	1N957B, 6.8 V, ±5%	186A797H06
Z2	1N3688A, 24 V, ±10%	862A288H01
Z3	1N3050B, 180 V	187A936H17

ELECTRICAL PARTS LIST

Loss of (S# 202C467G01) - Elec-Mech Systems (continued)
Potential Board (S# 202C529G01) - Solid State Systems

Δ - Indicates Typical Value

Elec-Mech Interface Board (S# 202C468G01)

Circuit Symbol	Reference	Style
	CAPACITORS	
C1, C2	1.5 MFD, 35 V, ±5%	187A508H18
	DIODES	
D1, D2, D3, D4, D5	1N645A	837A692H03
	RESISTORS	
R1	27 K, ½W, ±2%	629A531H66
R2, R5, R9, R12 R14, R15	10 K, ½W, ±2%	629A531H56
R3 Δ	30 K, ½W, ±2%	629A531H67
R4	22 ohm, ½W, ±5%	187A290H09
R6	12 K, ½W, ±2%	629A531H58
R7 Δ	12 K, ½W, ±2%	629A531H58
R8	470 ohm, ½W, ±2%	629A531H24
R10, R11, R13	22 K, ½W, ±2%	629A531H64
R16	6.8 K, ½W, ±2%	629A531H52
	TRANSISTORS	
Q1, Q2, Q3, Q4, Q5	2N3417	848A851H02
	ZENER DIODES	
Z1, Z2	1N957B	186A797H06

Δ - Indicates Typical Value

Channel (S# 202C530G01) - TCF Int.
Interface Board (S# 202C469G01) - TA3 Int.

Circuit Symbol	Reference	Style
	CAPACITORS	
C1, C3, C5	.047 MFD, 200 V DC	849A437H04
C4, C6	.27 MFD, 200 V DC	188A669H05

ELECTRICAL PARTS LIST

Channel Interface Board (S# 202C530G01) - TCF Int. (continued)
(S# 202C469G01) - TA3 Int.

Circuit Symbol	Reference	Style
	DIODES	
D2, D3	1N645A	837A692H03
	RESISTORS	
R1, R2, R9, R10 R17, R18	4.7 K, ½W, ±2%	629A531H48
R3, R7, R11, R15 R19, R23	82 K, ½W, ±2%	629A531H78
R4, R5, R12, R13 R20, R21, R26	10 K, ½W, ±2%	629A531H56
R6, R14, R22, R27	6.8 K, ½W, ±2%	629A531H52
R16, R24	150 ohm, 3 W, ±5%	762A679H01
R25	27 K, ½W, ±2%	629A531H66
	TRANSISTORS	
Q1, Q3, Q5, Q7	2N3417	848A851H02
Q2, Q4, Q6	2N3645	849A441H01
	ZENER DIODES	
Z1, Z4, Z7	1N3686B, 20 V, ±5%	185A212H06
Z2, Z5, Z8	1N957B, 6.8 V, ±5%	186A797H06
Z6, Z9, Z10	1N3688A, 24 V, ±20%	862A288H01

Channel Trip Board (S# 202C471G01) - TCF
(S# 202C472G01) - Tone

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	0.27 MFD, 200 V.	188A669H05
	DIODES	
D1	1N645A	837A692H03
	RESISTORS	
R1, R2, R5, R8, R11, R14, R17, R32, R33, R34, R37, R43	27 K, ½W, ±2%	629A531H66
R3, R6, R9, R12, R15 R19, R23, R27, R30, R35 R38, R39	10 K, ½W, ±2%	629A531H56

ELECTRICAL PARTS LIST

Channel (S# 202C471G01) - TCF (continued)
Trip Board (S# 202C472G01) - Tone

Circuit Symbol	Reference	Style
	RESISTORS	
R4, R7, R10, R13 R16, R20, R24, R28, R31, R36, R40	6.8 K, ½W, ±2%	629A531H52
R41	82 K, ½W, ±2%	629A531H78
R42	150 ohm, 3 W, ±5%	762A679H01
	TRANSISTORS	
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11	2N3417	848A851H02
Q12	2N3645	849A441H01
	ZENER DIODES	
Z1	1N3688A, 24 V, ±10%	862A288H01

TCF Channel (S# 202C473G01) - Elec-Mech Systems
Supv. Board (S# 202C531G01) - Solid State System

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	6.8 MFD, 35 V, ±5%	184A661H21
	DIODES	
D1, D2, D3	1N645A	837A692H03
	RESISTORS	
R1, R2, R6, R9, R14, R18, R19, R22, R23, R26	27 K, ½W, ±2%	629A531H66
R3, R4, R7, R10, R13 R15, R20, R24, R27	10 K, ½W, ±2%	629A531H56
R5, R8, R11, R21, R25, R28	6.8 K, ½W, ±2%	629A531H52
R12	1 K, ½W, ±2%	629A531H32
R17	470 ohm, ½W, ±2%	629A531H24
R16 Δ	43 K, ½W, ±2%	629A531H71
	TRANSISTORS	
Q1, Q3, Q4, Q6, Q7 Q8, Q9	2N3417	848A851H02

ELECTRICAL PARTS LIST

TCF Channel (S# 202C473G01) - Elec-Mech Systems (continued)
Supv. Board (S# 202C531G01) - Solid State System

Circuit Symbol	Reference	Style
	TRANSISTORS	
Q2	2N3645	849A851H02
Q5	2N3589	837A617H01
	ZENER DIODES	
Z1	1N3050B, 180 V.	187A936H17
Z2	1N957B, 6.8 V, ±5%	186A797H06

Δ - Indicates Typical Value

Tone Channel (S# 203C253G01) - Elec-Mech or
Supv. Board Solid State Systems

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	12 MFD, 35 V, ±10%	862A530H05
C2	6.8 MFD, 35 V, ±5%	184A661H21
	DIODES	
D1, D2, D3, D4, D5, D6	1N645A	837A692H03
	RESISTORS	
R1, R2, R3, R6 R15, R20, R23, R24, R25, R28, R29, R32, R35, R39	27 K, ½W, ±2%	629A531H66
R4, R7, R12, R13 R16, R19, R21, R26, R30, R33, R36, R41	10 K, ½W, ±2%	629A531H56
R5, R8, R14, R22, R27, R31, R34, R42	6.8 K, ½W, ±2%	629A531H52
R9 Δ	22 K, ½W, ±2%	629A531H64
R10 Δ	10 K, ½W, ±2%	629A531H56
R11	15 K, ½W, ±2%	629A531H60
R17	5.6 K, ½W, ±2%	629A531H50
R18	1 K, ½W, ±2%	629A531H32
R37 Δ	43 K, ½W, ±2%	629H531H71
R38	470 ohms, ½W, ±2%	629A531H24
R40	12 K, ½W, ±2%	629A531H58

ELECTRICAL PARTS LIST

Tone Channel (S# 203C253G01) - Elec-Mech or (continued)
Supv. Board Solid State Systems

Circuit Symbol	Reference	Style
	TRANSISTORS	
Q1, Q2, Q3, Q5 Q7, Q8, Q9, Q10, Q11, Q12	2N3417	848A851H02
Q4	2N3645	849A441H01
Q6	2N3589	837A617H01
	ZENER DIODES	
Z1, Z3	1N957B, 6.8 V, ±5%	186A797H06
Z2	1N3050B, 180 V	187A936H17

△ - Indicates Typical Valve

Transmitter (S# 202C534G01) - TCF Ch.
Key Board (S# 202C535G01) - Tone Ch.

Circuit Symbol	Reference	Style
	CAPACITORS	
C1, C2	0.27 MFD, 200 V DC	188A669H05
	DIODES	
D1, D2, D3, D4, D5, D6, D7	1N645A	837A692H03
	RESISTORS	
R1, R2, R3, R4, R5, R6, R7, R13	27 K, ½W, ±2%	629A531H66
R8, R9, R12, R14, R15, R20	10 K, ½W, ±2%	629A531H56
R10, R11, R16	6.8 K, ½W, ±2%	629A531H52
R17	82 K, ½W, ±2%	629A531H78
R18	150 ohm, 3W, ±5%	762A679H01
R19	4.7 K, ½W, ±2%	629A531H48
	TRANSISTORS	
Q1, Q4	2N3417	848A851H02
Q2, Q5	2N3645	849A441H01
Q3, Q6	2N3589	837A617H01

ELECTRICAL PARTS LIST

Transmitter (S# 202C534G01) - TCF Ch. - (continued)
Key Board (S# 202C535G01) - Tone Ch.

Circuit Symbol	Reference	Style
	ZENER DIODES	
Z1, Z3	1N3688A, 24 V, ±10%	862A288H01
Z2, Z4	1N3050B, 180 V	187A936H17

Checkback Board (S# 202C476G01)

Circuit Symbol	Reference	Style
	CAPACITORS	
C1, C2, C4	150 MFD, 35 V	849A007H01
C3	.047 MFD, 200 V DC	849A437H04
	DIODES	
D1, D2, D3, D4, D5, D6	1N645A	837A692H03
	RESISTORS	
R1, R4, R7, R8, R15, R23, R27	27 K, ½W, ±2%	629A531H66
R2, R5, R9, R12, R16, R21, R24, R28	10 K, ½W, ±2%	629A531H56
R3, R6, R17, R22 R29	6.8 K, ½W, ±2%	629A531H52
R10 Δ, R13 Δ, R25 Δ	33 K, ½W, ±2%	629A531H68
R11, R14, R26	470 ohm, ½W, ±2%	629A531H24
R18, R19	4.7 K, ½W, ±2%	629A531H48
R20	82 K, ½W, ±2%	629A531H78
	TRANSISTORS	
Q1, Q2, Q3, Q4, Q5 Q6, Q7, Q8	2N3417	848A851H02
	ZENER DIODES	
Z1, Z2, Z4, Z5	1N957B, 6.8 V, ±5%	186A797H06
Z3	1N3686B, 20 V, ±5%	185A212H06

Δ - Indicates Typical Value

ELECTRICAL PARTS LIST

Timing Board (S# 202C477G01)

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	.047 MFD, 200 V	849A437H04
C2	12 MFD, 35 V, ±10%	862A530H05
C3	1.5 MFD, 35 V, ±5%	187A508H18
C4	150 MFD, 30 V, ±10%	849A007H01
C5	1.0 MFD, 35 V, ±10%	837A241H15
	DIODES	
D1, D2, D3, D4, D5	1N645A	837A692H03
	RESISTORS	
R1, R2	4.7 K, ½W, ±2%	629A531H48
R3	82 K, ½W, ±2%	629A531H78
R4, R7, R10, R13 R16, R19, R22, R25, R28, R33	10 K, ½W, ±2%	629A531H56
R5, R8, R14, R17, R23, R26, R34	6.8 K, ½W, ±2%	629A531H52
R6, R9, R15, R18, R24, R27, R31, R32, R35	27 K, ½W, ±2%	629A531H66
R11	30 K, ½W, ±2%	629A531H67
R12, R21, R30	470 ohm, ½W, ±2%	629A531H24
R20 Δ, R29 Δ	33 K, ½W, ±2%	629A531H68
	TRANSISTORS	
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10	2N3417	848A851H02
	ZENER DIODES	
Z1	1N3686B, 20 V, ±5%	185A212H06
Z2, Z3, Z4, Z5	1N957B, 6.8 V, ±5%	186A797H06

Δ - Indicates Typical Value

ELECTRICAL PARTS LIST

Arming Board (S# 202C478G01)

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	22 MFD, 35 V, ±10%	184A661H16
C2	3.3 MFD, 35 V, ±5%	862A530H01
	DIODES	
D1, D2, D3, D4, D5	1N645A	837A692H03
	RESISTORS	
R1, R2, R5, R8, R9, R10, R16, R20, R23 R24, R25	27 K, ½W, ±2%	629A531H66
R3, R6, R11, R12, R18, R21, R26, R27, R32, R36	10 K, ½W, ±2%	629A531H56
R4, R7, R13, R19, R22, R28, R33	6.8 K, ½W, ±2%	629A531H52
R14	82 K, ½W, ±2%	629A531H78
R15	20 K, ½W, ±2%	629A531H63
R29, R34	1 K, ½W, ±2%	629A531H32
R30	100 ohm, ½W, ±2%	629A531H08
R31	15 K, ½W, ±2%	629A531H60
R35	12 K, ½W, ±2%	629A531H58
	TRANSISTORS	
Q1, Q2, Q3, Q5, Q6, Q7, Q9, Q10	2N3417	848A851H02
Q4, Q8	2N3645	849A441H01

▲ - Indicates Typical Value

Output Board (S# 202C479G01)

Circuit Symbol	Reference	Style
	CAPACITORS	
C1	1.5 MFD, 35 V, ±10%	187A508H18
C2, C4, C7	0.22 MFD, 100 V	763A219H21
C3	3.3 MFD, 35 V, ±10%	862A530H01
C6	0.047 MFD, 200 V.	849A437H04
C8, C9	0.1 MFD, 200 V	188A669H03
C10	0.27 MFD, 200 V	188A669H05

ELECTRICAL PARTS LIST

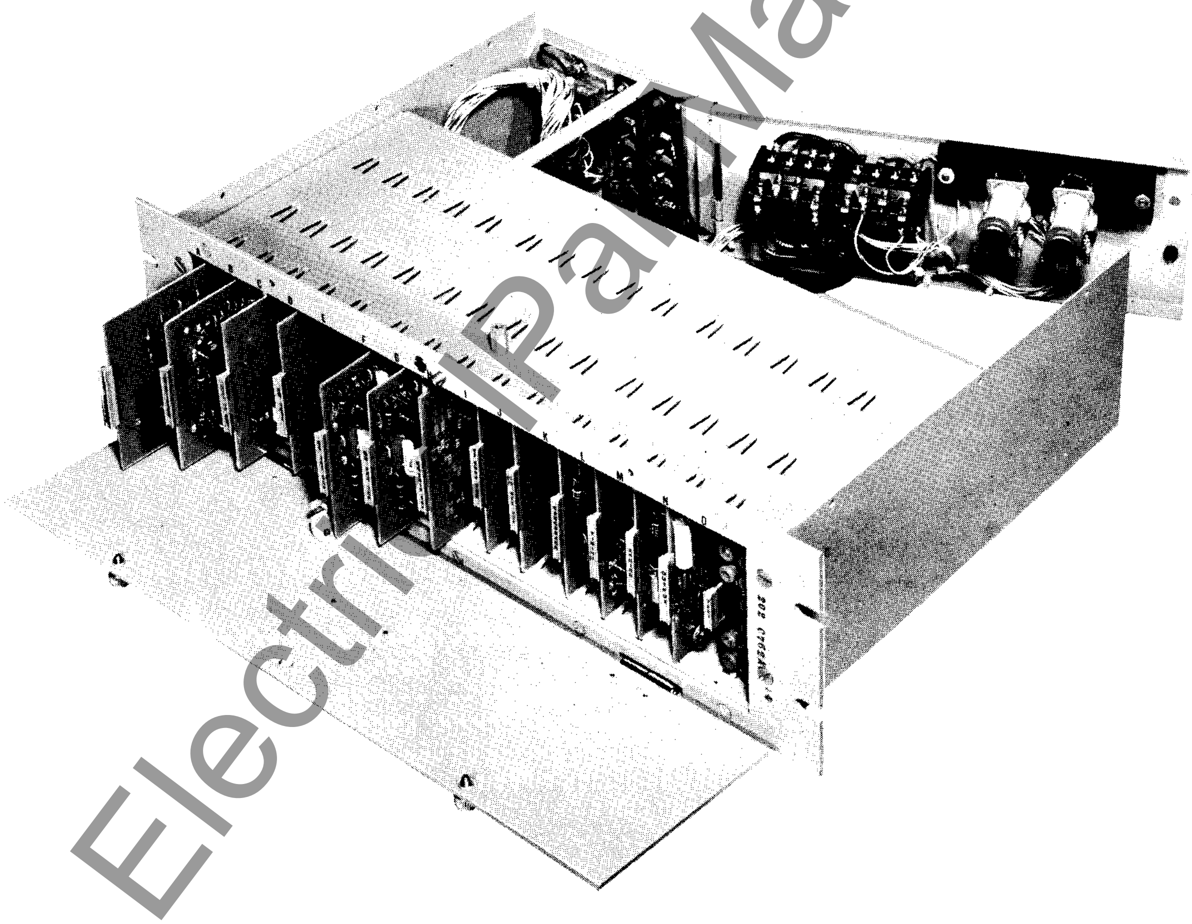
Output Board (S# 202C479G01) - (continued)

Circuit Symbol	Reference	Style
	DIODES	
D1, D2, D3, D4, D5, D6, D7, D8	1N645A	837A692H03
	POTENTIOMETERS	
R1	50 K, $\frac{1}{4}$ W, $\pm$20%	629A430H01
R14	15 K, $\frac{1}{4}$ W, $\pm$20%	629A430H08
R20	1 K, $\frac{1}{4}$ W, $\pm$20%	629A430H02
	RESISTORS	
R2, R7, R9, R12, R18, R21, R23, R24, R25, R26, R30, R31, R34, R36, R37	10 K, $\frac{1}{2}$W, $\pm$2%	629A531H56
R3	150 K, $\frac{1}{2}$W, $\pm$5%	629A531H84
R6	47 ohm, $\frac{1}{2}$W, $\pm$5%	187A290H17
R8, R35	27 K, $\frac{1}{2}$W, $\pm$2%	629A531H66
R10, R15	470 ohm, $\frac{1}{2}$W, $\pm$2%	629A531H24
R11	470 K, $\frac{1}{2}$W, $\pm$5%	184A763H91
R16, R28	4.7 K, $\frac{1}{2}$W, $\pm$2%	629A531H48
R4, R17, R19, R22, R29	22 K, $\frac{1}{2}$W, $\pm$2%	629A531H64
R5, R27, R32, R33, R38	6.8 K, $\frac{1}{2}$W, $\pm$2%	629A531H52
R39	82 K, $\frac{1}{2}$W, $\pm$2%	629A531H78
R40	150 ohm, 3W, $\pm$5%	762A679H01
R13	15 K, $\frac{1}{2}$W, $\pm$2%	629A531H60
	TRANSISTORS	
Q1, Q4, Q5, Q6, Q8, Q11	2N3645	849A441H01
Q2, Q3, Q7, Q10	2N3417	848A851H02
Q9	2N3589	837A617H01
	ZENER DIODES	
Z1, Z7	1N3688A, 24 V, $\pm$10%	862A288H01
Z2, Z3, Z4, Z5	1N957B, 6.8 V, $\pm$5%	186A797H06
Z6	1N3050B, 180 V	187A936H17

ELECTRICAL PARTS LIST

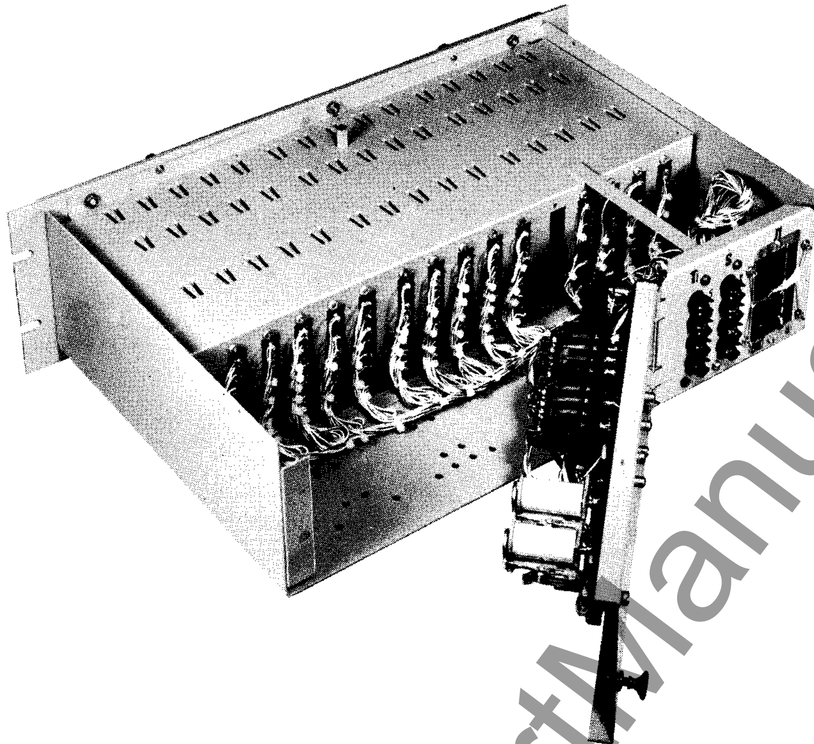
Test Board (S# 5490D87G01)

Circuit Symbol	Reference	Style
Tip Jacks (red) 1, 2, 3, 4, 5, 6, 7, 8, 9		187A332H01
Tip Jacks (black) 10		187A332H02



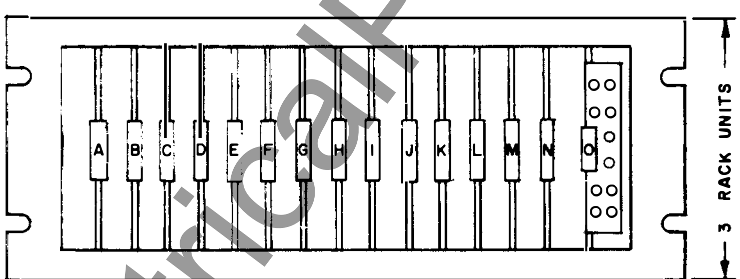
69-279

Fig. 1 Photograph (Front View with Door open).



69-280

Fig. 2 Photograph (rear view taken above relay with top cover off and door open).

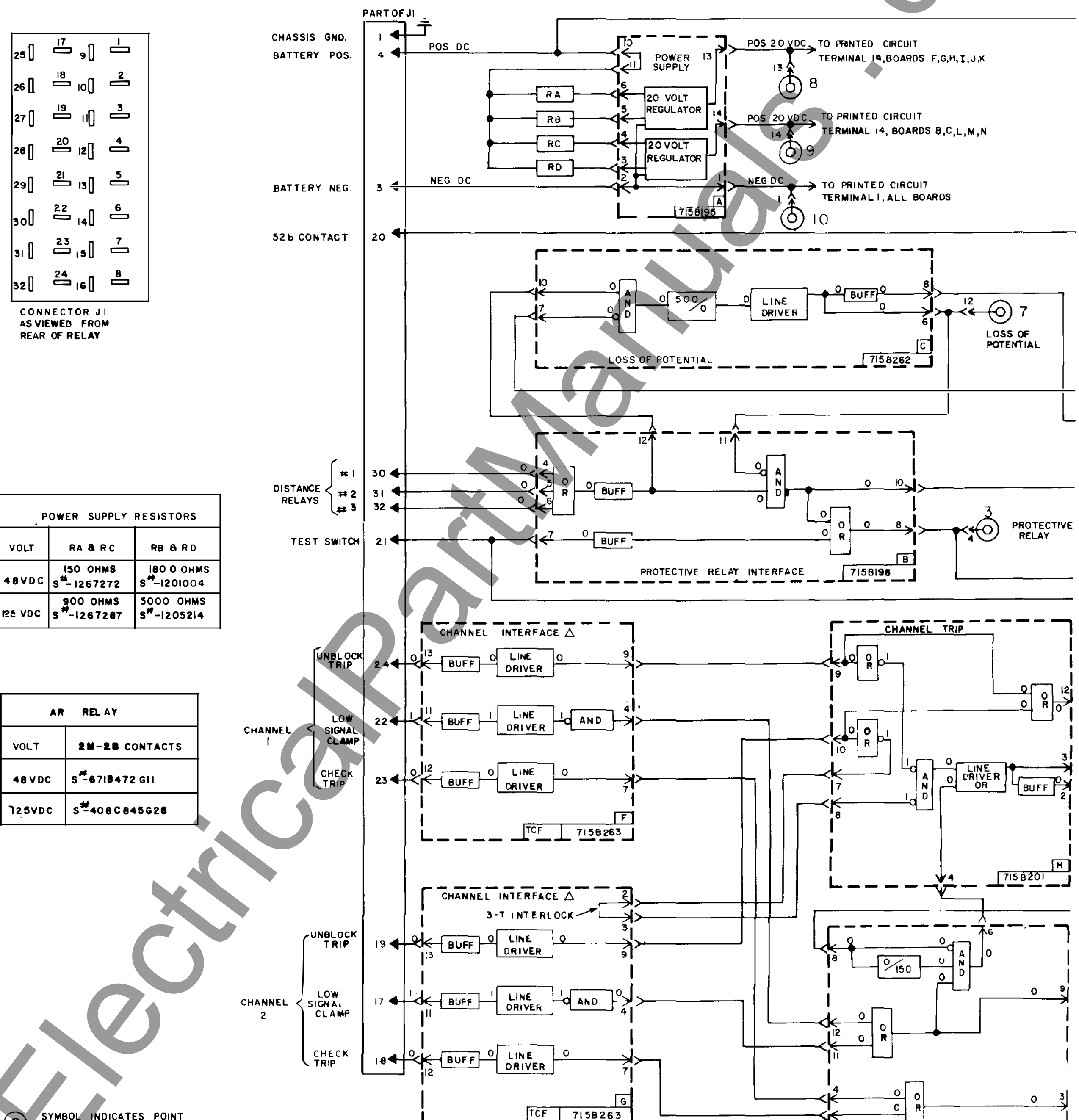


FRONT VIEW
(COVER REMOVED)

BOARD POSITION	BOARD DESCRIPTION
A	POWER SUPPLY
B	PROTECTIVE RELAY INTERFACE
C	LOSS OF POTENTIAL
D	ELEC. MECH. INTERFACE
E	———
F	CHANNEL 1 INTERFACE
G	CHANNEL 2 INTERFACE
H	CHANNEL TRIP
I	CHANNEL SUPERVISION
J	CHANNEL TRANSMITTER KEY
K	CHECK BACK
L	TIMING
M	ARMING
N	OUTPUT
O	TEST

876A611

Fig. 3 Relay Component Location.



POWER SUPPLY RESISTORS		
VOLT	RA & RC	RB & RD
48VDC	150 OHMS S#-1267272	180 0 OHMS S#-1201004
125 VDC	900 OHMS S#-1267287	5000 OHMS S#-1205214

AR RELAY	
VOLT	2M-2B CONTACTS
48VDC	S#-671B472G11
125VDC	S#-408C845G26

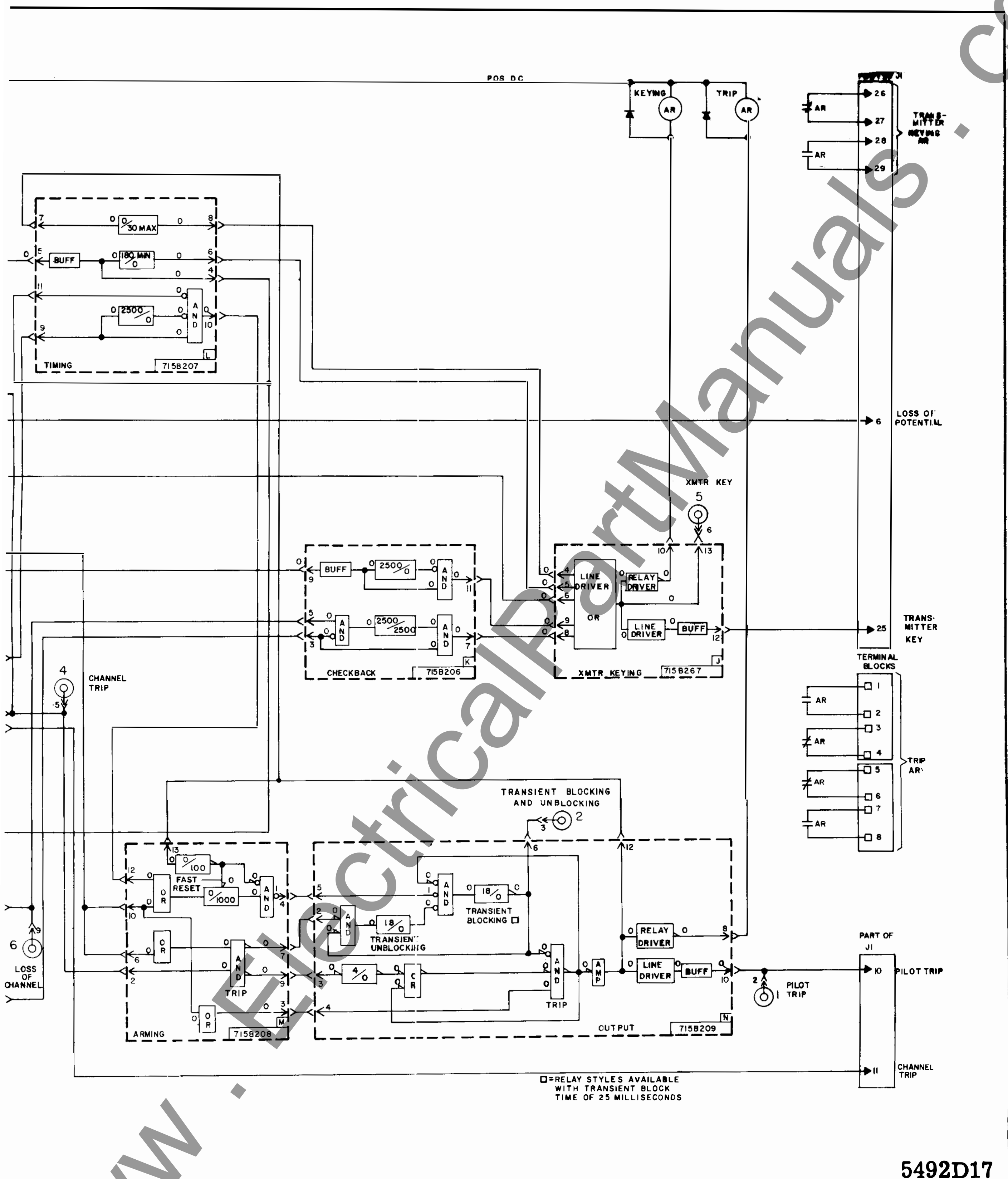
SYMBOL INDICATES POINT ON TEST BOARD (SLOT O)

SYMBOLS "0" AND "1" REPRESENT THE LOGIC VOLTAGE STATES FOR NORMAL OPERATING STATE OF RELAY

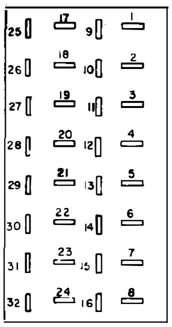
△ FOR TWO TERMINAL LINE APPLICATIONS, CHANNEL TWO INTERFACE BOARD (SLOT G) MUST NOT BE USED IN THE RELAY

△ FOR THREE TERMINAL LINE APPLICATIONS, BOTH CHANNEL ONE AND TWO INTERFACE BOARDS (SLOTS F AND G) MUST BE USED IN RELAY

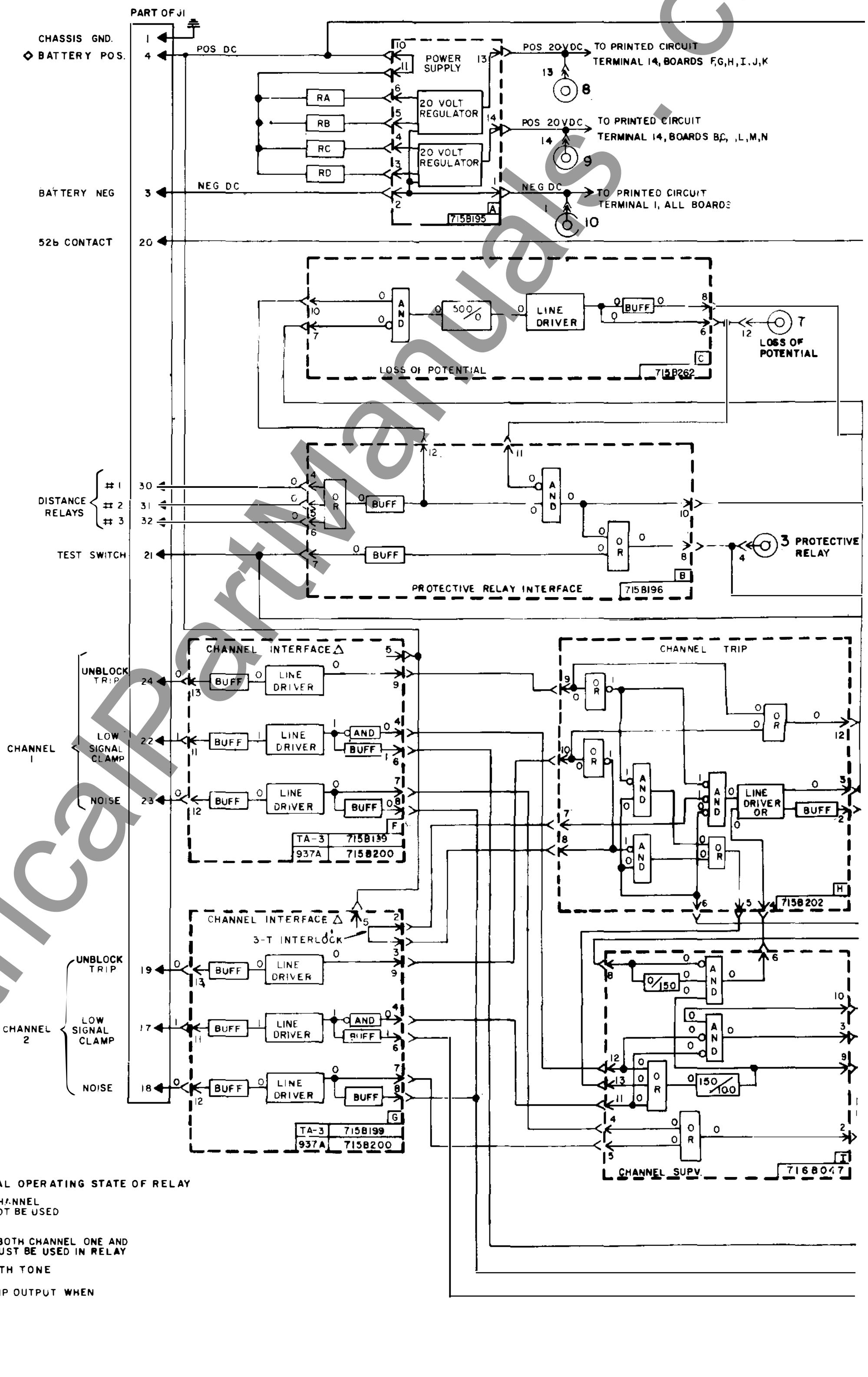
Fig. 5 **STU logic - for use w carrier channel.**



ith solid state distance relays and a TCF



CONNECTOR J1
AS VIEWED FROM
REAR OF RELAY.



· POWER SUPPLY RESISTORS		
VOLT	RA & RC	RB & RD
48VDC	150 OHMS S[#]-1267272	1800 OHMS S[#]-1201004
125VDC	900 OHMS S[#]-1267287	5000 OHMS S[#]-1205214

AR RELAY	
VOLT	2M-2B CONTACTS
48VDC	S[#]671B472G11
125VDC	S[#]408C845G26

SYMBOL INDICATES POINT ON TEST BOARD (SLOT O)

SYMBOLS "0" AND "1" REPRESENT THE LOGIC VOLTAGE STATES FOR NORMAL OPERATING STATE OF RELAY

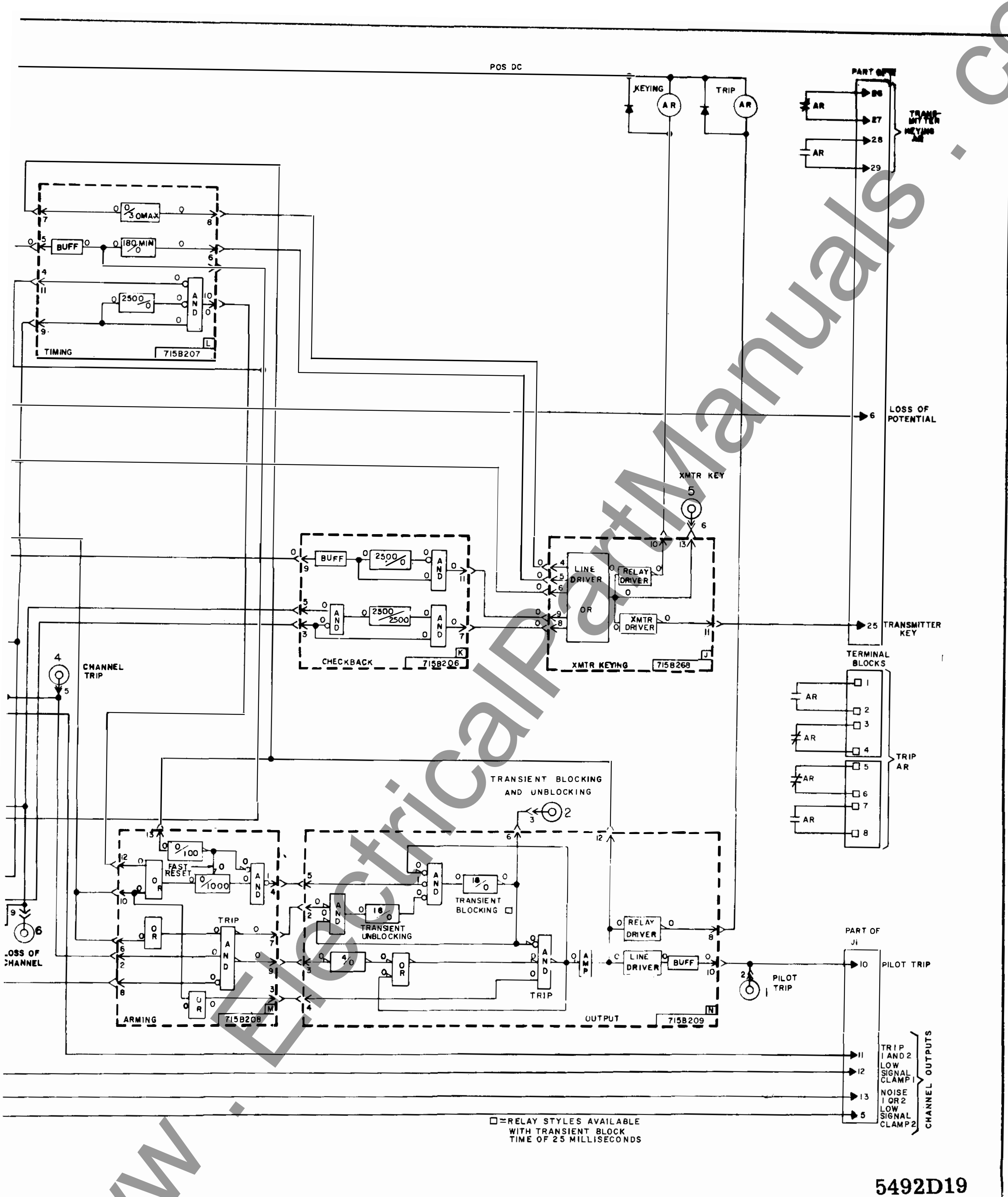
△ FOR TWO TERMINAL LINE APPLICATIONS, CHANNEL TWO INTERFACE BOARD (SLOT G) MUST NOT BE USED IN THE RELAY

△ FOR THREE TERMINAL LINE APPLICATIONS, BOTH CHANNEL ONE AND TWO INTERFACE BOARDS (SLOTS F AND G) MUST BE USED IN RELAY

FOR THE STU-UNBLOCK SYSTEM USED WITH TONE CHANNELS, THE TONE RECEIVERS MUST BE INTERNALLY STRAPPED TO CLAMP TO A TRIP OUTPUT WHEN A LOW SIGNAL CONDITION OCCURS

◇ FOR 937A TONES, ONLY 48VDC IS USED

Fig. 7 STU logic - for use with solic



state distance relays and a tone channel.

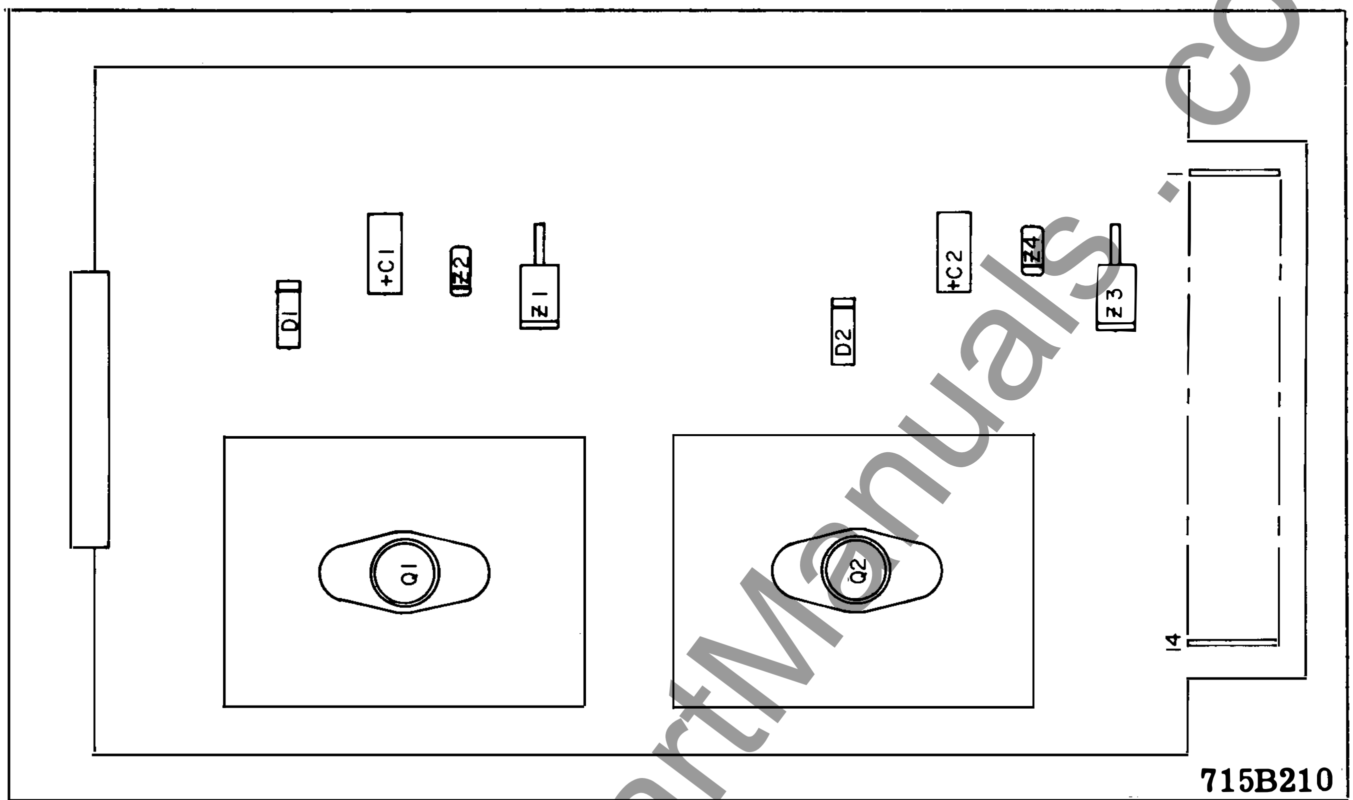


Fig. 8 Component location power supply board.

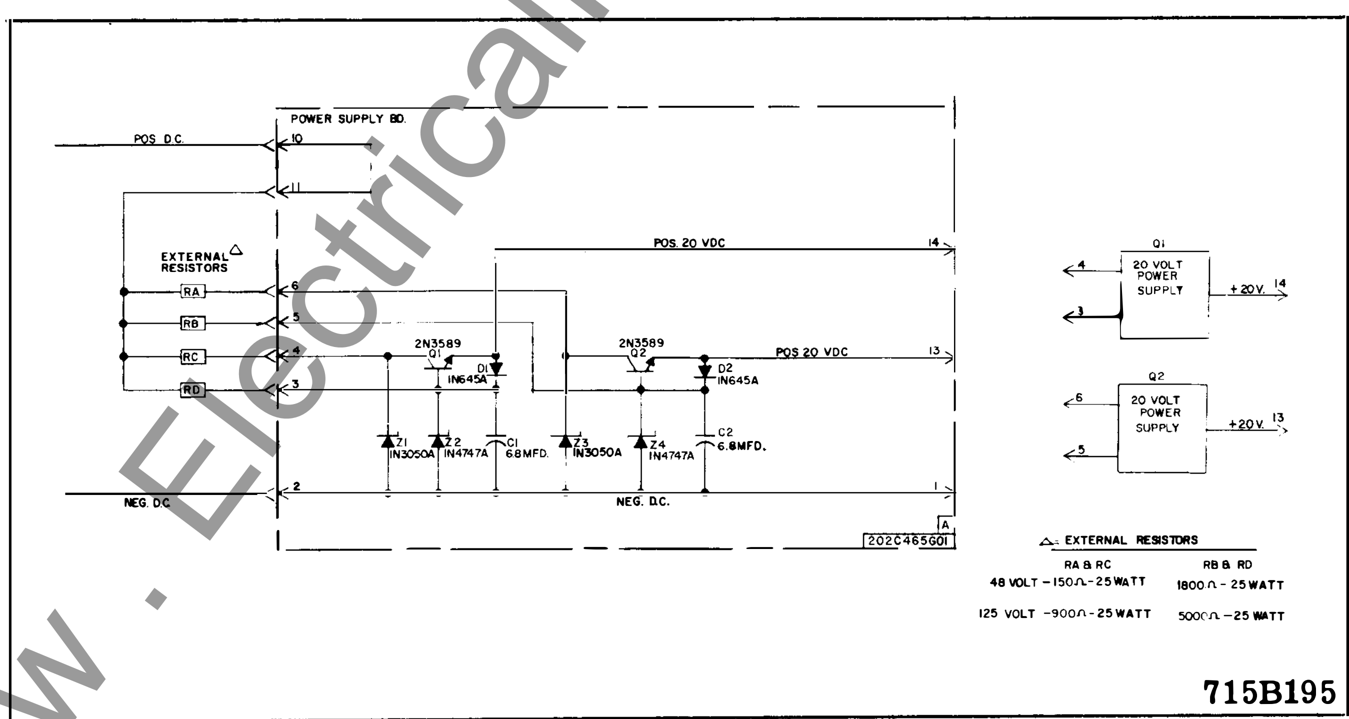


Fig. 9 Internal schematic power supply board

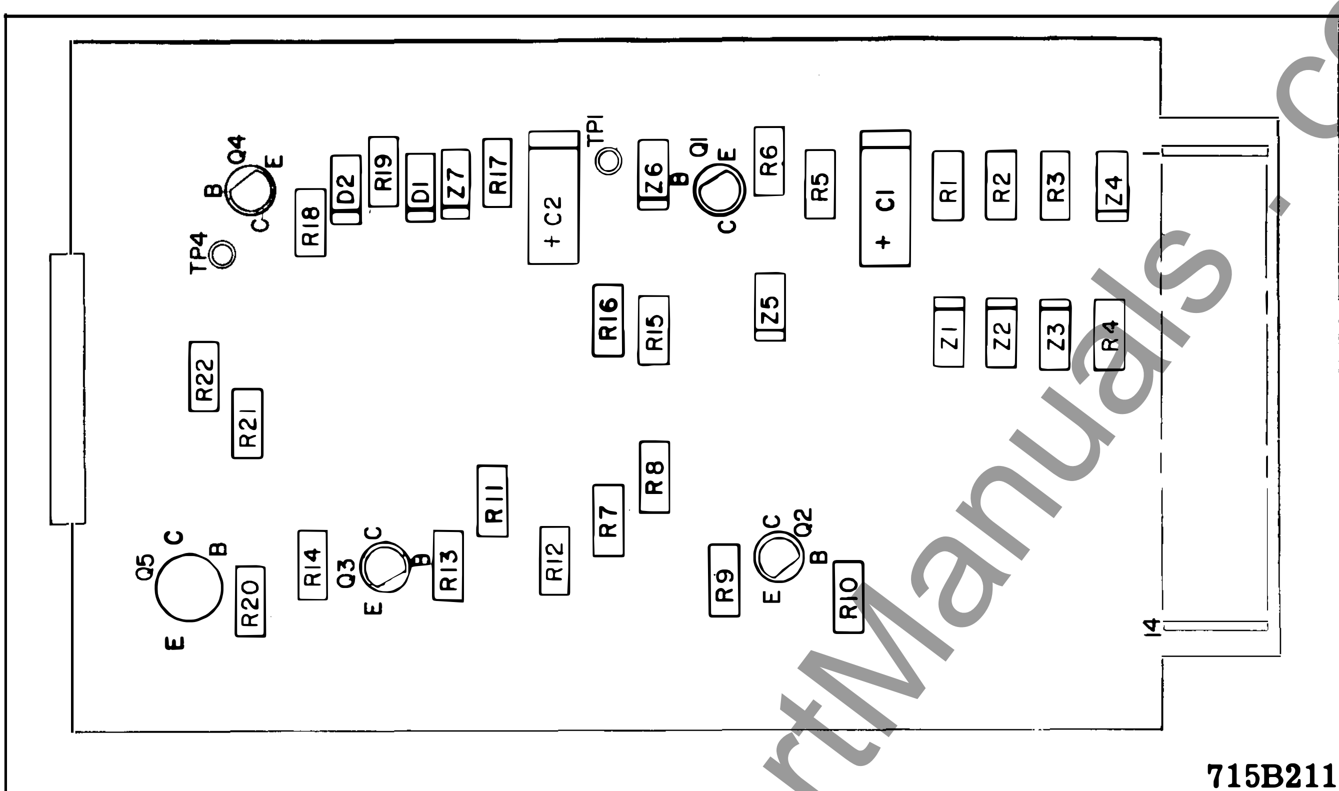


Fig. 10 Component location Protective Relay Interface Board.

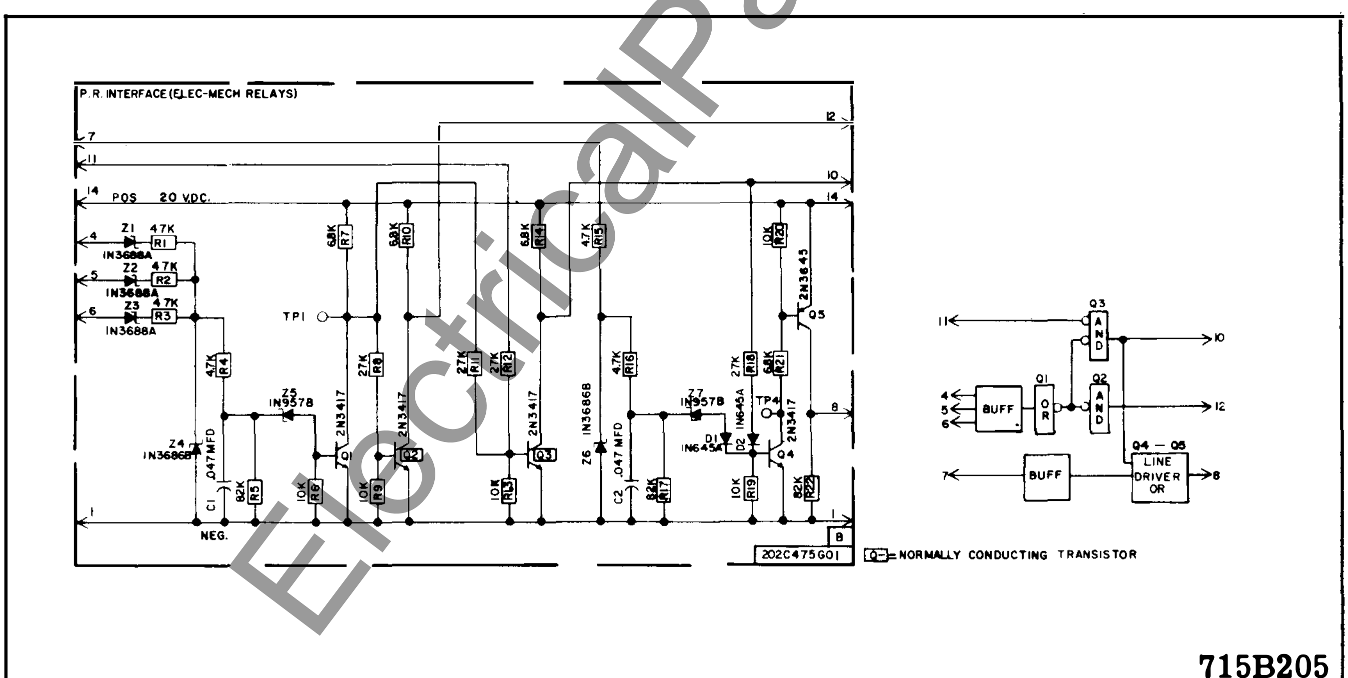


Fig. 11 Internal Schematic Protective Relay Interface Board for Elec-Mech System.

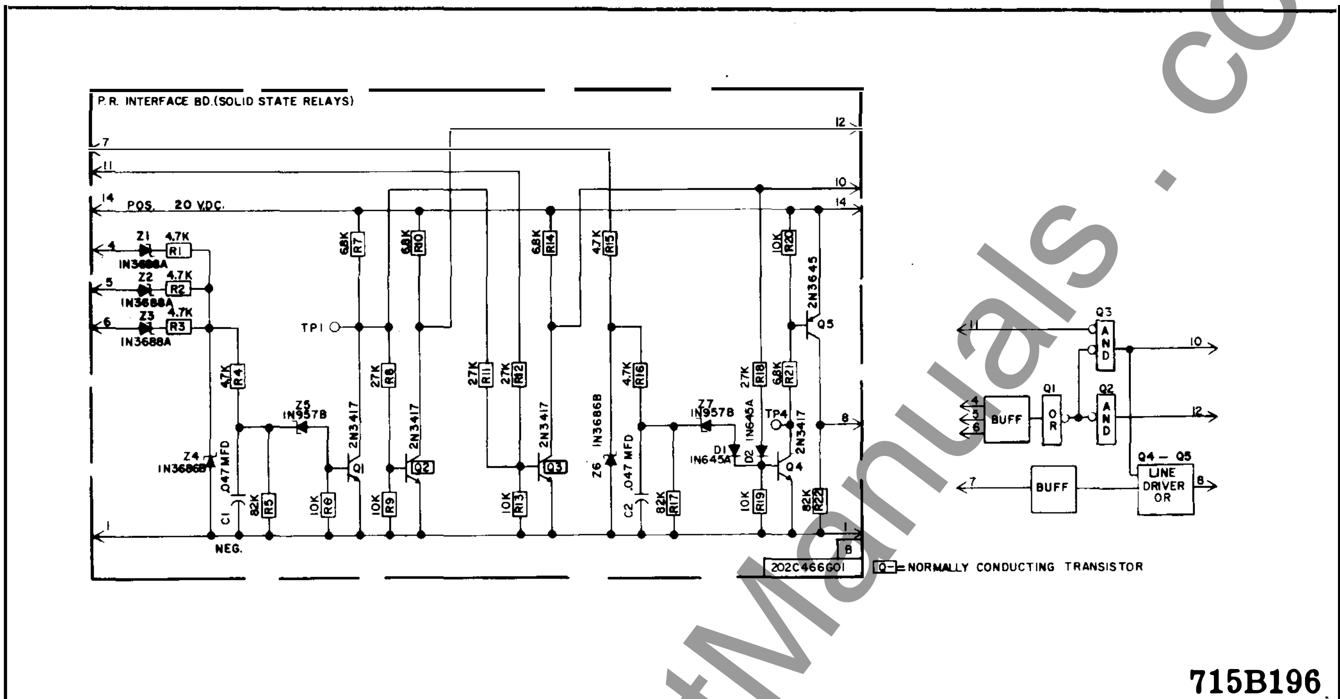


Fig. 12 Internal Schematic Protective Relay Interface Board for solid state System.

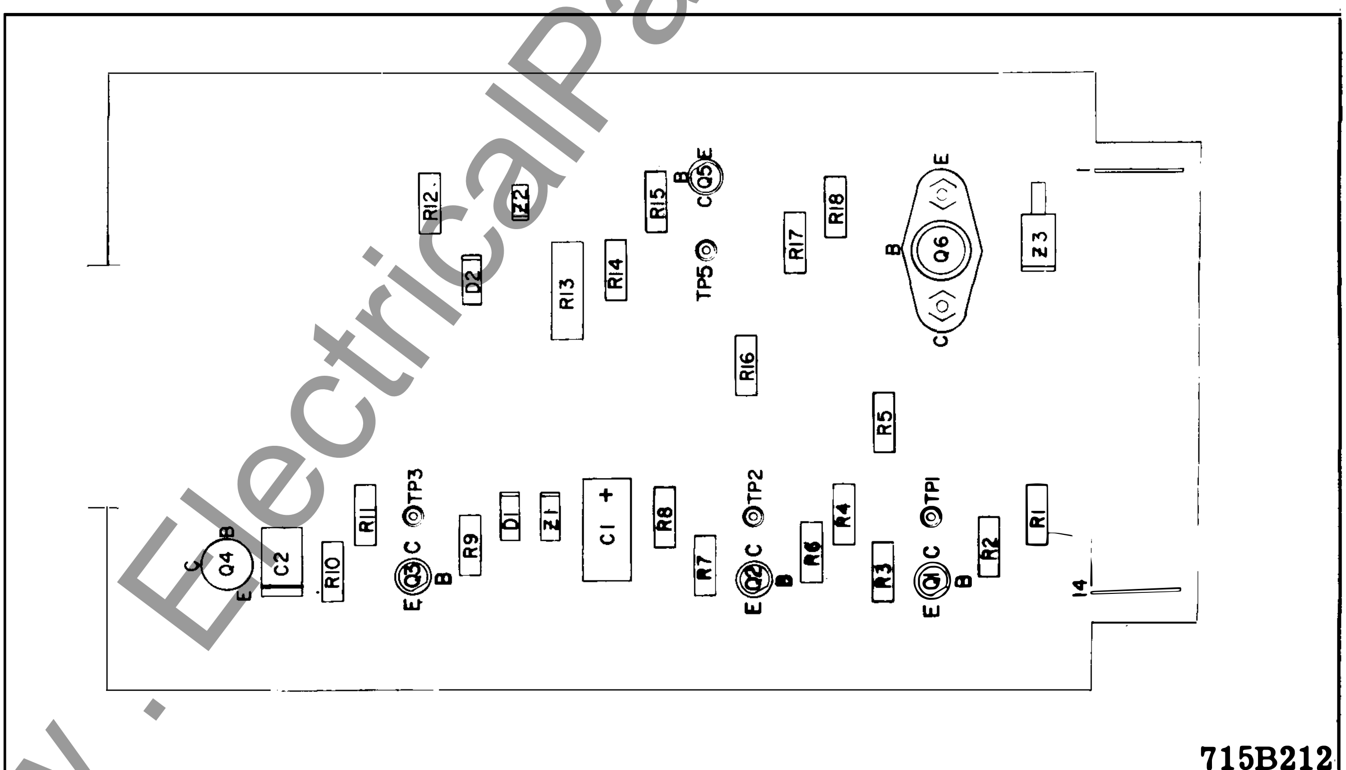


Fig. 13 Component Location Loss of Potential Board.

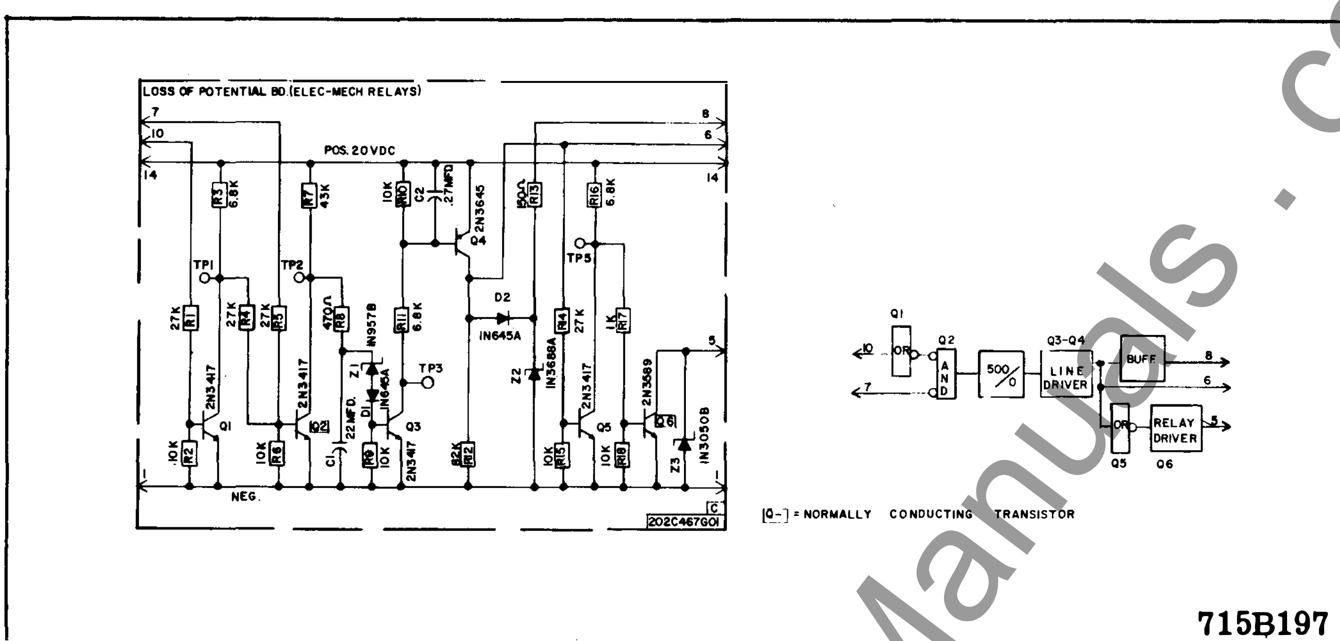


Fig. 14 Internal Schematic Loss of Potential Board for Elec-Mech Systems.

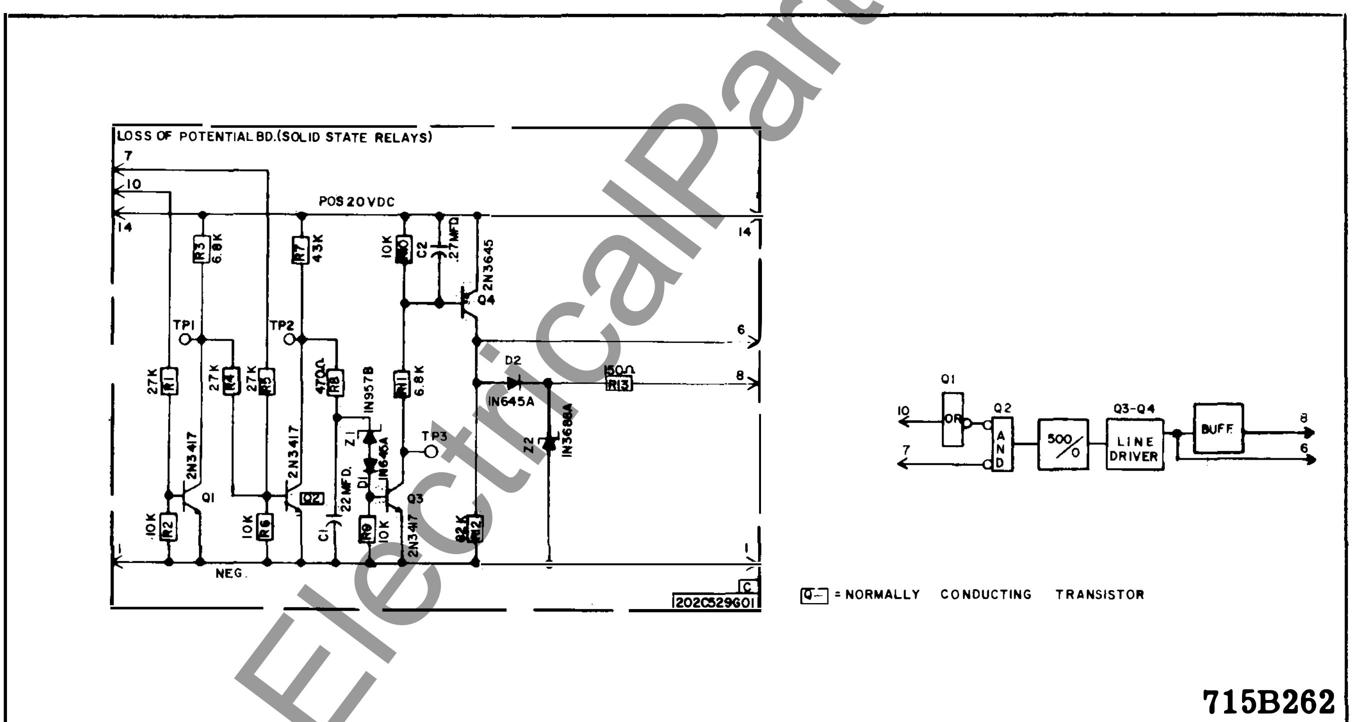
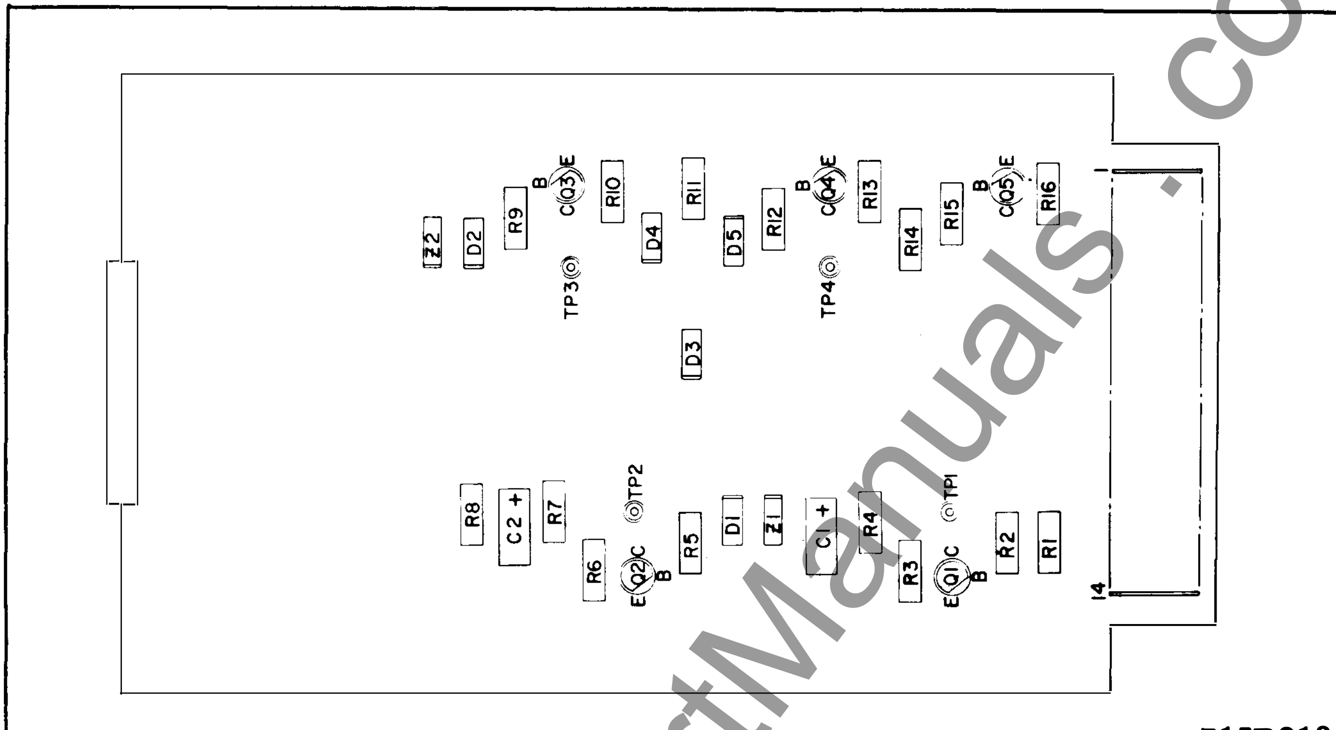
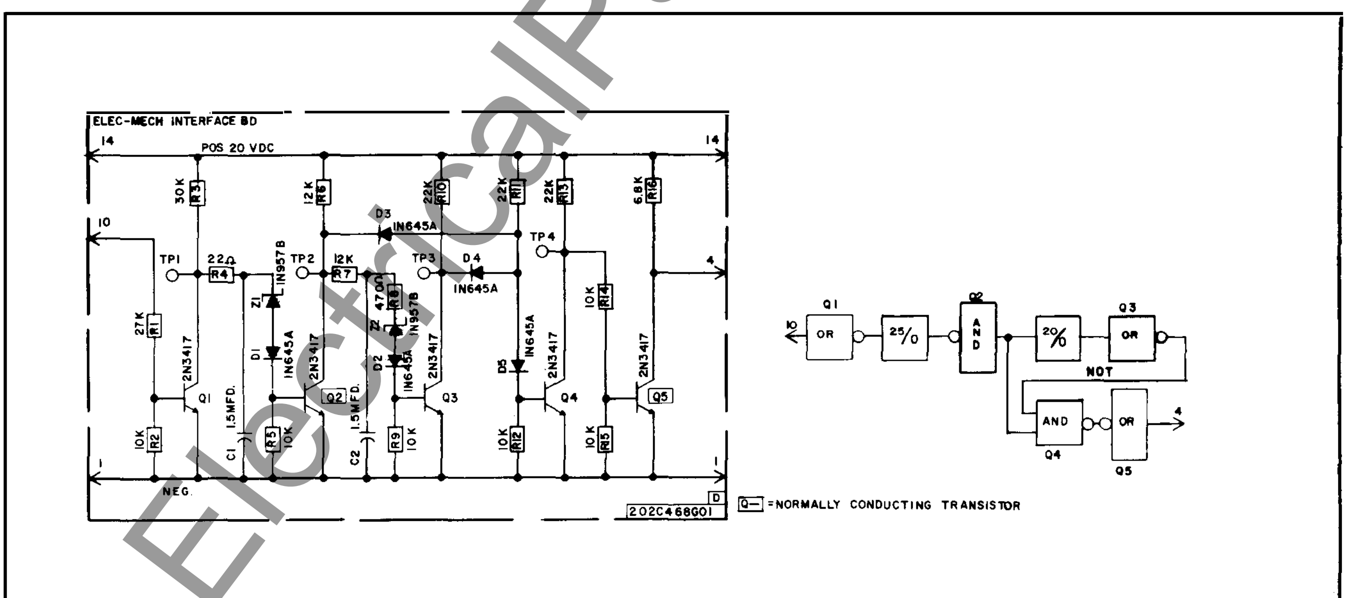


Fig. 15 Internal Schematic Loss of Potential Board for solid state system.



715B213

Fig. 16 Component Location Elec-Mech Interface Board.



715B198

Fig. 17 Internal Schematic Elec-Mech Interface Board.

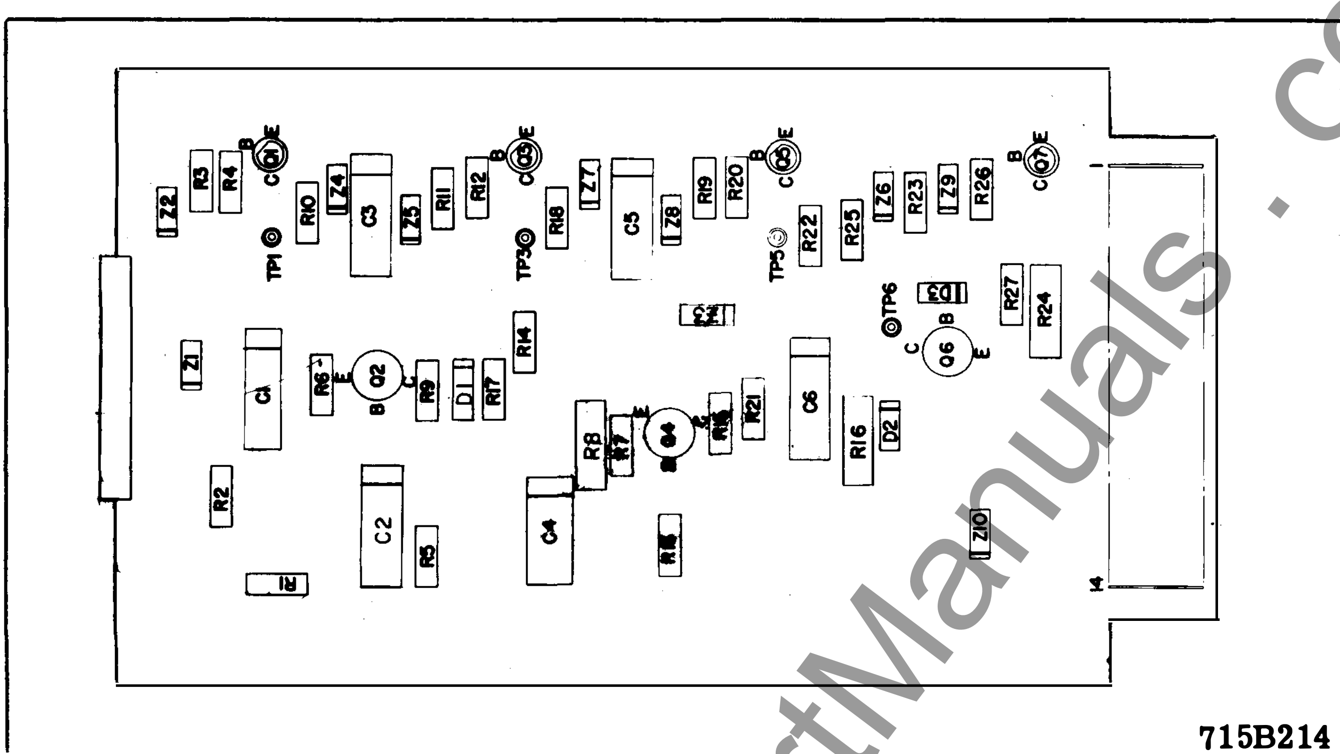


Fig. 18 Component Location Channel Interface Board

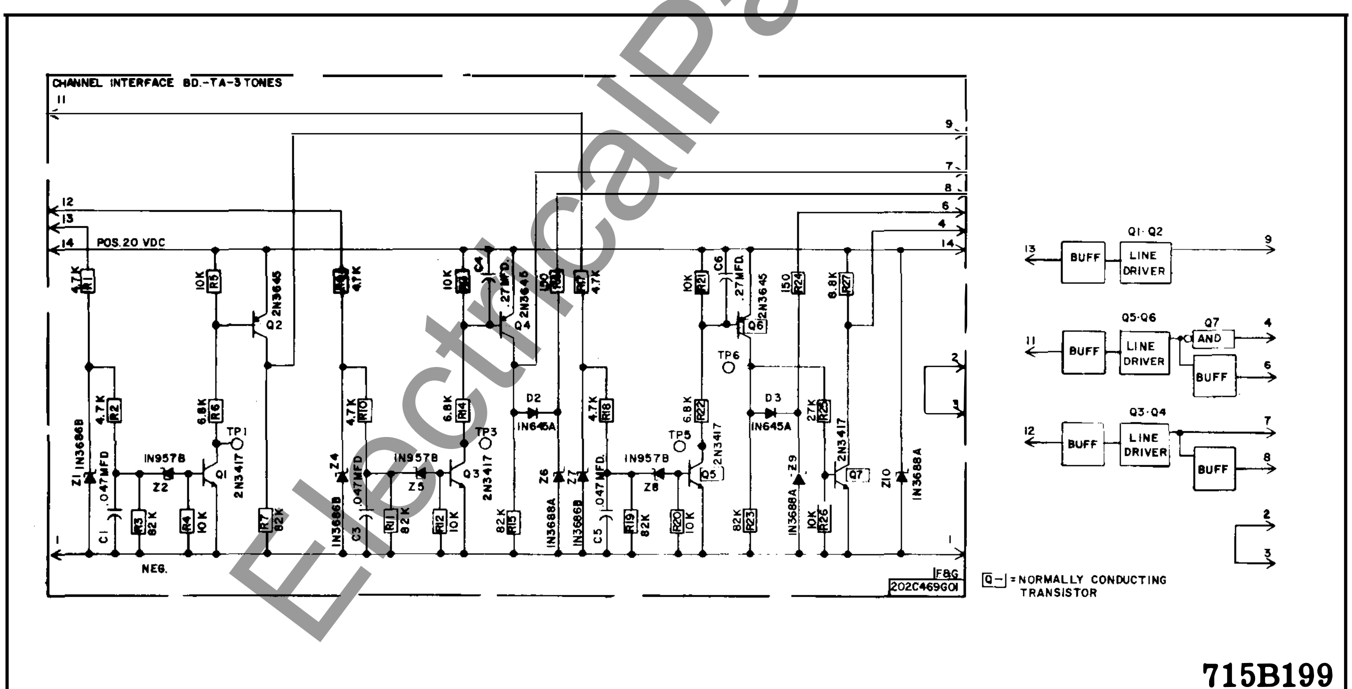


Fig. 19 Internal Schematic Channel Interface Board for TA-3 Tone.

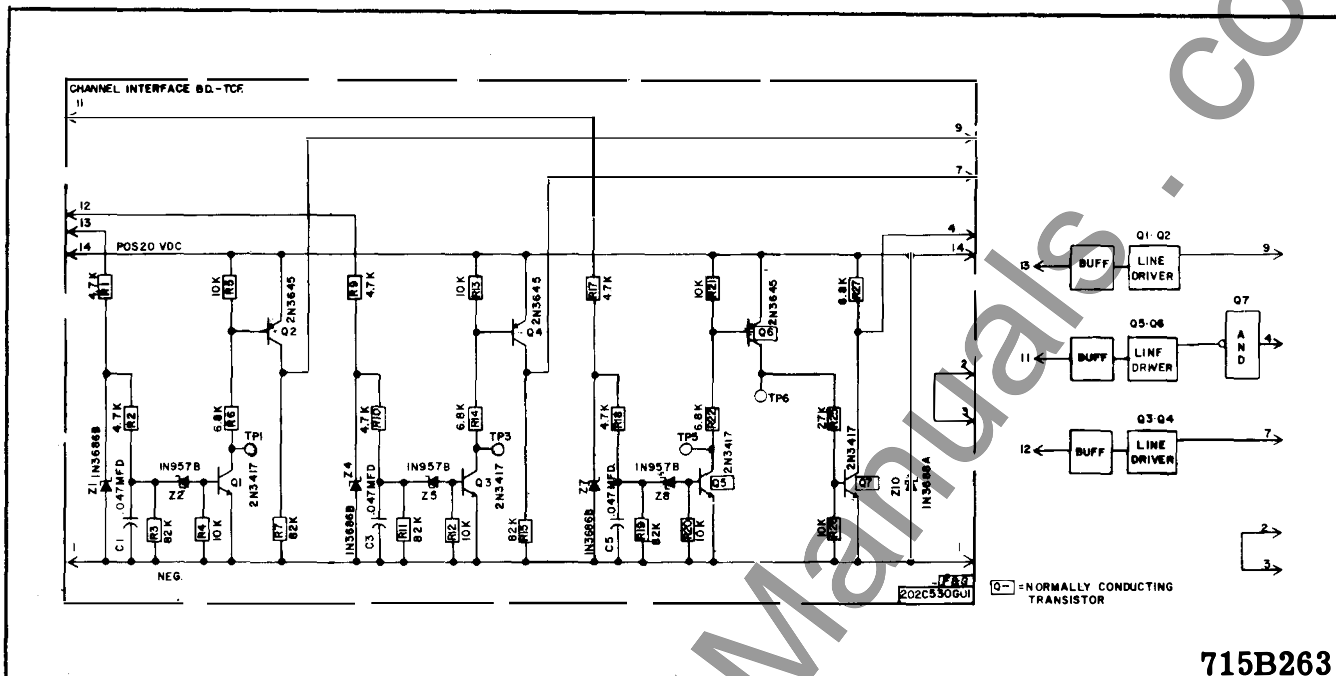


Fig. 20 Internal Schematic Channel Interface Board for TCF Carrier.

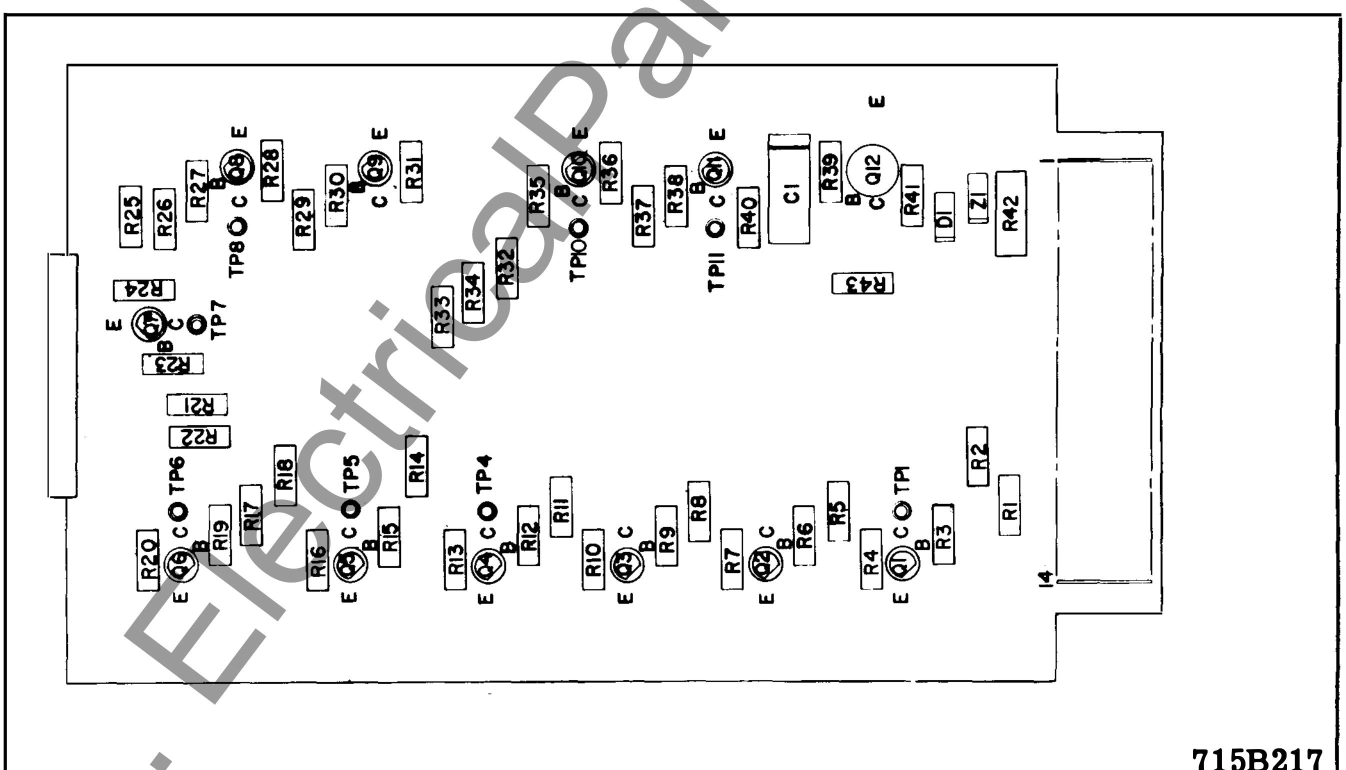


Fig. 21 Component Location Channel Trip Board.

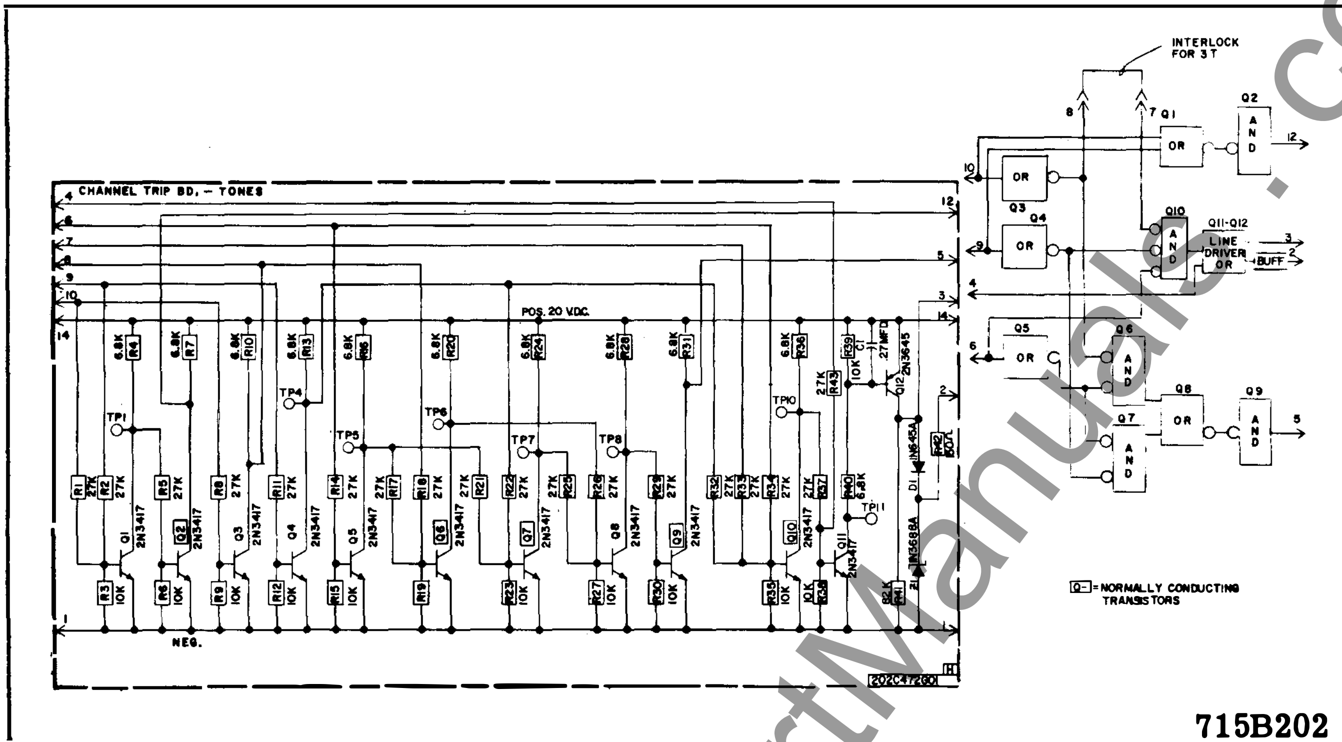


Fig. 22 Internal Schematic Channel Trip Board for Tones.

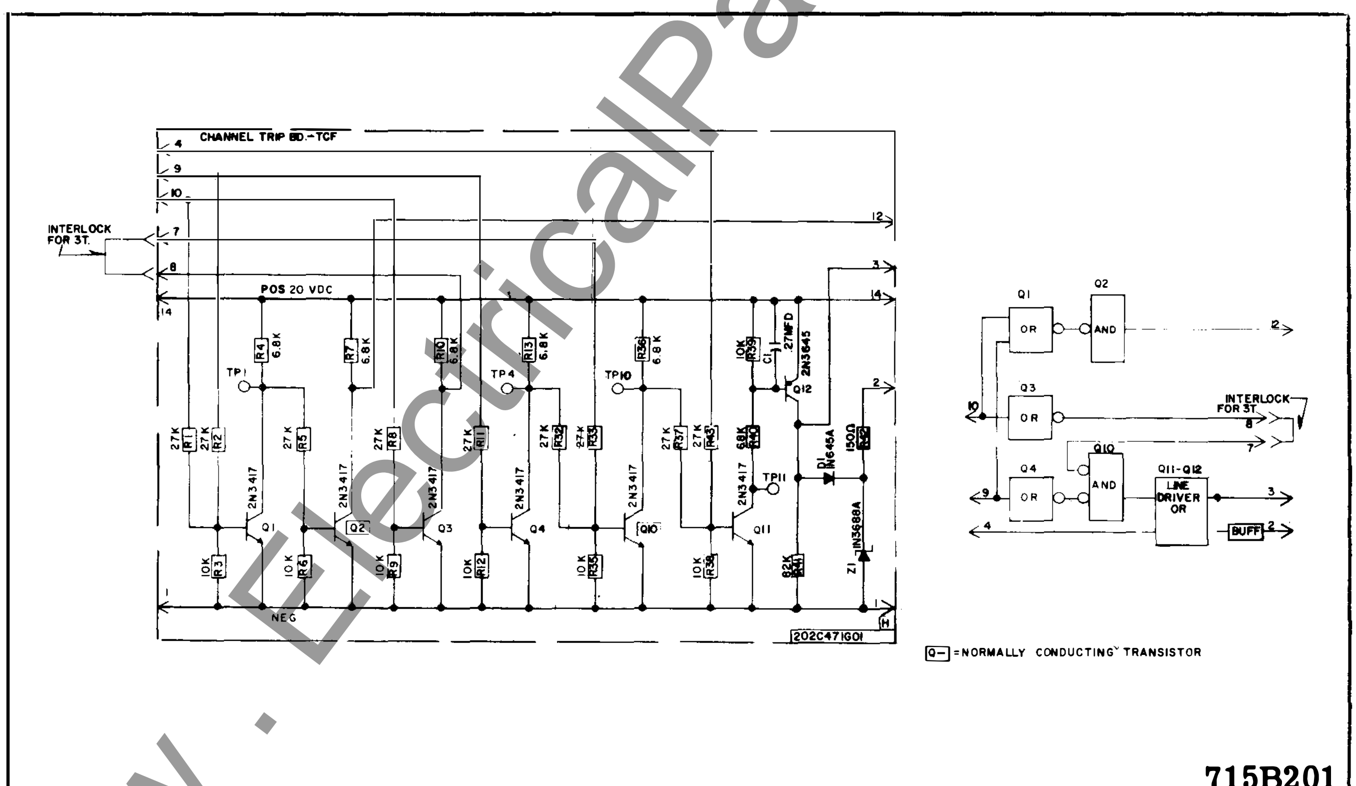
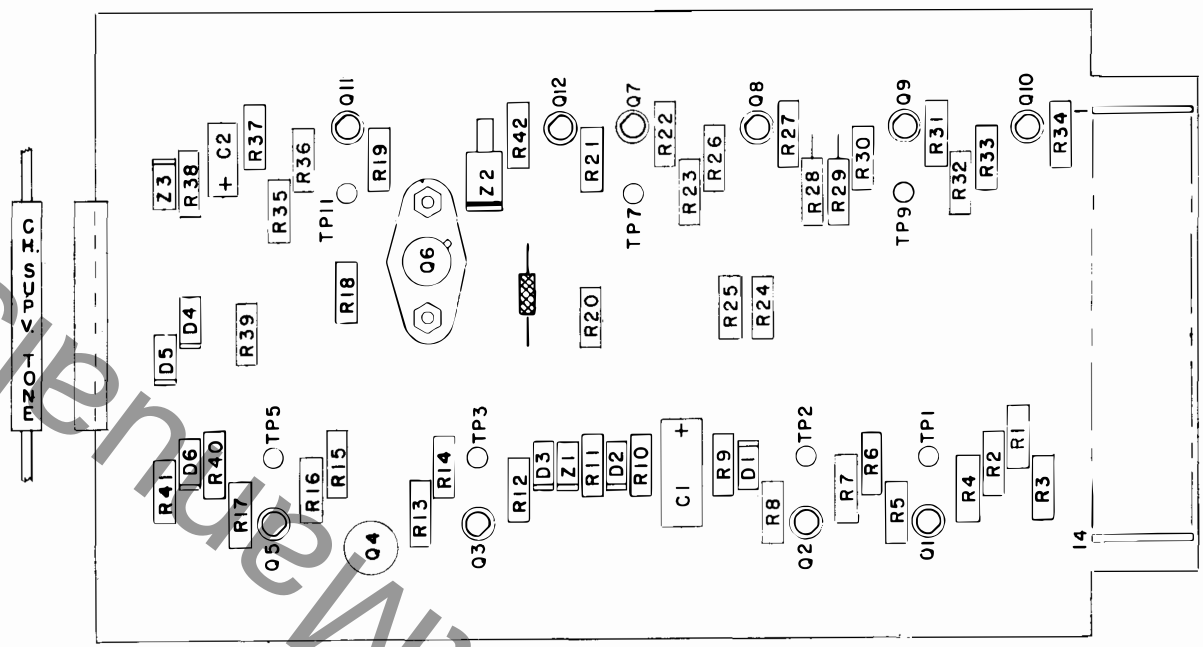
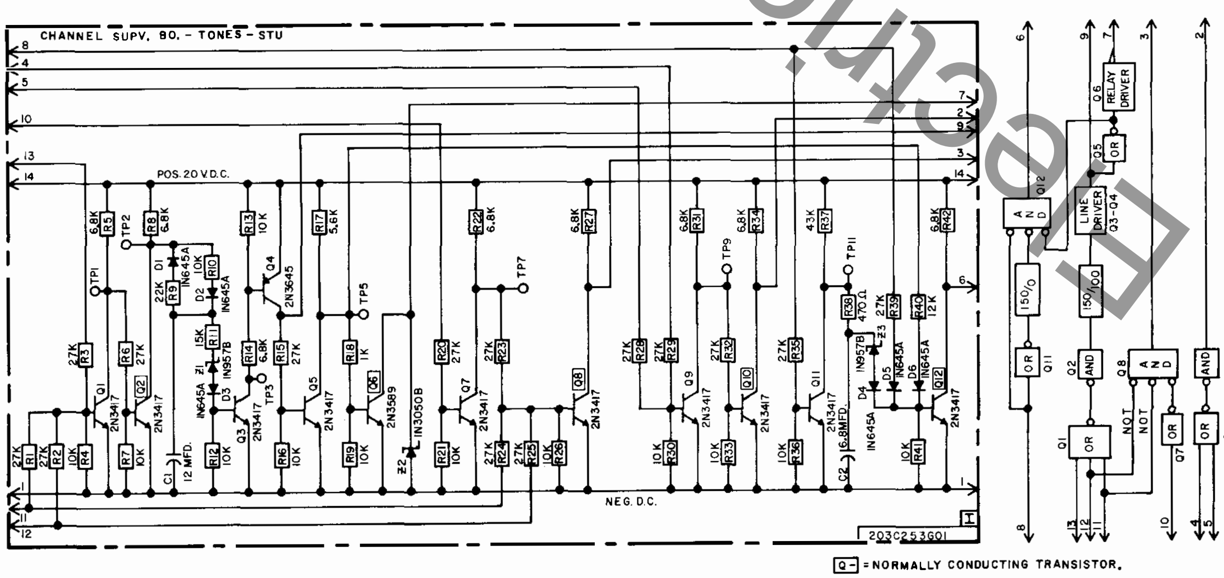


Fig. 23 Internal Schematic Channel Trip Board for TCF.



716B048

Fig. 24 Component Location Channel Supervision Board tone Channel.



716B047

Fig. 25 Internal Schematic Channel Supv. Board for Tone Channel.

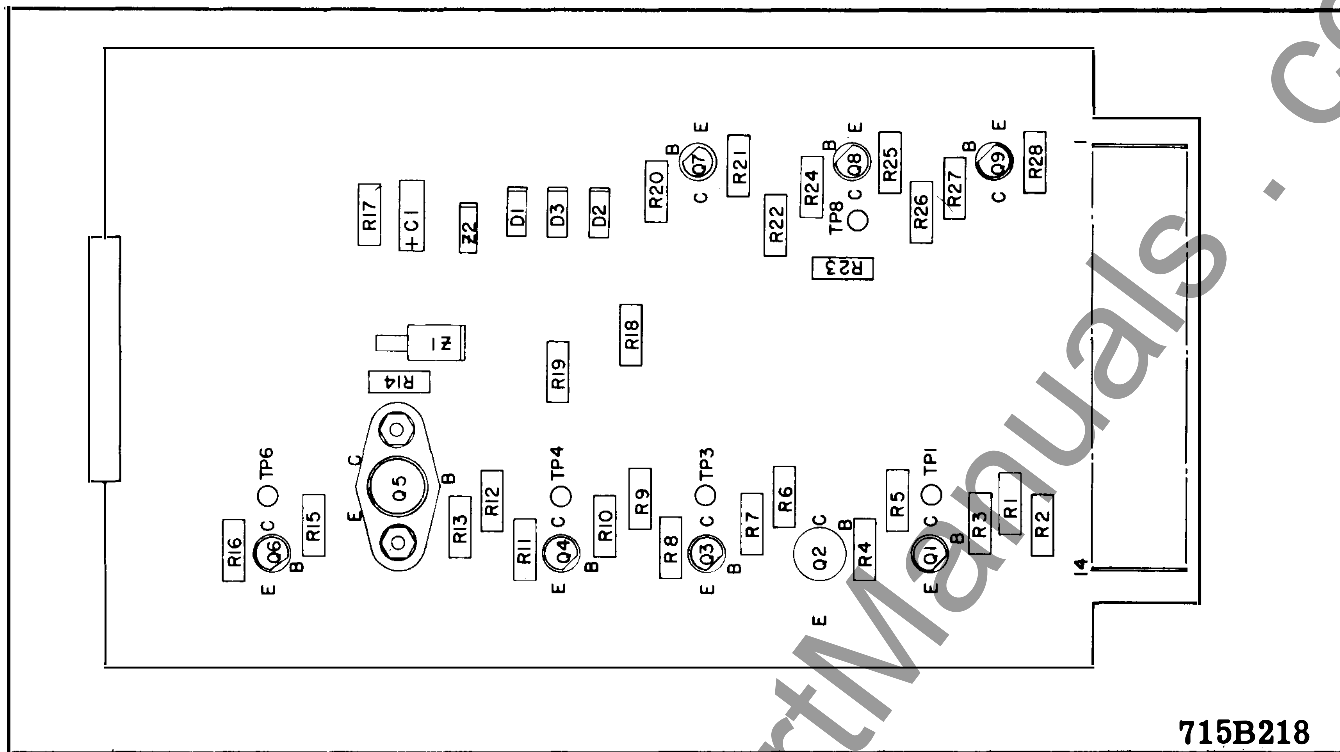


Fig. 26 Component Location Channel Supervision Board - TCF Channel.

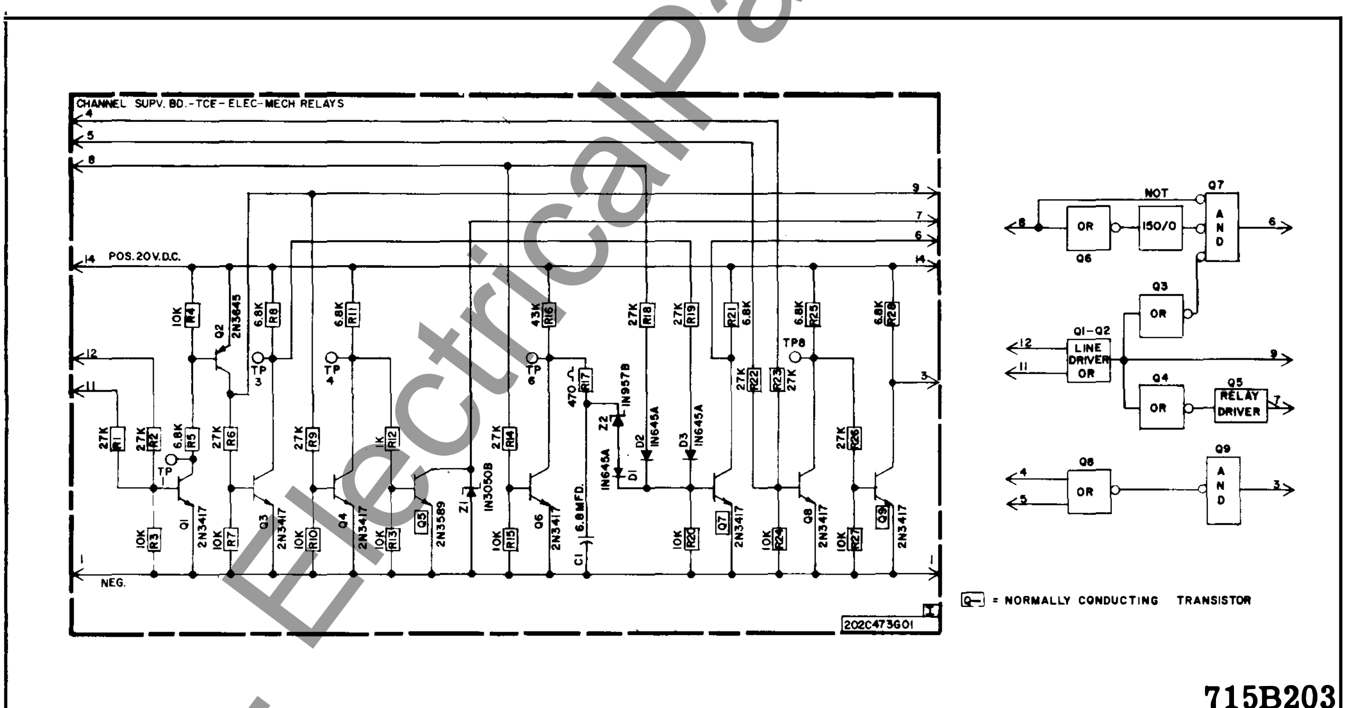


Fig. 27 Internal Schematic Channel Supervision Board for TCF Channel and Elec-Mech System.

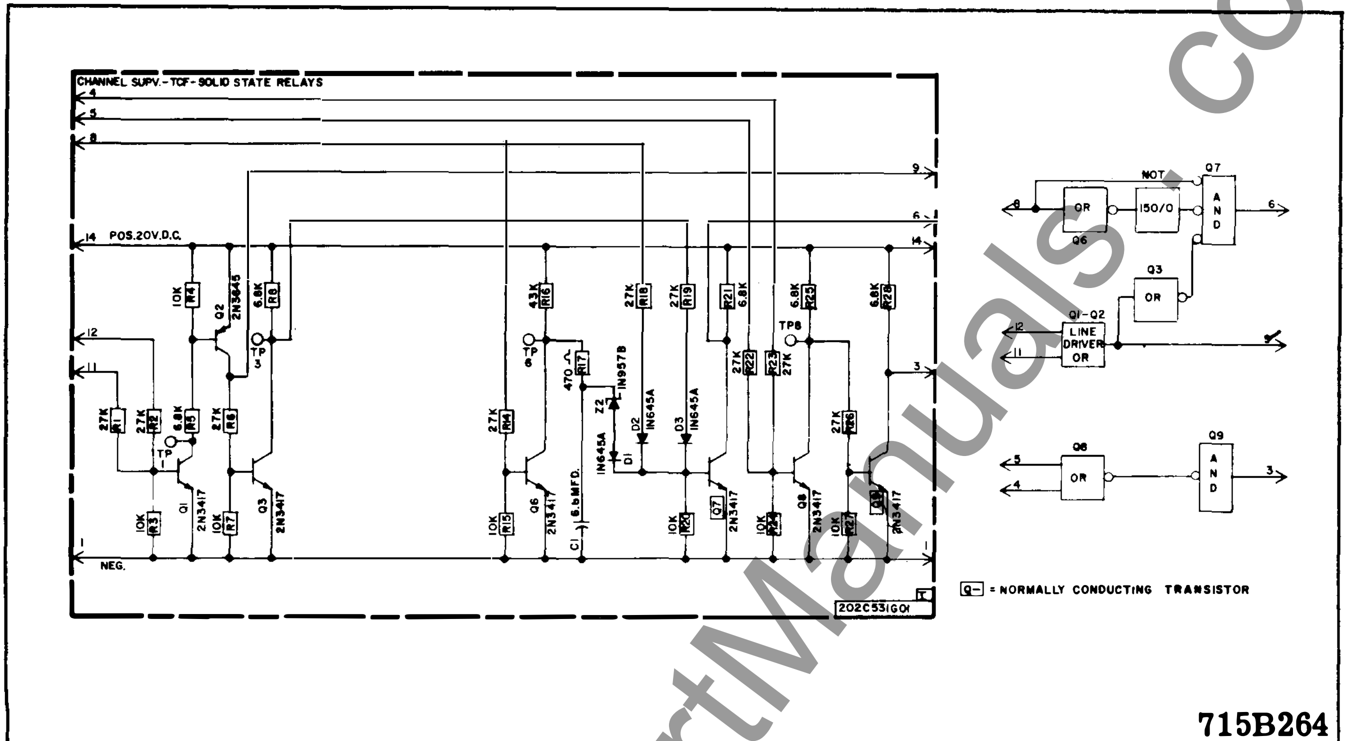


Fig. 28 Internal Schematic Channel Supervision Board for TCF Channel and Solid State System.

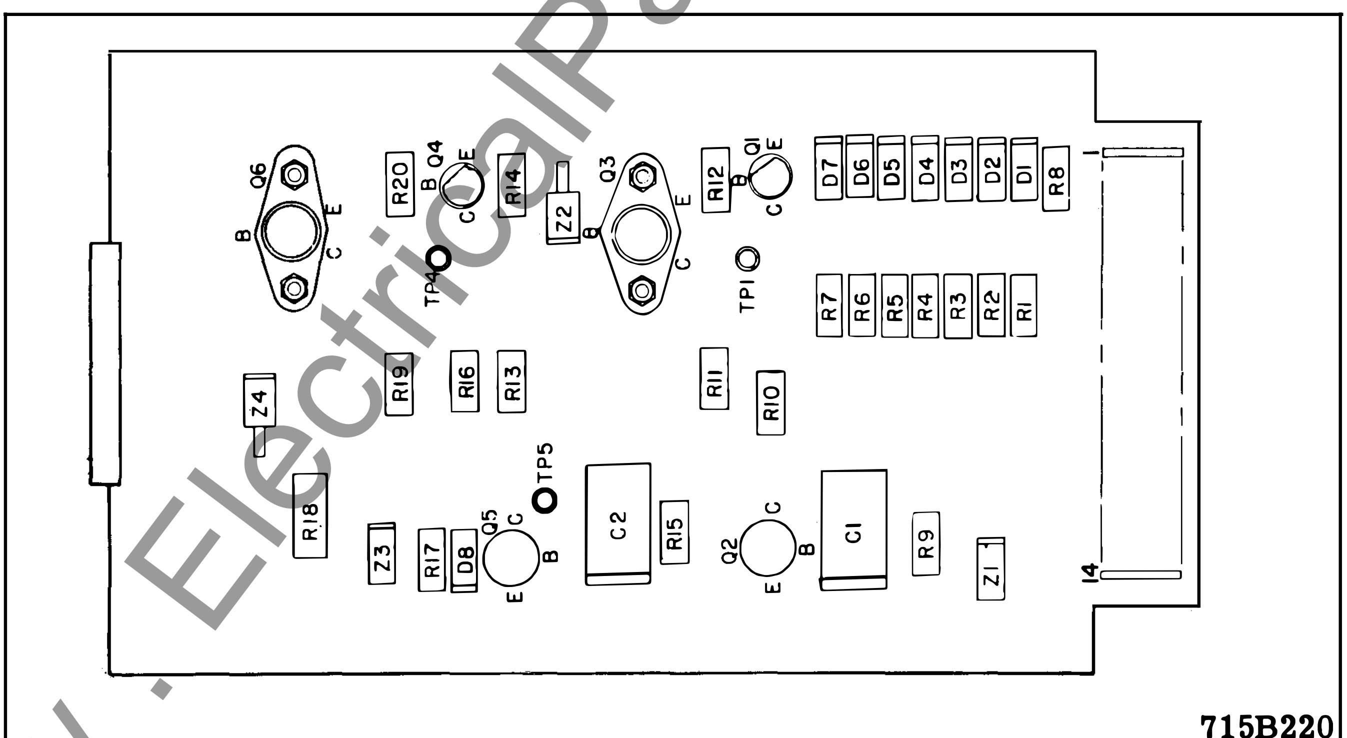


Fig. 29 Component Location Transmitter Key Board.

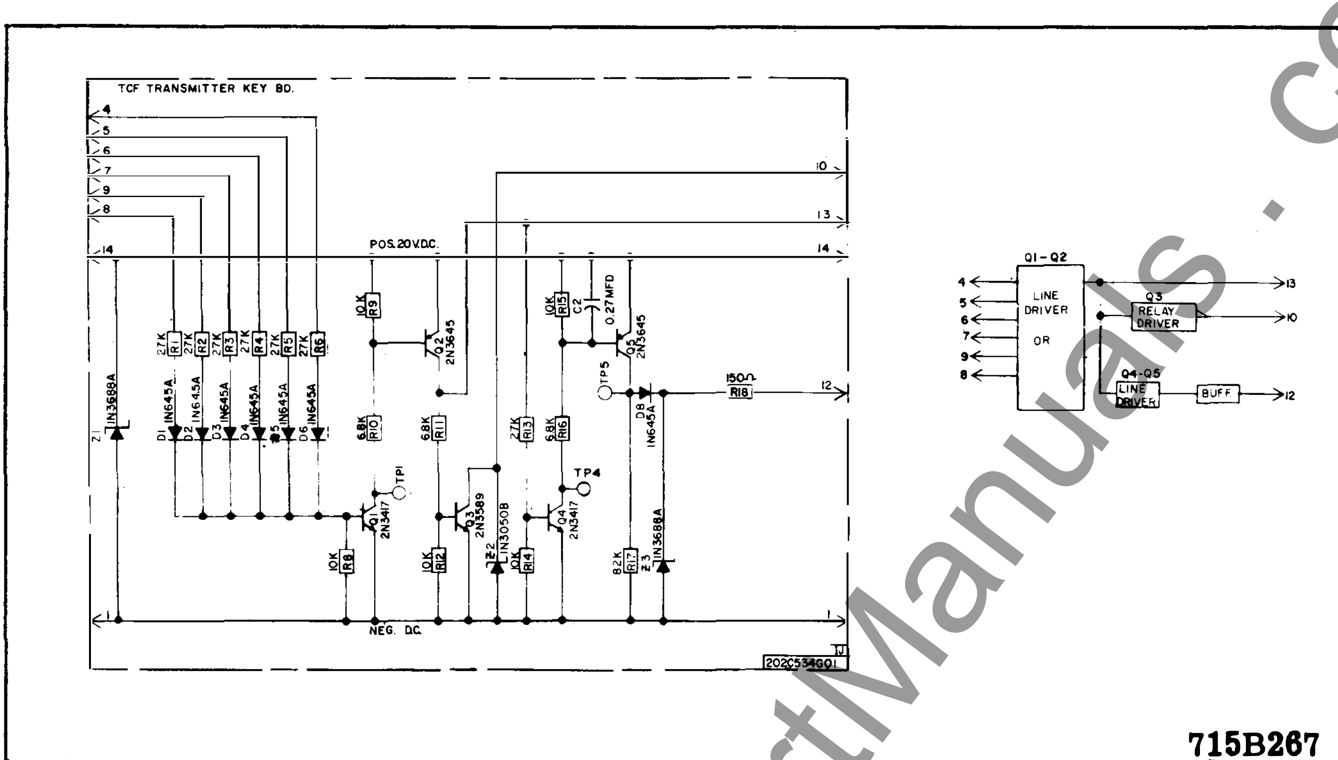


Fig. 30 Internal Schematic Transmitter Key Board for TCF Channel.

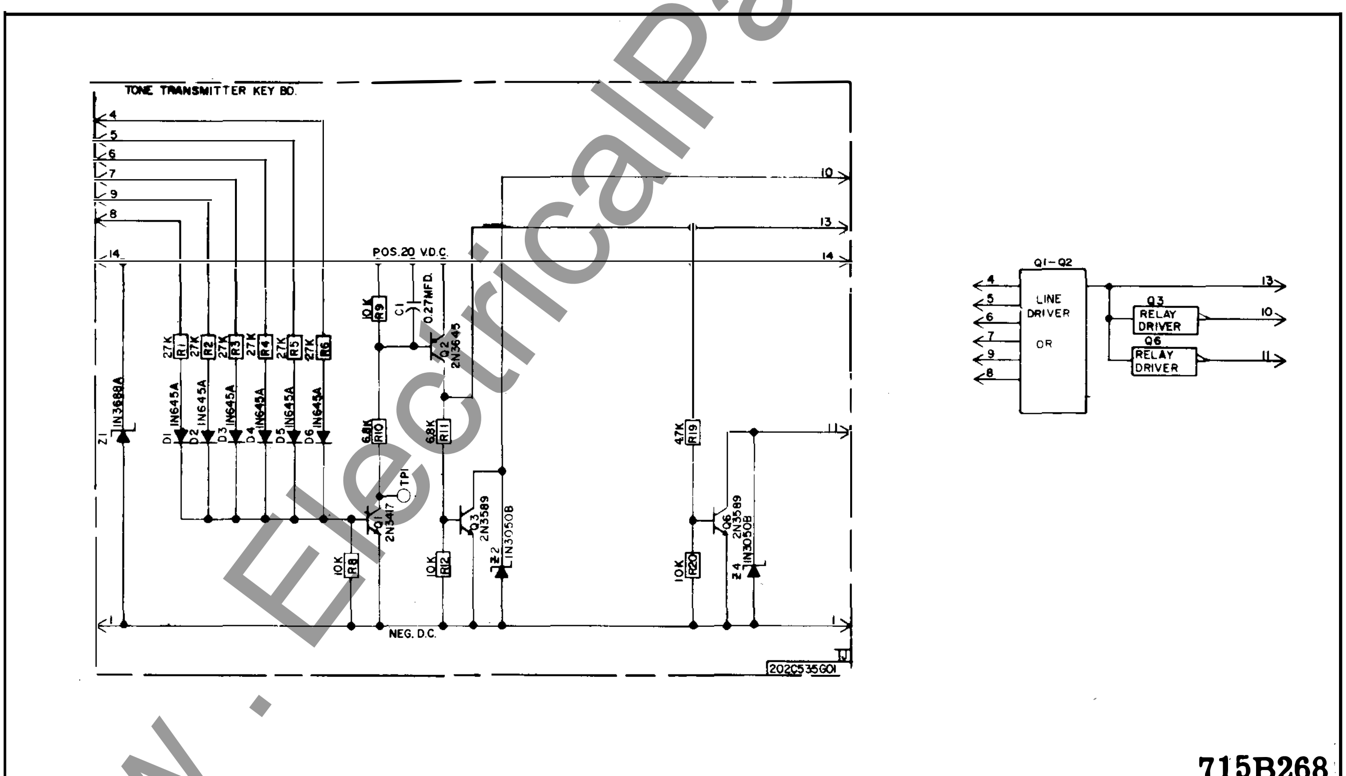


Fig. 31 Internal Schematic Transmitter Key Board for Tone Channel.

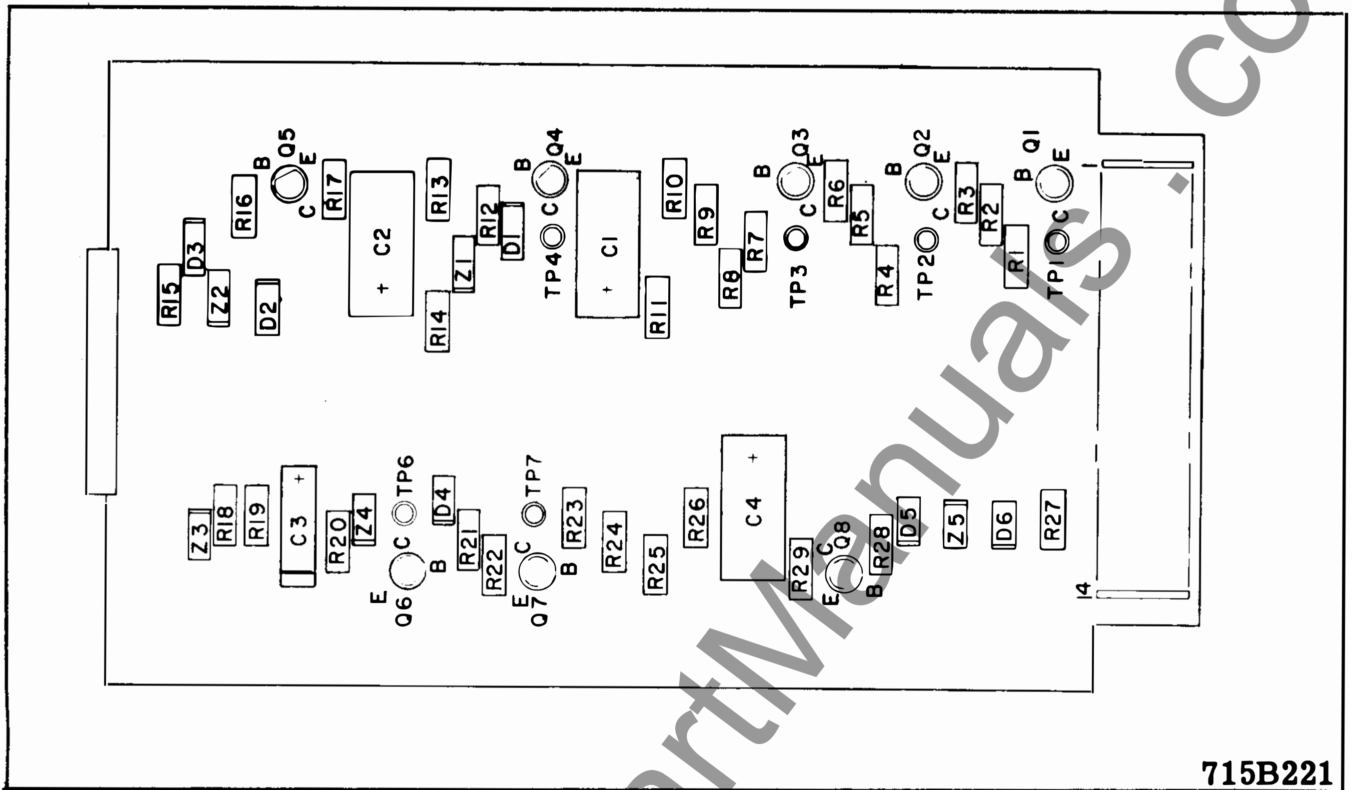


Fig. 32 Component Location Checkback Board.

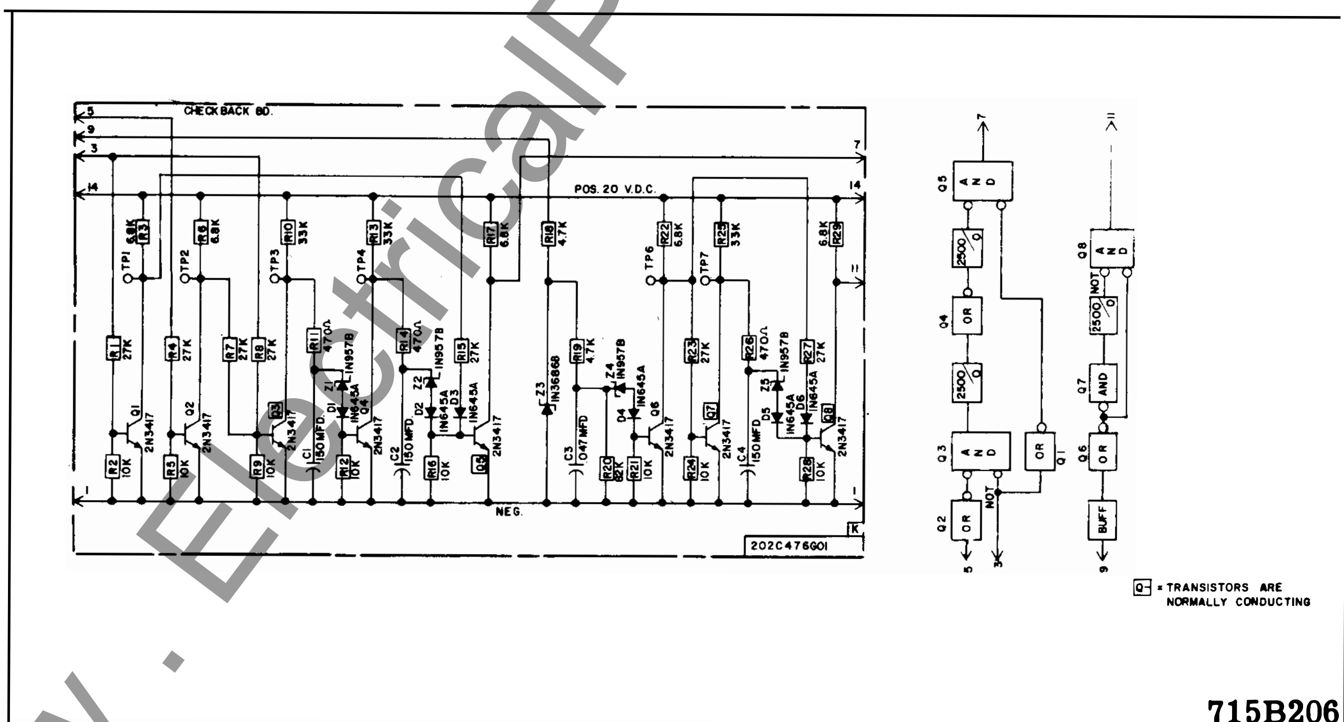


Fig. 33 Internal Schematic Checkback Board.

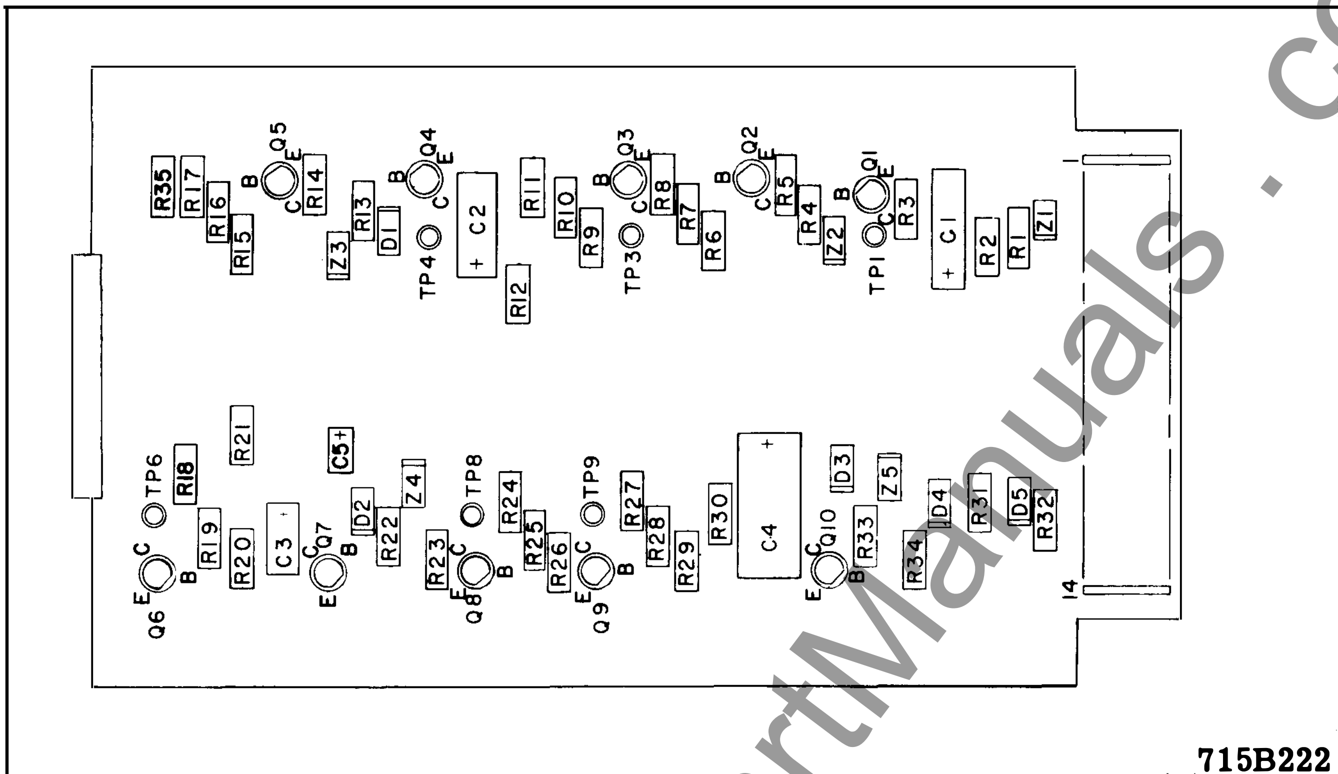


Fig. 34 Component Location Timing Board.

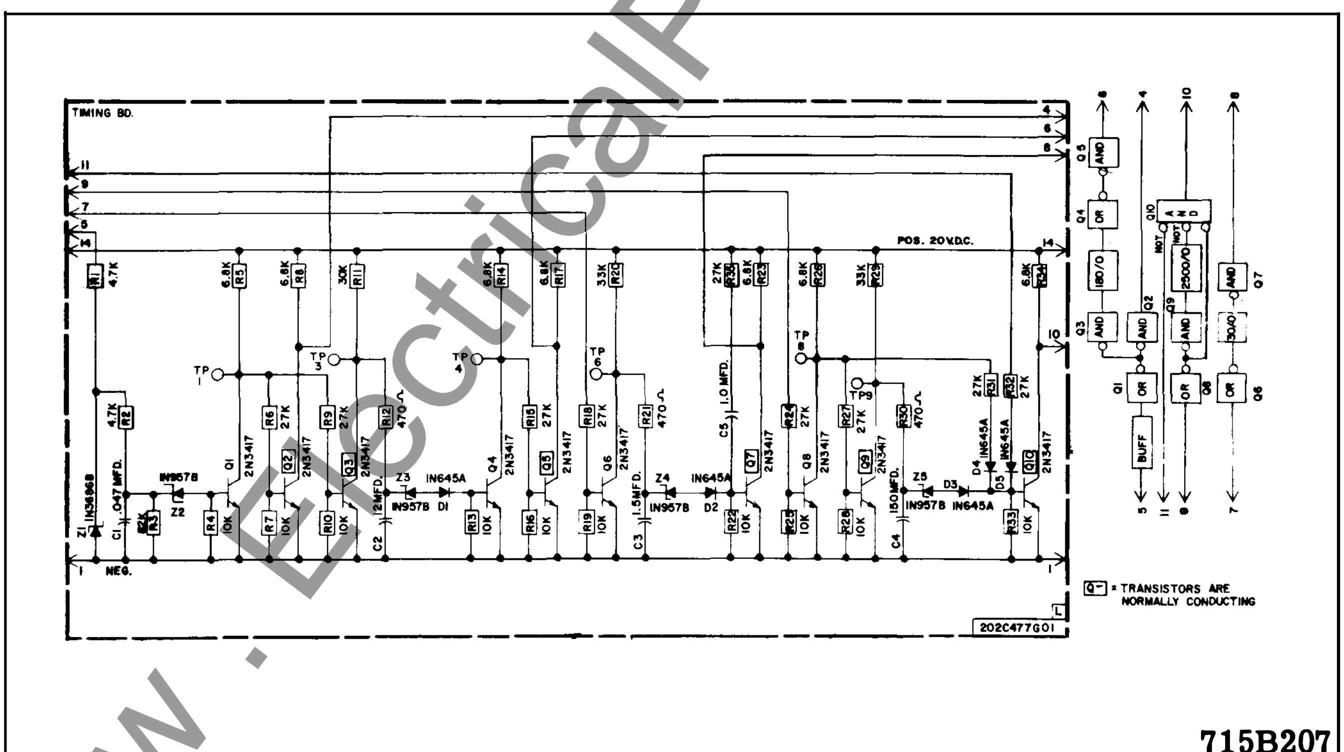


Fig. 35 Internal Schematic Timing Board.

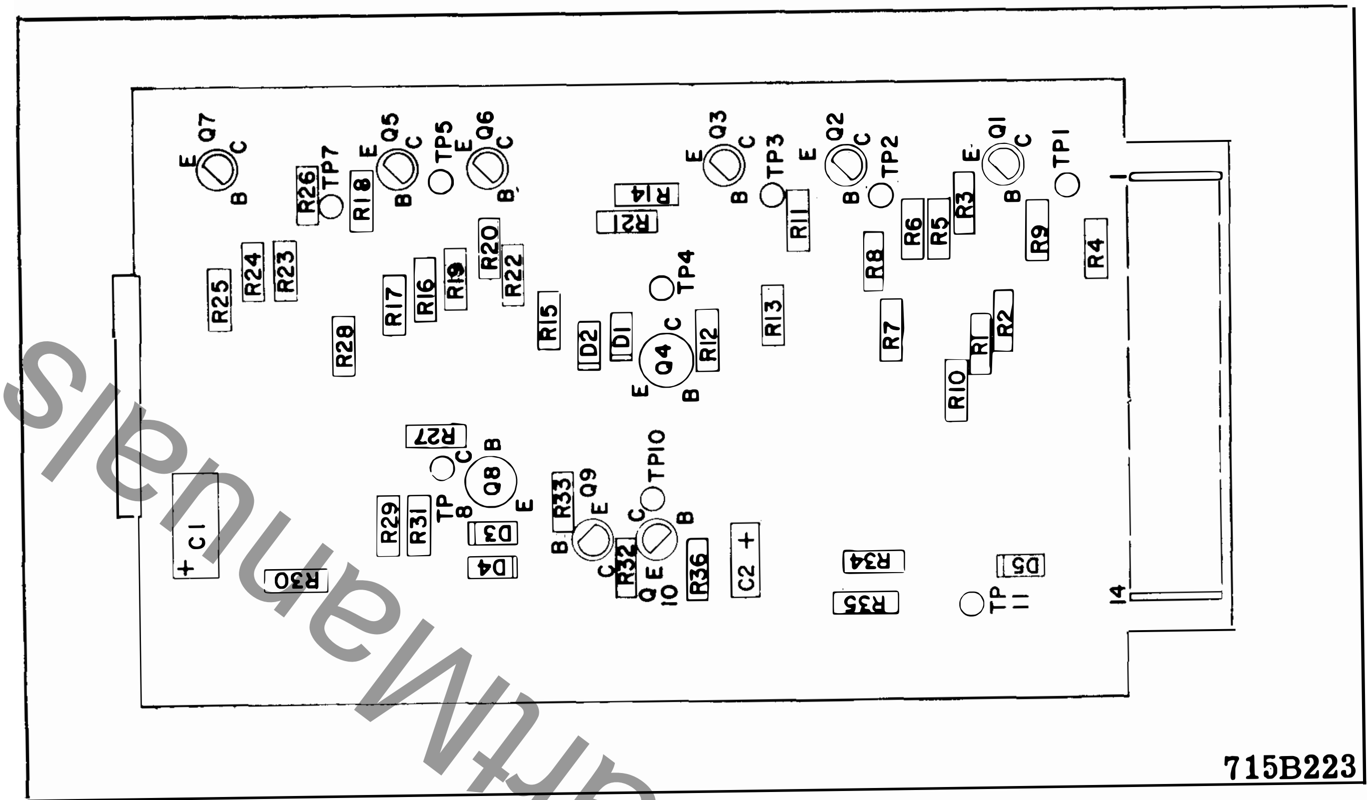


Fig. 36 Component Location Arming Board.

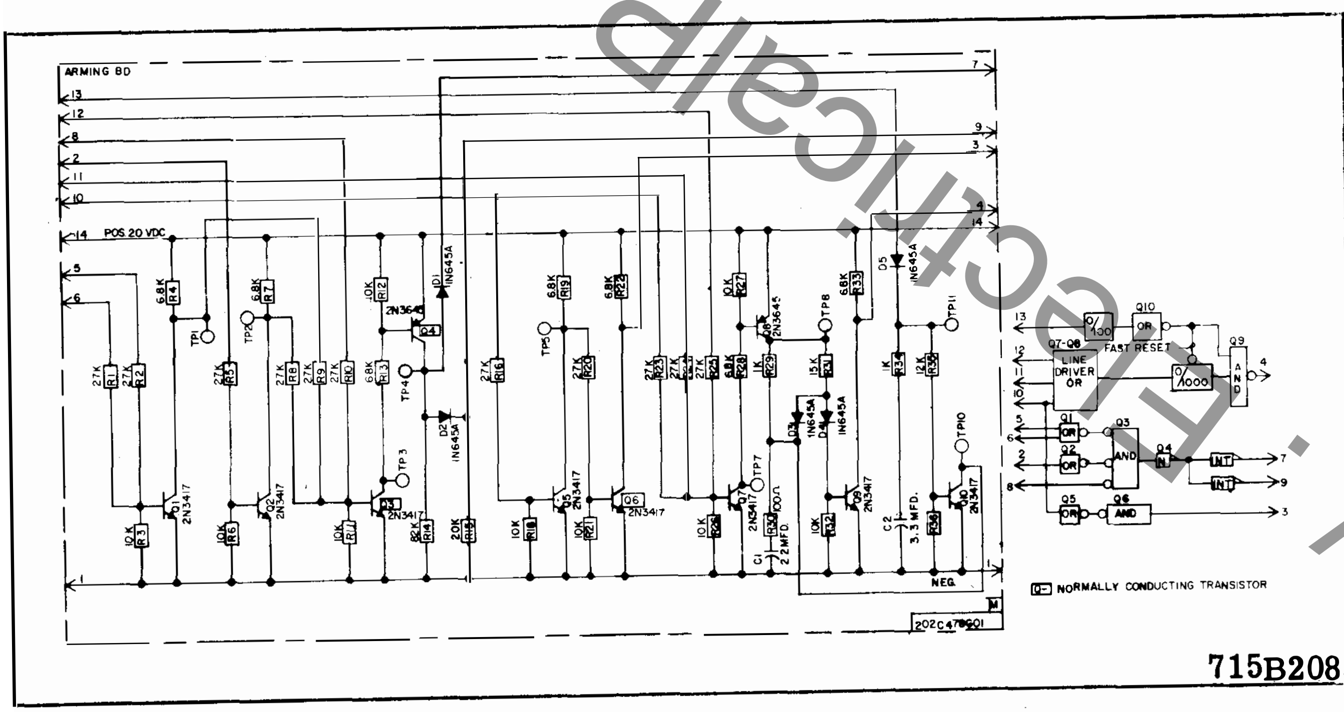


Fig. 37 Internal Schematic Arming Board.

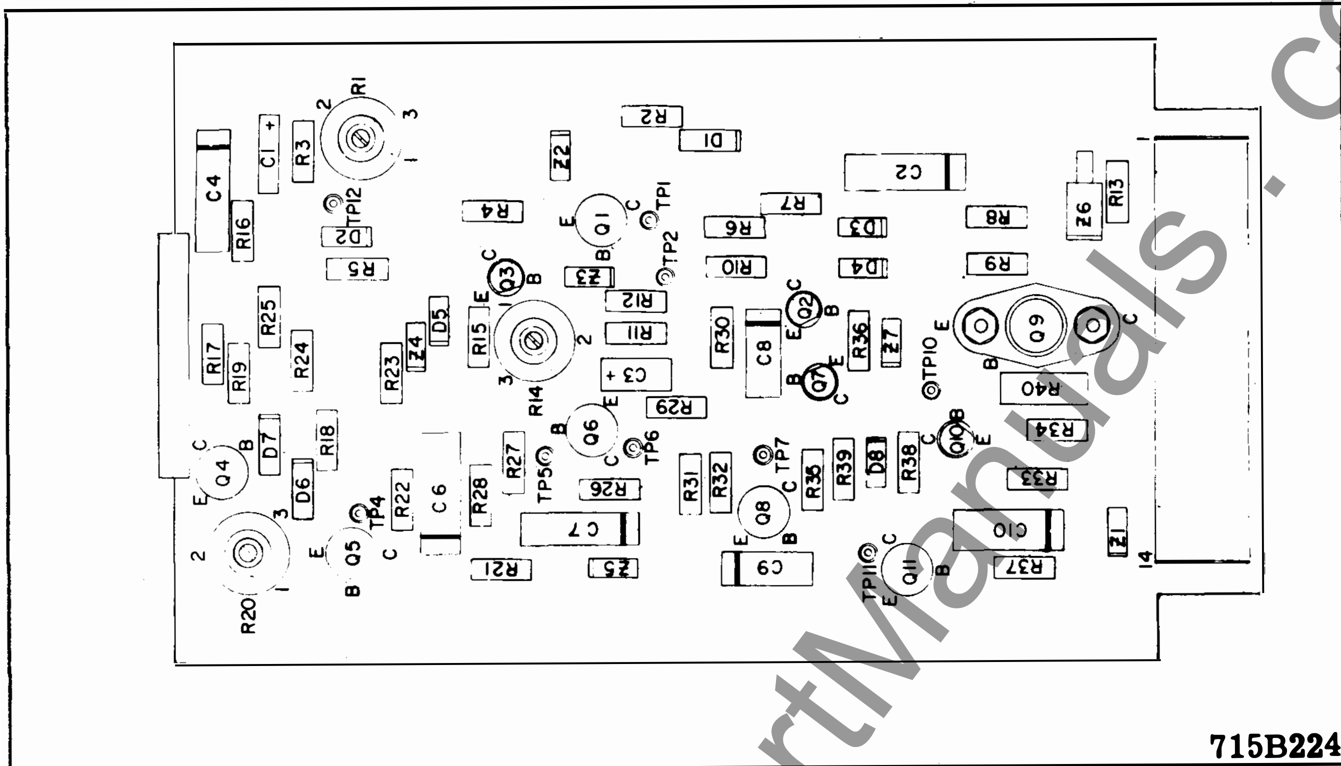


Fig. 38 Component Location Output Board.

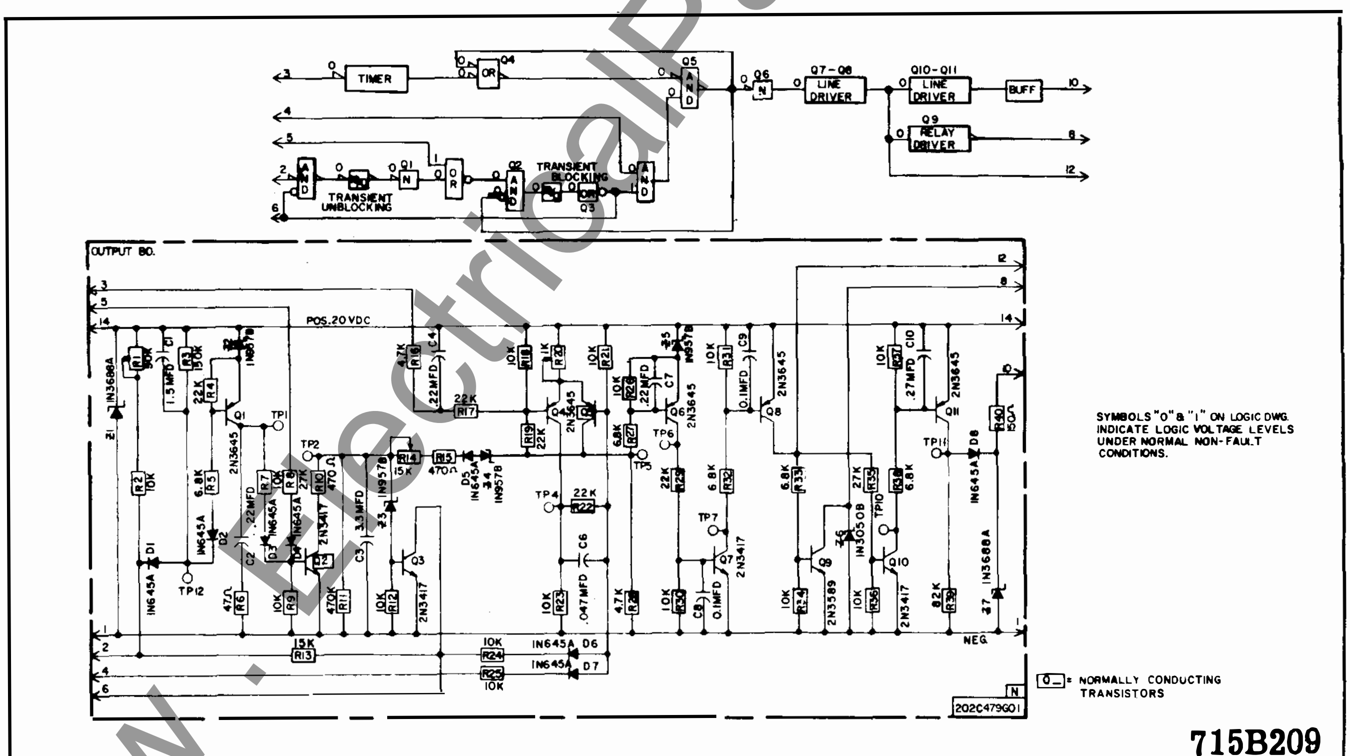


Fig. 39 Internal Schamtic Output Board.

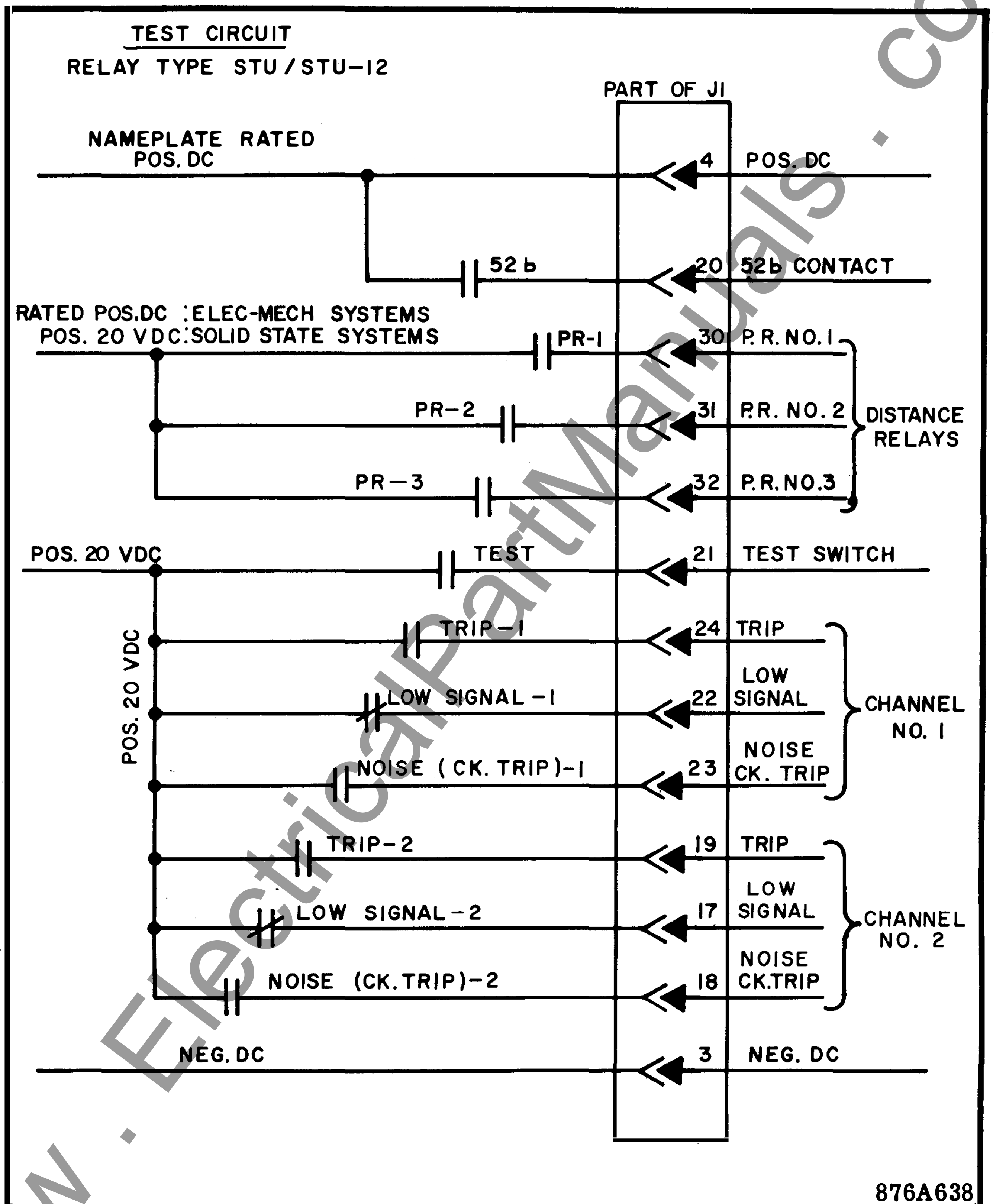


Fig. 40 Test Circuit.

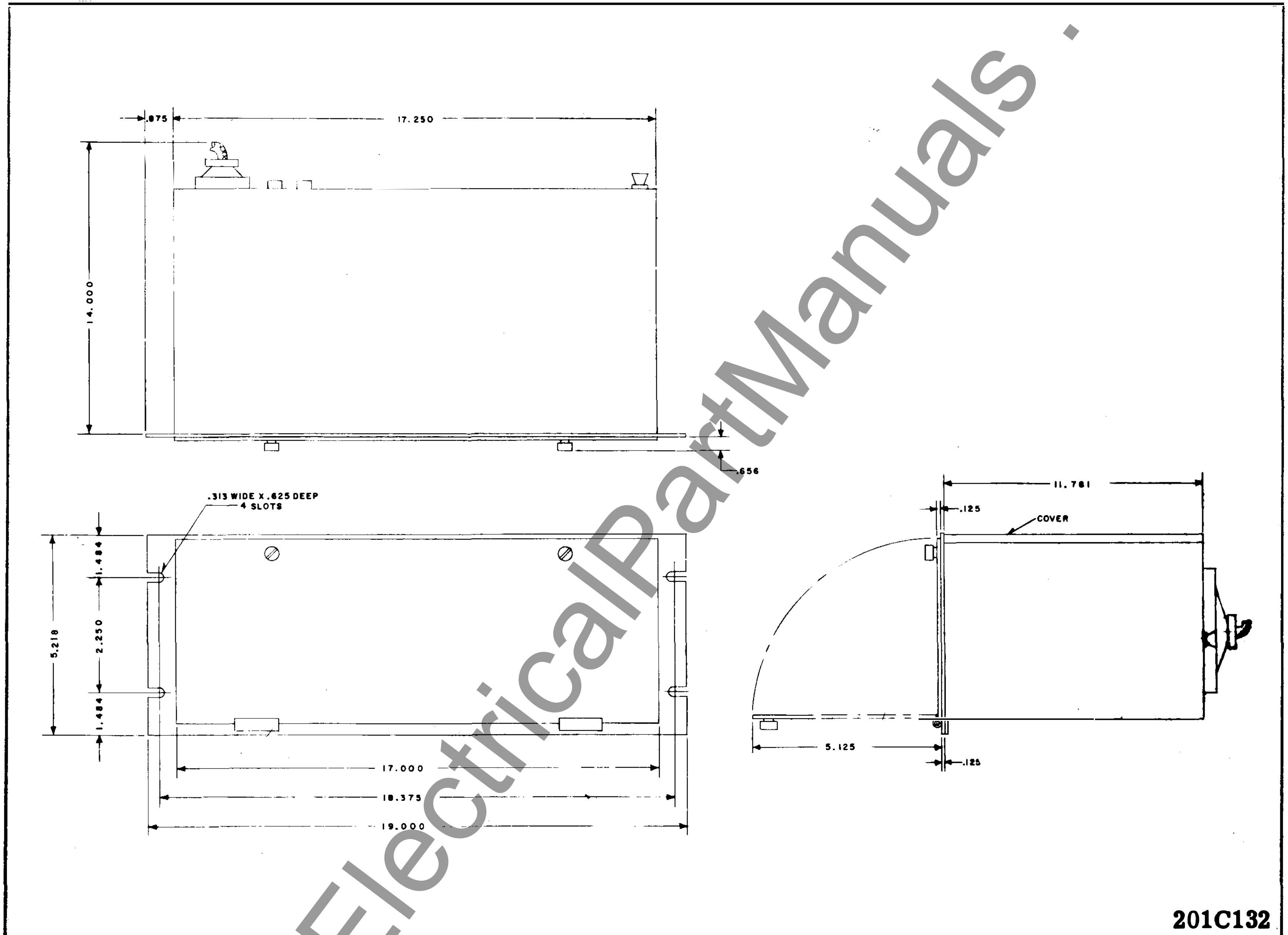


Fig. 41 Outline and Drilling Plan.

WESTINGHOUSE ELECTRIC CORPORATION

RELAY-INSTRUMENT DIVISION **NEWARK, N. J.**

Printed in U.S.A.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

STU-91 AND STU-92 TRANSFER TRIP RELAYS

CAUTION: It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet before energizing the relay.

If transfer into a single channel mode of operation after a loss of one channel is not desired on STU-92 relay, the link on both "OR" boards must be changed to the OPEN position. The relay as shipped will transfer to a single channel mode if one channel is lost.

APPLICATION

The type STU–91 and STU–92 relays are solid state auxiliary relays for use with direct transfer trip systems. Direct transfer trip systems are usually applied to trip a remote breaker for a transformer or shunt reactor fault where no high side breaker exists at the local station. The direct transfer trip relaying system is also applied with breaker failure protection.

The STU–91 relay is for use with single channel transfer trip systems. It provides the channel monitoring logic, channel status indication, thyristor breaker tripping, and trip indication.

If it is desired to have a dual channel transfer trip system; the STU–92 should be used. The STU–92 provides the same logic for both channels as the STU–91 does for a single channel. The logic and tripping of each channel is completely isolated from each other, and where logic signals cross from one channel to the other DC isolation is provided. With this isolation, the STU–92 can provide a dual channel transfer tripping function which will switch to a single channel system if one channel fails. The STU–92 may also be operated such that if one channel fails the relay system is blocked from tripping.

The STU–91 & STU–92 may be used with audio tones or power line carrier equipment. The STU–92 provides further flexibility in that it may be used with dual channel tones, dual channel carrier, or one channel on tones and the other on power line carrier.

CONSTRUCTION

The type STU–92 relay consists of printed circuit boards, tripping AR relays, alarm relays, tripping thyristors, pulse transformers, switches, and monitoring lights mounted on a standard 19-inch wide panel, 7 inches high (4 rack units). Edge slots are provided for mounting the rack on a standard relay rack. The components are connected as shown in Figure 1 and Figure 2.

Printed Circuit Boards

The number of boards varies with the type of frequency shift channel equipment. For a tone channel, the STU–92 relay contains fourteen (14) printed circuit boards: two channel interface boards, two lockout boards, two transfer boards, two relay driver boards, two indicator boards, two OR boards, and two trip boards. For TCF frequency-shift power-line carrier channels, the lockout boards are not required since they are part of the TCF carrier assembly.

The STU–91 relay consists of one-half the boards of the STU–92 relay. For a tone channel, the STU–91 relay contains seven boards: a channel interface board, a lockout board, a transfer board, a relay driver board, an indicator board, an OR board, and a trip board.

All of the circuitry that is suitable for mounting on printed-circuit boards is contained in an enclosure that projects from the rear of the panel and is accessible by opening a removable hinged door on the front of the panel. The printed-circuit boards slide into position in slotted guides at the top and bottom of each compartment, and the board terminals engage a terminal block at the rear of the compartment. Each board and terminal block is keyed so that if a board is placed in the wrong compartment, it cannot be inserted into the terminal block. A handle on the front of each board is labeled to identify its function in the relay.

Following is a description of the STU–91/92 printed circuit boards:

1. CH. INTER (Channel Interface Board)

The interface board contains logic to connect the relay to the channel receiver. It also contains the power supply for the logic circuits of the STU–91 and STU–92 relay that are associated with one channel of the scheme. The following figures apply to this board.

TYPE CHANNEL	SCHEMATIC DIAGRAM	LOCATION OF COMPONENT
TA-3 Tones, TCF Carrier	Fig. 3	Fig. 4
937A Tones	Fig. 5	Fig. 6.

The logic circuits of this board include three buffer inputs, three line drivers, and OR and an AND.

2. Lockout Board (Tone Channel Only)

The lockout board contains the logic to lockout either the STU–92 or STU–91 relay on loss of a tone channel or noise on the channel. The circuits on this board:

a. Lockout the relay 150 milliseconds after a loss of tone channel or a loss of dc voltage on the tone receiver.
b. Initiate intelligence to the transfer board on a lost channel.
c. Lockout the relay when the tone receiver produces a noise clamp.
d. Provide channel trip intelligence to the trip OR of the relay.
e. Provide logic that requires the channel receiver return to a non-trip state after a loss of channel before the relay is enabled on that channel.

This board contains OR circuits, AND circuit and a 150/15 timer circuit. Figure 7 shows the schematic of the board, and Figure 8 shows the location of components on this board.

3. Transfer Board

The transfer boards consists of timing logic that initiates steps to sound an alarm and in the case of the STU–92 relay and to switch from a dual-channel mode of operation to a single channel mode of operation on the loss of one channel.

The circuits of the board include:

A. 500–2500 millisecond adjustable timer which allows a time delay in transferring to a single channel mode of operation after a loss of channel. An alarm relay drops out when the timer times out.
B. Two 10 millisecond timers which delay the inputs to the OR board to assure that tripping is blocked from:
   1. The loss of both channels.
   2. The re-energization of either one or both channels after a loss of both channels.

The schematic of the board is shown in Figure 9, and the location of the components is shown in Figure 10.

4. Relay Driver Board

The relay driver board contains the necessary circuits to drive:

A. The self-resetting white guard light.
B. The tripping relay (AR).
C. The noise and transfer alarm relay (AL)

Two AND circuits, three relay drivers, and a 500/0 timer are located on this board. The 500/0 timer provides a time delay on noise outputs from the channel receiver before the alarm relay drops out.

Figure 11 shows the schematic of the board, and Figure 12 shows the component location on the board.

5. Indicator Board

The indicator board contains the circuits that control all of the lights except the white guard light. These circuits consist of transistors and thyristors which drive the indicator lights. The thyristor requires the presence of an input signal for approximately 10 milliseconds before the thyristor will latch in its conducting state. It will remain in this state until the test switch is hand operated momentarily.

Figure 13 shows the schematic of the board, and Figure 14 shows the component location.

6. OR Board

The OR board either connects the lockout board (for tone channels) or the interface board (for TCF channels) to the trip board of the relay. The circuits of this board will:

A. Provide trip information to the trip board.
B. Allow the STU–92 relay to either lockout or

transfer to a single-channel mode of operation on a loss of channel. A link on the board determines in which manner the STU–92 relay will operate.

1. With the link closed the relay will be locked out on a loss of one channel. Tripping will not occur if a trip signal is received over the remaining good tone channel.
2. With the link open, the relay will operate in a single-channel mode of operation on a loss of one channel. Tripping will not occur if a trip signal is received over the remaining channel.

This function is not provided in the STU–91 relay because the relay is used on a single channel only.

Figure 15 shows the schematic of the board, and Figure 16 shows the component location for the STU–92 relay. Figure 17 shows the schematic of the board and Figure 18 shows the component location for the STU–91 relay.

7. Trip Board

The trip board connects the OR board to the tripping AR and tripping thyristors. This board contains transistor circuitry and isolator circuits that will provide a gate signal to the tripping thyristors.

The following figures apply to this relay:

TRIP VOLTAGE RATING	SCHEMATIC	LOCATION OF COMPONENTS
48/125	Fig. 19	Fig. 20
250	Fig. 21	Fig. 22

AR Tripping Relay

The tripping AR relay is a small high-speed attracted armature type of unit. An insulated member, fastened to the free end of the armature, draws down four moving-contact springs to close the trip-circuit contacts when the relay coil is energized. This relay is mounted on the rear hinged door and is available for inspection by removing the locking screw and swinging the door outward.

Alarm Relay

The alarm relays are telephone type relays. In these relays, an electromagnet attracts a right-angle iron bracket which in turn operates a set of make or break contacts. These relays are mounted on the rear door with the tripping AR relays.

Pulse Transformer

This is a low impedance two-winding iron core transformer. The primary is connected into the trip circuit so that when trip current flows, a pulse is produced in the secondary and fed to the trip light indicator circuit.

Switches

These switches are hand toggle switches with a spring return and are used for resetting the lights as well as testing the light filament.

Lights

All lights are incandescent and removable from the front panel for replacement when necessary. The lights are energized below rated current so that they will have long life but yet provide sufficient illumination.

The lens colors are assigned according to functions. Red is used for trip indication, white for monitoring receipt of a channel guard, and amber for indicating channel noise and trip.

Card Extender

A card extender (style #849A019G01) is available for facilitating circuit voltage measurements or major adjustments. After withdrawing any one of the circuit boards, the extender is inserted in that position. The board then is inserted into the terminal block on the front of the extender. This restores all circuit connections, and all components and test points are readily accessible.

OPERATION

The circuits of the STU–91 and STU–92 relays use the signals from the channel receivers to perform the following functions:

1. The STU–92 relay provides a trip output to the trip coil of a breaker if a trip signal is received by both channel receivers from the remote terminal. For the STU–91 relay, the trip output is provided to the trip coil upon receipt of a trip signal from one channel receiver.
2. For tone channels, both relays prevent tripping of the circuit breakers for a noise clamp from the channel receiver.

3. The relays initiate action to do one of the following for a low-signal clamp from the channel receivers:
   a. For a STU–92 relay, transfer to a single-channel mode of operation after an adjustable time delay. For this condition, the system will trip upon receipt of a trip signal from the remote terminal on the remaining channel.
   b. For tone channels, lockout the STU–91 and STU–92 relays. For this condition, the system will not trip on receipt of a signal from the remote terminal.

   The low signal lockout of the STU–92 relay is determined by the position of a link on the OR board. With the link closed the relay will lockout on the loss of one channel. With the link open, the relay will transfer to a single-channel status, and lockout only on loss of both channels.
4. Both relays provide channel monitoring lights to determine the state of the channels.

When the frequency-shift channel equipment is transmitting a guard signal, the signals to the STU–92 relay are shown on the logic drawings of either Figure 23, 24 or 25. The signals to the STU–91 relay are shown on the logic drawing of Figure 26 and 27. The number "1" indicates that a voltage is obtained at that point, while a "0" indicates that the voltage is approximately zero. As seen in the logic diagrams, the relays require a "1" from the low-signal clamp, and "0" from the trip and noise clamps of the tone channels to indicate normal operating conditions. For the condition shown, the white lights are on and the alarm relays are picked up.

Trip Sequence

For a STU–92 system, both channels are shifted to trip and the "0" from the frequency shift receiver changes to a "1". The channel interface of the STU–92 relay see this change and puts a "1" into either the lockout board (tone channel) or the OR board (TCF channel). In the case of a tone channel, the change in state is applied to OR-2 (lockout board) whose output changes to a "0". This fulfills all the input requirements to AND 5.

1. A "1" from the 150/15 timer.
2. A "0" from OR-2.
3. A "0" from the noise interface.

The output of AND–5 goes to a "1" and the following occurs:

1. A "1" is applied to the relay driver board which will cause the output of AND–1 to change to a "0" thereby turning the white light off.
2. A "1" is applied to the indicator board which energizes driver 3 to turn on the amber channel trip light.
3. A "1" input is applied to OR-1 of the OR board. The output of OR-1 changes to a "0" which is applied to OR-2 and OR-3. With a change in state of the output of OR-2, the input to the isolator on the second OR board changes to a "0" and the output of the isolator to a "0". Since both channels are in a trip state, the output of the isolator on the first OR board changes to a "0" in the same manner. All the inputs to both OR-3 circuits of the two OR boards are thus "0". The outputs on the OR-3 circuits change to a "1" which is applied to the driver of a trip board. In turn, this "1" is applied to:
   a. Relay driver 2 of the driver board which operates the AR unit.
   b. The isolator of the trip board to gate the thyristors. The thyristors conduct to trip the breakers. When breaker trip current flows, the pulse transformers are energized to apply an input to the amplifiers of the indicator board to turn the red breaker trip lights on.

If trip is received only on one frequency shift receiver, the required three inputs to the two OR-3 logics of the OR board are not satisfied, and the STU–92 relay will not operate. For example, if channel 1 receives a trip signal and channel 2 does not, OR-3 of the channel 1 OR board will not be satisfied because of a "1" input from the isolator. OR-3 of the channel 2 OR board will not be satisfied. because of a "1" input from OR-1 of the channel 2 OR board.

The STU–91 operates in the same manner except that its performance is based on a single channel and the input to OR-3 of the OR board from the isolation is not required.

Loss of Channel

With reference to a tone channel, a low signal clamp from the tone receiver clamps into a "0" output, and the signal at terminal 2 of the lockout board changes to a "0" through the channel interface board. This change in signal is applied to OR-4 of the lockout board. Since a "0" input is applied to OR-4, an output is obtained from this circuit and applied to the 150/15 timer. 150 milliseconds later, a "0" output is obtained from the timer which:

1. Locks out AND–5 of the lockout board.
2. Removes one "1" input to OR-3 of the lockout board.
3. Changes the input to AND–1 of the relay driver board to a "0". This changes the output of AND–1 to turn the white guard light off.
4. Changes the input to terminal 2 of the transfer board to a "0". The change in signal energizes the 500–2500 adjustable timer. After a time delay (depending on the timer setting), a "0" output is obtained at terminal 12 of the transfer board which is applied to three logic circuits.

   a. To AND–2 of the relay driver board. The "0" input changes the output of AND–2 to a "0", and the alarm relay drops out to close its contacts.
   b. To a 10/0 timer whose output instantaneously changes to a "1". This "1" is applied to OR-3 of the OR board to lockout OR-3 of that channel.
   c. To a 0/10 timer whose output changes to "1" 10 milliseconds later. This change in signal is applied to OR-1 and OR-2 of the OR board. The output of OR-1 changes to a "0" and is applied to OR-2 and OR-3. If the link is closed, the output of OR-2 does not change status, (because of "1" input from 0/10 timer) and the output of the isolator on the second channel OR board does not change state. Thus, the OR-3 circuit of the second OR board is locked out. If the link is open, the output of OR-2 (on OR board) will change to a "0". This changes the output of the isolator of the second OR board to a "0". This applies two "0" signals to OR-3 of this board, and tripping will occur if the receiver of the good channel gives a trip output.

If a trip signal is supplied to either the STU–92 relay or the STU–91 relay from the non-serviceable channel during a loss of channel condition, a "1" input is applied to OR-2 of the lockout board. OR-2 inverts the signal and applies a "0" to AND–5 and OR-3 of the lockout board. Since AND–5 had been previously locked out from the 150/15 timer (due to loss of channel) the output of AND–5 remains at "0". The change in signal to OR-3 causes a "1" input to OR-4 to hold the 150/15 timer picked up. Since AND–5 is locked out, tripping will not occur due to the trip input from the non-serviceable channel. However, for STU–92 relay tripping can occur on the remaining channel if the relay had been set to transfer to a single-channel status after the loss of one channel.

For the condition where the channel has been lost AND–5 will remain locked out when the channel is restored to normal if the channel receiver returns in a trip state. When loss of channel occured, the 150/15 timer picked up and applied a "0" to one input of OR-3. If a trip is received with this condition, then the other OR-3 input will become "0" and the output of OR-3 will go to "1" thereby applying an input to OR-4 thus preventing the 150/15 timer from dropping out. The trip signal must be removed from the lockout board before the 150/15 timer drops out to return AND-5 to normal.

With reference to a TCF carrier channel, the lockout features are included as a part of the TCF carrier receiver.

Loss of Second Channel

If the second channel is lost while the STU–92 relay is set up in a single-channel mode of operation, the following occurs:

1. The output of the low signal clamp interface changes to "0".
2. After a 150 millisecond time delay, AND–5 of the lockout board of second channel is clamped to a "0".
3. A "0" input is applied to the AND–1 of the relay driver board. This changes the output of AND–1 to turn the white guard light off.
4. A "0" input is applied to the 500–2500 timer of the transfer board, and the timer is energized. After a time delay (as determined by the setting), the 10/0 and 0/10 timers of the transfer board are energized. Instantaneously the 10/0 timer drops out to apply a "1" input to OR-3 of the OR board. This disables OR-3. 10 milliseconds later, the 0/10 timer times out to apply a "0" input to OR-3 through OR-1. An output from the 500–2500 timer also causes an alarm to dropout through AND–2 of the relay BD.

For the condition where both channels are out of service and one or both channels are restored to service, instantaneously the 0/10 millisecond timer puts a "0" into OR-1, thus a "1" into OR-3, and the 10/0 millisecond timer takes 10 milliseconds to change its input to OR-3 to a "0". Hence, OR-3 is locked out during the restoration period.

Noise

If an output is obtained from the noise clamp on the frequency shift receiver, the output of the noise interface circuit on the CH INTER board changes to a "1". This signal is applied to a 500/0 timer of the Relay Driver Board. After 500 milliseconds, the timer times out to apply a "1" input to AND–2 of the Relay Driver Board and the indicator circuit of the Indicator Board. This causes the alarm relay to drop out and the noise amber light to turn on.

In the case of a tone channel, the output of the noise interface circuit is applied to the lockout board. This input locks out AND–5 on this board to prevent tripping during the noise condition.

CHARACTERISTICS

The STU–92 relay is available for frequency-shift channels, either tone, carrier or a combination as shown in the logic diagrams 23, 24 and 25. The STU–91 relay is available for frequency shift tones or carrier as shown in the logic diagrams, Figures 26 and 27. Following are the three (3) types of trip outputs provided.

1. Thyristor Trip
2. Relay Trip
3. Voltage Trip

Noise Alarm Time	500 Milliseconds
Lockout Time (Tone Channel Only) (Lockout Time provided in TCF channel, when used)	150 Milliseconds
Transfer Time	Adjustable 0.5 to 2.5 Seconds
Operating Time	3 Milliseconds with AR Relay Output 75 Microseconds for solid-state thyristor or voltage output.
Maximum Allowable Output Current on Voltage Output Terminals	10 milliamperes at 20 volts dc
Ambient Temperature Range	-20°C to +55°C

Battery Voltage Variations

Rated Voltage	Allowable Variation
48 V DC	42-56 V DC
125 V DC	105-140 V DC

Battery Drain Normal	125 milliamperes - 48 V DC
	110 milliamperes - 125 V DC
Maximum	300 milliamperes - 48 V DC
	250 milliamperes - 125 V DC

Setting

The only setting required is the setting of the timer for transferring to a single-channel mode of operation upon a loss of one channel. This setting is made by means of the knob on the front of the transfer board of the relay. This knob should be locked after the setting is made.

If the application requires that the relay lockout after a loss of a single channel, the link on the two OR boards should be changed to the closed position.

Installation

The STU–92 and STU–91 relays are generally supplied in a cabinet or on a relay rack as part of a complete assembly. The location must be free from dust, excessive humidity, vibration, corrosive fumes, or heat. The maximum temperature around the chassis must not exceed 55°C.

Routine Maintenance

Periodic checks of the relaying system as described in the assembly instructions are desirable to indicate impending failure so that the equipment can be taken out of service for correction.

All contacts should be periodically cleaned. A contact burnisher S#182A836H01 is recommended for this purpose. The use of abrassive material for cleaning is not recommended because of the danger of embedding small particles in the face of the soft silver and thus imparing the contacts.

ADJUSTMENTS AND MAINTENANCE

The Acceptance Test listed below can be followed to verify that the STU–91 or STU–92 relays are functioning properly.

Acceptance Test

Connect the relay to the test circuit of Figure 24 which for test purposes represents the system to which the STU–92 relay is connected. The switches shown represent 20 volt inputs to the relay. These inputs can be placed on the relay by the circuit or by jumpering the correct board terminals to the internal 20 volt board terminal.

For the STU–91 relay, only the information to channel 1 need be considered.

Test Equipment:

1. Timer or Cathode Ray Oscilloscope
2. Card Extender Style 849A534G01

With a jumper, connect the link on both "OR" boards. Close dc power switches 1 and 2: (1) White lamps will light, (2) Alarm relays will pickup.

Check lamps by means of test reset switches 1 and 2. All channel 1 lamps should light when test switch 1 is open, and all channel 2 lamps should light when test reset switch 2 is open.

I. Trip Circuit

A. Close channel 1 trip switch.
   1. White lamp of channel 1 will go off.
   2. Amber channel trip lamp of channel 1 will light.

B. With channel 1 trip switch closed, close channel 2 trip switch.
   1. WL switches will operate.
   2. Red breaker trip lamps will light
   3. External trip light will light.
   4. White lamp of channel 2 will go off.
   5. Amber channel trip lamp of channel 2 will light.

C. Open both channel 1 and channel 2 switches. Reset lamps and WL switches.

II. Noise Circuit (500 Millisecond Timer)

A. Channel 1

   1. Connect timer start (scope trigger) to terminal 8 of CH INTER board (A board).
   2. Set timer start (scope trigger) to positive pulse.
   3. Connect timer stop (scope probe) to terminal 13 of channel 1 relay driver board (D board). Connect ground to terminal 1 of the board.
   4. Close channel 1 noise switch.
      a. Timer (scope) will start and stop after 440 to 560 milliseconds.
      b. Channel 1 amber noise lamp will light.
      c. Channel 1 alarm relay will drop out.
   5. Open channel 1 noise switch. Reset lamps.

B. Channel 2

   1. Connect timer start (scope trigger) to terminal 8 of CH INTER board (F board).
   2. Set timer start (scope trigger) to positive pulse.
   3. Connect timer stop (scope probe) to terminal 13 of channel 2 relay driver board (I board). Connect ground to terminal 1 of the board.
   4. Close channel 2 Noise Switch.
      a. Timer will start and stop after 440 to 560 milliseconds.
      b. Channel 2 amber noise lamp will light.
      c. Channel 2 alarm relay will drop out.
   5. Open channel 2 Noise Switch. Reset lamps

C. Lockout (Tone Channel Only - where boards B or G are used)

   1. Close channel 1 Noise Switch.
      a. Channel 1 alarm relay will drop out.
      b. Channel 1 noise lamp will light.
   2. Close channel 1 and channel 2 trip switches. Channel 2 guard lamp will go off and channel 2 trip lamp will light.
   3. Open channel 1 Noise Switch.
      a. WL relays will operate.
      b. External trip light will light.
      c. Channel 1 guard lamp will go out.
      d. Channel 1 amber trip lamp will light.
      e. 4 red breaker trip lamps will light.
   4. Open channel 1 and 2 trip switches and reset lamps. If board G is not used go to step III.
   5. Close channel 2 Noise Switch.
      a. Channel 2 alarm relay will drop out.
      b. Channel 2 noise lamp will light.
   6. Close channel 1 and channel 2 trip switches. Channel 1 guard lamp will go off and channel 1 trip lamp will light.
   7. Open channel 2 Noise Switch.
      a. WL relays will operate.
      b. External trip light will light.
      c. Channel 2 guard lamp will go out.

d. Channel 2 amber lamp will light.
e. 4 red breaker trip lamps will light.

8. Open channel 1 and 2 trip switches and reset lamps.

III. Low Signal Clamp (Tone Channel Only - where boards B or G are used)

A. Channel 1

1. 150 Millisecond Timer
   a. Connect timer start (scope trigger) to terminal 5 of CH INTER (A board)
   a. Set timer start (scope trigger) to negative pulse.
   c. Connect timer stop (scope probe) to terminal 13 of channel 1 lockout board (B board). Set timer stop on negative pulse.

      Use terminal 1 as common or ground.
   d. Open channel 1 low-signal switch.
      1. Timer (scope) will start and stop after a time delay of 125 to 185 milliseconds (scope voltage will drop from 20 volts to 0 volts in same time).
      2. Channel 1 guard lamp will go out.
      3. After a time delay, channel 1 alarm relay will drop out.
2. 15 Millisecond Delay.
   a. Set timer start (scope trigger) to positive pulse.
   b. Close channel 1 low-signal switch. Timer should start and should stop after a delay of 12 to 18 milliseconds (scope voltage will change from 0 volts in the same time).
   c. Open channel 1 low-signal switch
3. Guard Return
   a. Close channel 1 and channel 2 trip switches.
      1. Channel 2 guard lamp will go out.
      2. Channel 2 trip lamp will light.
   b. Close channel 1 low-signal clamp switch. No change in status should occur.
   c. Open channel 1 trip switch.
      a. Channel 1 guard lamp will light.
      2. Channel 1 alarm relay will pickup.
   d. Open channel 2 trip switch and reset lamps.

B. Channel 2 (If board G not used to to step IV)

1. 150 Millisecond Timer.
   a. Connect timer start (scope trigger) to terminal 5 of CH INTER (F board).
   b. Set timer start (scope trigger) to negative pulse.
   c. Connect timer stop (scope probe) to terminal 13 of channel 2 lockout board (G board). Set timer stop on negative pulse.

      Use terminal 1 as common or ground.
   d. Open channel 2 low-signal switch.
      1. Timer (Scope will start and stop after a time delay of 125 to 185 milliseconds (scope voltage will drop from 20 volts to 0 volts in same time).
      2. Channel 2 guard lamp will go out.
      3. After a time delay, channel 2 alarm relay will drop out.
2. 15 Millisecond Delay
   a. Set timer start (scope trigger) to positive pulse.
   b. Close channel 2 low-signal switch. Timer should start and should stop after a delay of 12 to 18 milliseconds (scope voltage will change from 0 volts to 20 volts in same time).
   c. Open channel 2 low-signal switch.
3. Guard Return
   a. Close channel 2 and channel 2 trip switches.
      1. Channel 1 guard lamp will go out.
      2. Channel 1 trip lamp will light.
   b. Open channel 2 low signal clamp switch. No change in status should occur.
   c. Open channel 2 trip switch.
      1. Channel 2 guard lamp will light.
      2. Channel 2 alarm relay will pickup.
   d. Open channel 1 trip switch and reset lamps.

IV. Transfer Timers

A. Channel 1

1. Adjustable 500 to 2500 Millisecond Timer

a. Connect timer start (scope trigger) to terminal 2 of channel 1 transfer board (C board).
b. Set timer start (scope trigger) to negative pulse.
c. Connect timer stop (scope probe) to red test point on front of transfer module. Set timer stop on negative pulse. Use black test point on front of module as common or ground.
d. Set timer knob at minimum setting.
e. Open channel 1 low-signal clamp switch.
   1. Timer should start and stop within ±5% of the time specified on the calibration plate (scope voltage will drop from 20 volts to zero volts in same time).
   2. Check each setting of timer by moving knob to that setting. Time should be within ±5% of marking.
f. Close channel 1 low-signal clamp switch.

2. 0/10 Timer
   a. Connect timer start (scope trigger) to red test point of channel 1 transfer board (C board).
   b. Set timer start (scope trigger) to negative pulse.
   c. Connect timer stop (scope probe) to terminal 13 of channel 1 transfer board (C board). Set timer stop on positive pulse. Use black test point or terminal 1 as common or ground.
   d. Open channel 1 low-signal clamp switch. Timer should start and stop after a time delay of 7 to 13 milliseconds (scope voltage will change from zero to 13.5 volts in same time).
   e. Set timer start (scope trigger) to positive pulse.
   f. Set timer stop to negative pulse.
   g. Close channel 1 low-signal clamp switch. Timer should start and stop in less than 1 millisecond (scope voltage will change from 13.5 volts to zero volts in same time).

3. 10/0 Timer
   a. Connect timer start (scope trigger) to red test point of channel 1 transfer board.
   b. Set timer start (scope trigger) to negative pulse.
   c. Connect timer stop (scope probe) to terminal 8 of channel 1 transfer board (C board). Set timer stop on positive pulse. Use black test point or terminal 1 as common or ground.
   d. Open channel 1 low-signal clamp switch. Timer should start and stop after a time delay of less that 1 millisecond. (Scope voltage will change from zero volts to 9 volts in same time.)
   e. Set timer start (scope trigger) to positive pulse.
   f. Set timer stop to negative pulse.
   g. Close channel 1 low-signal clamp switch. Timer should start and stop after a time delay of 7 to 13 ms (scope voltage will change from 9 volts to 0 volts in same time).

B. Channel 2

1. Adjustable 500 to 2500 Millisecond Timer
   a. Connect timer start (scope trigger) to terminal 2 of channel 2 transfer board (H board).
   b. Set timer start (scope trigger) to negative pulse.
   c. Connect timer stop (scope probe) to red test point on front of transfer module. Set timer stop on negative pulse. Use black test point on front of module as common or ground.
   d. Set timer knob at minimum setting.
   e. Open channel 2 low-signal clamp switch.
      1. Timer should start and stop within ±5% of the time specified on the calibration plate (scope voltage will drop from 20 volts to zero volts in same time).
      2. Check each setting of timer by moving knob to that setting. Time should be within ±5% of marking.
   f. Close channel 2 low-signal clamp switch.

2. 0/10 Timer
   a. Connect timer start (scope trigger) to red test point of channel 2 transfer board (H board).

b. Set timer start (scope trigger) to negative pulse.

c. Connect timer stop (scope probe) to terminal 13 of channel 2 transfer board (H board). Set timer stop on positive pulse. Use black test point or terminal 1 as common or ground.

d. Open channel 2 low-signal clamp switch. Timer should start and stop after a time delay of 7 to 13 milliseconds (scope voltage will change from zero volts to 13.5 volts in same time).

e. Set timer start (scope trigger) to positive pulse.

f. Set timer stop to negative pulse.

g. Close channel 2 low-signal clamp switch. Timer should start and stop in less than 1 millisecond (scope voltage will change from 13.5 volts to zero volts in same time).

3. 10/0 Timer

a. Connect timer start (scope trigger) to red test point of channel 2 transfer board.

b. Set timer start (scope trigger) to negative pulse.

c. Connect timer stop (scope probe) to terminal 8 of channel 2 transfer board (H board). Set timer stop on positive pulse. Use black test point on terminal 1 as common or ground.

d. Open channel 2 low-signal clamp switch. Timer should start and stop after a time delay of less than 1 millisecond. (Scope voltage will change from zero volts to 9 volts in same time.)

e. Set timer start (scope trigger) to positive pulse.

f. Set timer stop to negative pulse.

g. Close channel 2 low-signal clamp switch. Timer should start and stop after a time delay of 7 to 13 milliseconds (scope voltage will change from 9 volts to zero volts in same time.)

V. Transfer To Single Channel

A. Loss of Signal

1. Open link on both "OR" boards by removing jumper placed there at beginning of test.
2. Open channel 1 low-signal clamp switch. Channel 1 white guard lamp will go off.
3. After STU–92 has transferred to a single channel as indicated by alarm relay dropping out, close channel 2 trip switch.
4. External trip light will light, and WL relays will operate, breakers 1 and 2, trip 2 red lamps will light, white lamp of channel 2 will go off and amber trip lamp of channel 2 will light.
5. Close channel 1 low-signal clamp switch, and open channel 2 trip switch, reset lamps and WL switches.
6. Open channel 2 low-signal clamp switch. Channel 2 white guard lamp will go off.
7. After STU–92 has transferred to a single channel as indicated by alarm relay dropping out, close channel 1 trip switch.
8. External trip light will light and WL relays will operate, breakers 1 and 2 trip 1 red lamps will light, white lamp of channel 1 will go off, and amber trip lamp of channel 1 will light.
9. Close channel 1 low-signal clamp switch, and open channel 1 trip switch, reset lamps and WL switches.

B. Loss of DC Voltage

1. Open dc power supply switch 1.
   a. Alarm relay 1 should drop out.
   b. White guard light 1 should go out.
2. Close trip switch of channel 2.
   a. WL should operate.
   b. Red breaker trip lamps of channel 2 should light.
   c. Amber trip lamp of channel 2 will light.
   d. External trip light should light.
3. Open trip switch of channel 2, close dc power supply switch 1, and open dc power supply switch 2.

a. Alarm relay 2 should drop out.
b. White guard light 2 should go out.

4. Close trip switch of channel 1.
   a. WL should operate.
   b. Red breaker trip lamps of channel 1 should light.
   c. Amber trip lamp of channel 1 will light.
   d. External trip light should light.

Tripping Relay (AR)

The type AR tripping relay unit has been properly adjusted at the factory to insure correct operation and should not be disturbed after receipt by the customer. If, however, the adjustments are disturbed in error, or it becomes necessary to replace some part in the field, use the following adjustment procedure. This procedure should not be used until it is apparent that the AR unit is not in proper working order, and then only if suitable tools are available for checking the adjustments.

a. Adjust the set screw at the top of the frame to obtain a 0.009 inch gap at the rear end of the armature air gap.

b. Adjust each contact spring to obtain 4 grams pressure at the very end of the spring. This pressure is measured when the spring moves away from the edge of the slot in the insulated crosspiece.

c. Adjust each stationary contact screw to obtain a contact gap of 0.020 inch. This will give 15–30 grams contact pressure.

Trouble Shooting

The components of the STU–92 and STU–91 relays are operated well within their ratings, and under normal conditions, they should give long, trouble-free service. However, if a relay has given an indication of trouble in service or during routine checks, the "truth tables" of Figure 32 should be checked to determine the faulty component. All voltages are measured with respect to negative except where noted.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing the repair work. When ordering parts, always give the complete nameplate data, and style numbers from the electrical parts list.

ELECTRICAL PATRS LIST

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
INTERFACE BOARD S#202C482G01		
Capacitors		
C1	6.8 MFD	184A661H10
C2,C3,C4	0.047 MFD	849A437H04
Diodes		
D1	1N645A	837A692H03
Transistors		
Q1	2N3589	837A617H01
Q2,Q4, Q6	2N3417	848A851H02
Q3,Q5,Q7	2N3645	849A441H01
Resistors		
R1,R2,R8,R9,R15,R16	4.7 k-ohm	629A531H48
R3,R7,R17,R21	82 k-ohm	629A531H78
R4,R5,R11,R12,R18,R19	10 k-ohm	629A531H56
R6,R13,R20	6.8 k-ohm	629A531H52
R14	47 k-ohm	629A531H72
Zener Diodes		
Z1	1N3050A, 120 V	187A936H16
Z2	1N4747A, 20 V	849A487H01
Z3,Z5,Z7	1N3686B, 20 V	185A212H06
Z4,Z6,Z8	1N957B, 6.8 V	186A797H06
INTERFACE BOARD S#202C491G01		
Capacitors		
C1	6.8 MFD	184A661H10
C2,C3,C4	0.047 MFD	849A437H04
Diodes		
D1	1N645A	837A692H03
Transistors		
Q1	2N3589	837A617H01
Q2.Q5,Q8	2N4356	849A441H02
Q3,Q6,Q9	2N3417	848A851H02
Q4,Q7,Q10	2N3645	849A441H01
INTERFACE BOARD S#202C491G01 Cont.		
Resistors		
R1,R2,R5,R6,R13,R14	4.7 k-ohm	629A531H48
R3,R7,R12,R21,R27	82 k-ohm	629A531H78
R4,R9,R10,R15,R17,R18 R22,R24,R25	10 k-phm	629A531H56
R8,R16,R20,R23	47 k-ohm	629A531H72
R11,R19,R26	6.8 k-ohm	629A531H52
Zener Diodes		
Z1	1N2050A, 180 V	187A936H16
Z2	1N4747A, 20 V	849A487H01
Z3,Z5,Z7	1N3686B, 20 V	185A212H06
Z4,Z6,Z8	2N957B, 6.8 V	186A797H06
Z9	UZ5875, 75 V	837A693H04
LOCKOUT BOARD (WHERE USED) S#202C456G01		
Capacitors		
C1	6.8 MFD	184A661H10
Diodes		
D1 to D4-D6 to D10	1N645A	837A692H03
Transistors		
Q1,Q2,Q3,Q4,Q5,Q6 Q7,Q8,Q9,Q11	2N3417	848A851H02
Q10, Q12	2N3645	849A441H01
Resistors		
R1,R4,R7,R14,R25	39 k-ohm	629A531H70
R2,R5,R8,R11,R15 R19,R22,R26,R29, R30,R34,R35	10 k-ohm	629A531H56
R3,R9,R16,R23,R27 R31,R36	6.8 k-ohm	629A531H52
R6, R13, R33	33 k-ohm	629A531H68
R10,R12,R17,R18 R20, R21, R28	27 k-ohm	629A531H66
R24, R38	12 k-ohm	629A531H58
R32	82 k-ohm	629A531H78
R37	47 k-ohm	629A531H72

ELECTRICAL PARTS LIST Cont.

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
LOCKOUT BOARD (WHERE USED) S#202C456G01		
Zener Diodes		
Z1	1N957B, 6.8 V	186A797H06
OR BOARD S#202C446G01		
Capacitors		
C1-C2	0.27 MFD	849A437H02
C3	1.5 MFD	187A508H09
Diodes		
D1,D2,D4 to D15	1N645A	837A692H03
D3	MAL3053	629A370H04
Transistors		
1Q,Q3,Q4,Q5,Q6,Q7	2N3417	848A851H02
Q2,Q8	2N3645	849A441H01
Resistors		
R1,R3,R5,R7,R10 R14,R21,R24,R25	10 k-ohm	629A531H56
R2,R8,R11,R15,R22,R26	6.8 k-ohm	629A531H52
R4	47 k-ohm	629A531H72
R6	4.7 k-ohm	629A531H48
R9,R12,R13,R16,R17 R18,R19,R20,R23	27 k-ohm	629A531H66
R27	82 k-ohm	629A531H78
R28	150 ohm, 3W	762A679H01
Transformers		
TR1	FD 505	629A372H01
Zener Diodes		
Z1,Z2	1N3688A, 24 V	872A288H01
TRIP BOARD 48/125 VOLTS DC, S#899C826G01 250 VOLTS DC, S#201C416G01		
Capacitors		
C1,C2	2 MFD	187A624H05
C3,C4	.27 MFD	188A669H05

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
TRIP BOARD (Cont.) 48/125 & 250 VOLTS DC		
Diodes		
D1 to D4	1N645A	837A692H03
Transistors		
Q1	2N2647	629A453H01
Q1	2N3645	849A441H01
Q3	2N3417	848A851H02
Resistors		
R1 to R4	470 ohm, 1W	187A643H19
R5	300 ohm	629A531H19
R6	15 k-ohm	629A531H60
R7	3.3 k-ohm	629A531H44
R8	22 k-ohm	629A531H64
R9	6.8 k-phm	629A531H52
R10	10 k-ohm	629A531H56
R11 to R13	27 k-ohm	629A531H66
Zener Diodes		
Z1 to Z6	1R200	629A369H01
Transformer		
TR1	FD505	629A372H01
TRANSFER BOARD, S#5489D25G01		
Capacitors		
C1	100 MFD	184A761G01
C2,C3	1.5 MFD	187A508H09
Diodes		
D1 to D4	1N645A	837A692H03
Transistors		
Q1,Q2,Q3,Q5,Q6 Q7,Q8,Q9,Q10	2N3417	848A851H02
Q4	2N3645	849A441H01

ELECTRICAL PARTS LIST (Cont.)

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
TRANSFER BOARD, S#5489D25G01 (Cont.)		
Resistors		
R1,R12,R17,R21,R29	33 k-ohm	629A531H68
R2,R3,R6,R9,R10 R13,R16,R19,R22 R25,R28	10 k-ohm	629A531H56
R4,R15,R27	470 ohm	629A531H24
R5	50 k-ohm pot.	862A303H01
R7,R8,R18,R23,R24	27 k-ohm	629A531H66
R11	47 k-ohm	629A531H72
R14,R26	15 k-ohm	629A531H60
R20	6.8 k-ohm	629A531H52
Zener Diodes		
Z1,Z2,Z3	1N957B, 6.8V	186A797H06
RELAY DRIVER, S#202C488G01		
Capacitors		
C1	22 MFD	184A661H16
Diodes		
D1 to D4	1N645A	837A692H03
Transistors		
Q1,Q2,Q4,Q5,Q6 Q8,Q9	2N3417	848A851H02
Q3,Q10,Q11	2N3589	837A617H01
Q7	2N3645	849A441H01
Resistors		
R1,R5,R26	39 k-ohm	629A531H70
R2,R6,R9,R12,R15,R18, R19,R23,R27,R30,R32	10 k-ohm	629A531H56

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
RELAY DRIVER, S#202C488G01		
Resistors		
R3,R4,R24,R25	22 k-ohm	629A531H64
R7,R8,R28,R29	3.3 k-ohm	629A531H44
R10	15 ohm, 3 W	763A127H36
R11,R13,R14	33 k-ohm	629A531H68
R14,R20,R21	47 k-ohm	629A531H72
R17	470 ohm	629A531H24
R22	27 k-ohm	629A531H66
R31	6.8 k-ohm	629A531H52
Zener Diodes		
Z1	1N3688A, 24V	862A288H01
Z2	1N957B, 6.8V	186A797H06
INDICATOR BOARD 48 VOLT DC, S#202C502G01		
Capacitors		
C1,C2	0.56 MFD	763A219H18
C3,C5,C7,C9	0.082 MFD	849A437H01
C4,C6,C8,C10	0.01 MFD	763A219H03
Diodes		
D1 to D10	1N645A	837A692H03
Transistors		
Q1,Q3	2N3417	848A851H02
Q2,Q4	2N3645	849A441H01
Q5,Q7,Q9,Q11	2N2646	629A43: H03
Q6,Q8,Q10,Q12	K1149-13 SCR	184A640H13
Resistors		
R1,R2,R7,R8,R13,R17	20 k-ohm	629A531H63
R3,R4,R9, R10	10 k-ohm	629A531H56
R5,R11	6.8 k-ohm	629A531H52
R6,R12	27 k-ohm	629A531H66
R14,R18,R22,R26	300 ohms	629A531H19
R15,R19,R23,R27	51 ohms	629A531H01
+R16, R20,R24,R28	1.2 k-ohms, 3W	763A127H03
R21,R25	100 k-ohm	629A531H80
R29	15 ohms, 3W	763A127H36

+ NOT USED ON 48 VOLT DC INDICATOR BOARD

FRONT VIEW
(COVER REMOVED)

BOARD POSITION		BOARD DESCRIPTION
CHANNEL 1	CHANNEL 2	
A	F	INTERFACE
B	G	LOCKOUT (TONE CHANNEL ONLY)
C	H	TRANSFER
D	I	RELAY DRIVER
E	J	OR
K	N	INDICATOR
L	O	TRIP

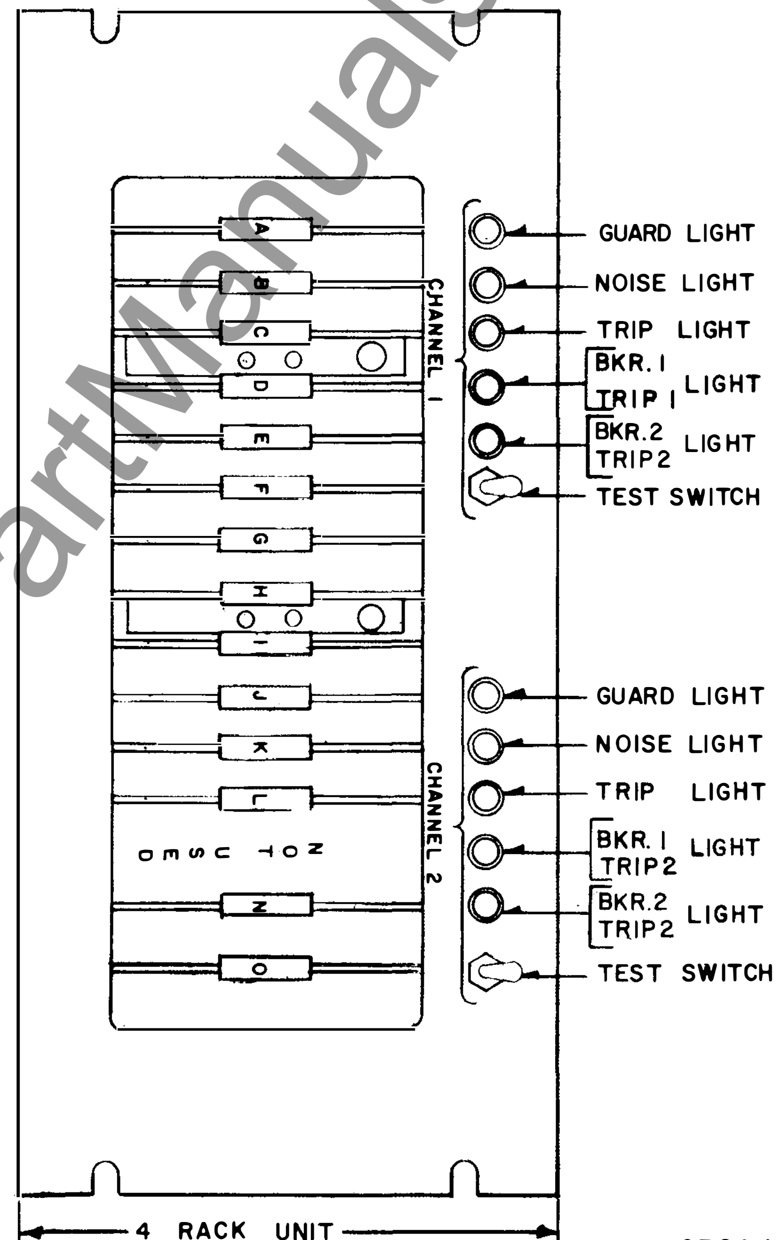


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Fig. 1. Front View of STU–92 Relay

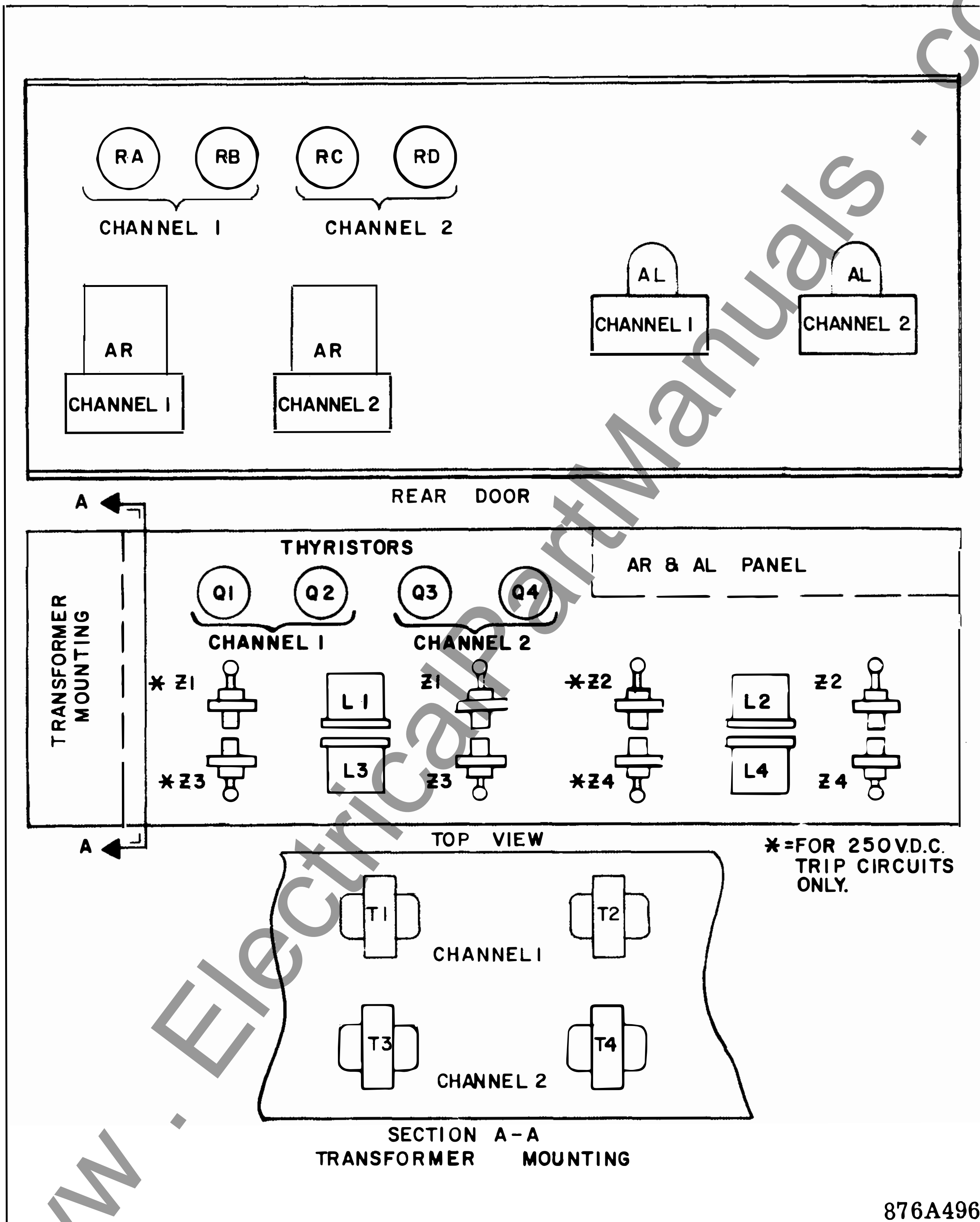


Fig. 2. Conponent Location in the STU–92 Relay

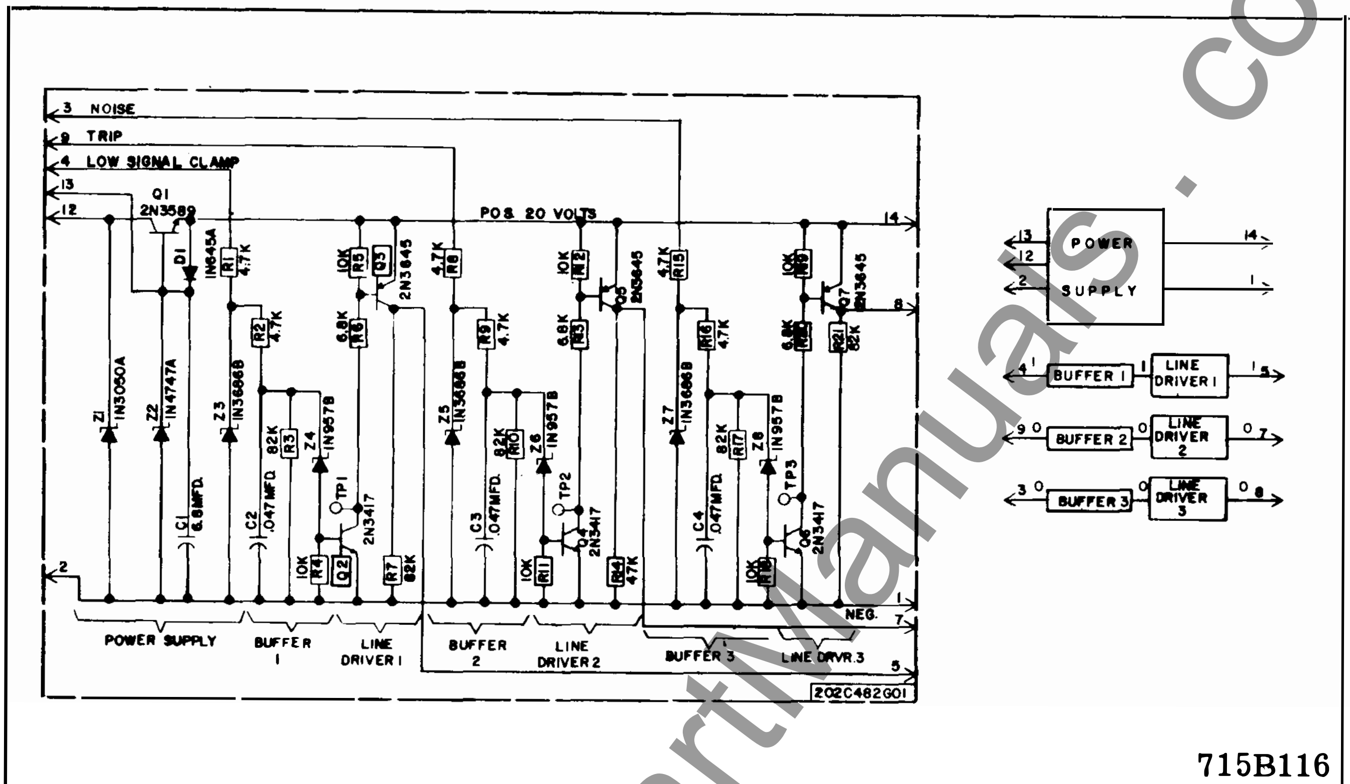


Fig. 3. Schematic Diagram of the Channel Interface Board for TA-3 Tone Channel and TCF Carrier

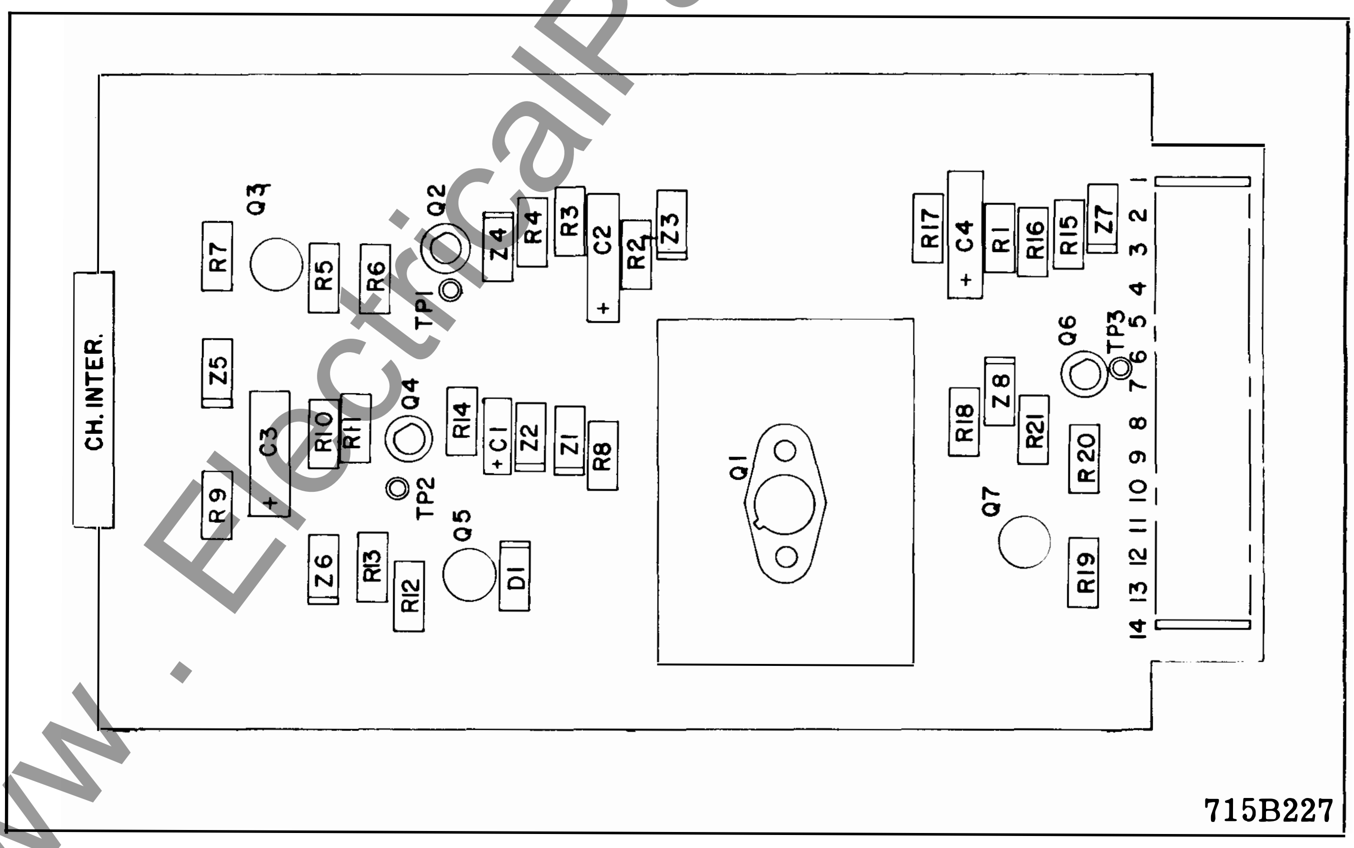


Fig. 4. Component Location on the Channel Interface Board for TA-3 Tone Channel and TCF Carrier

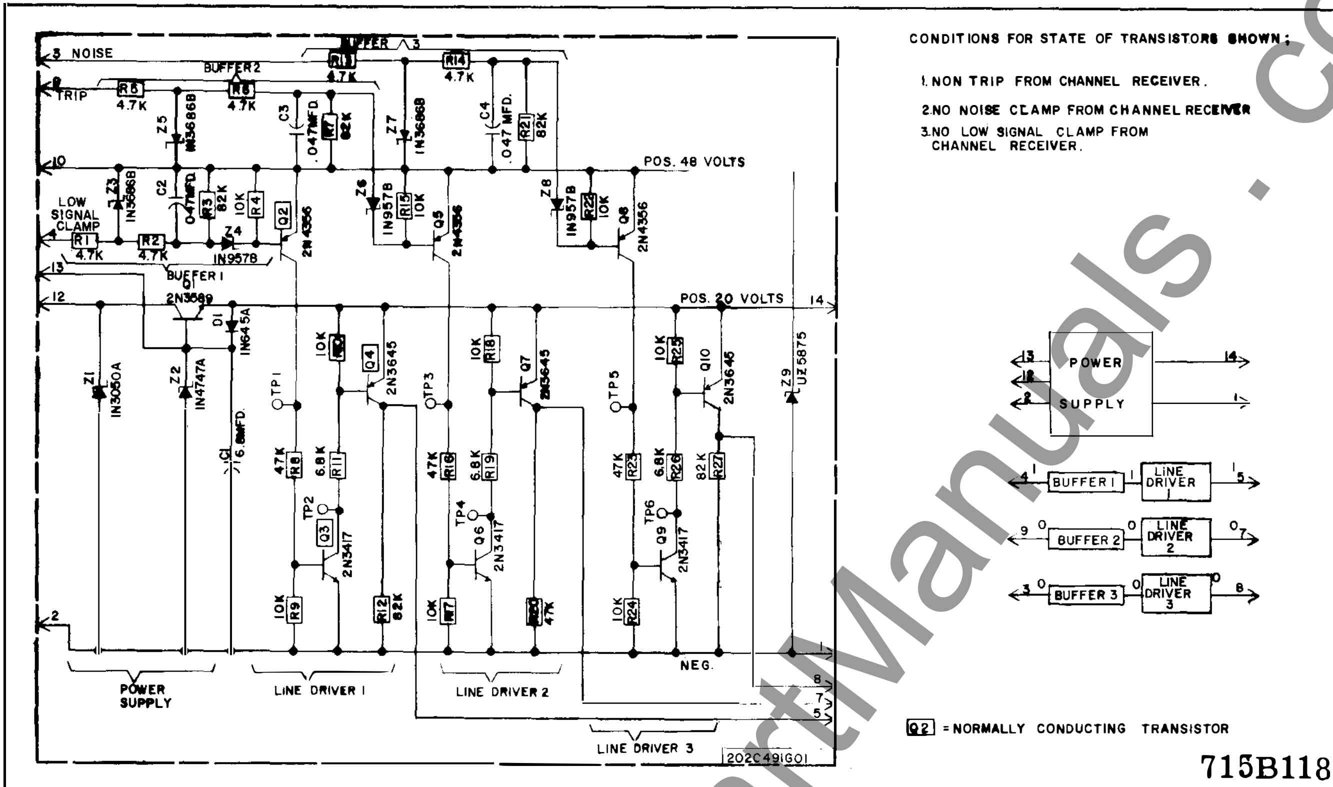


Fig. 5. Schematic Diagram of the Channel Interface Board for Lenkurt 937A Tone Channel

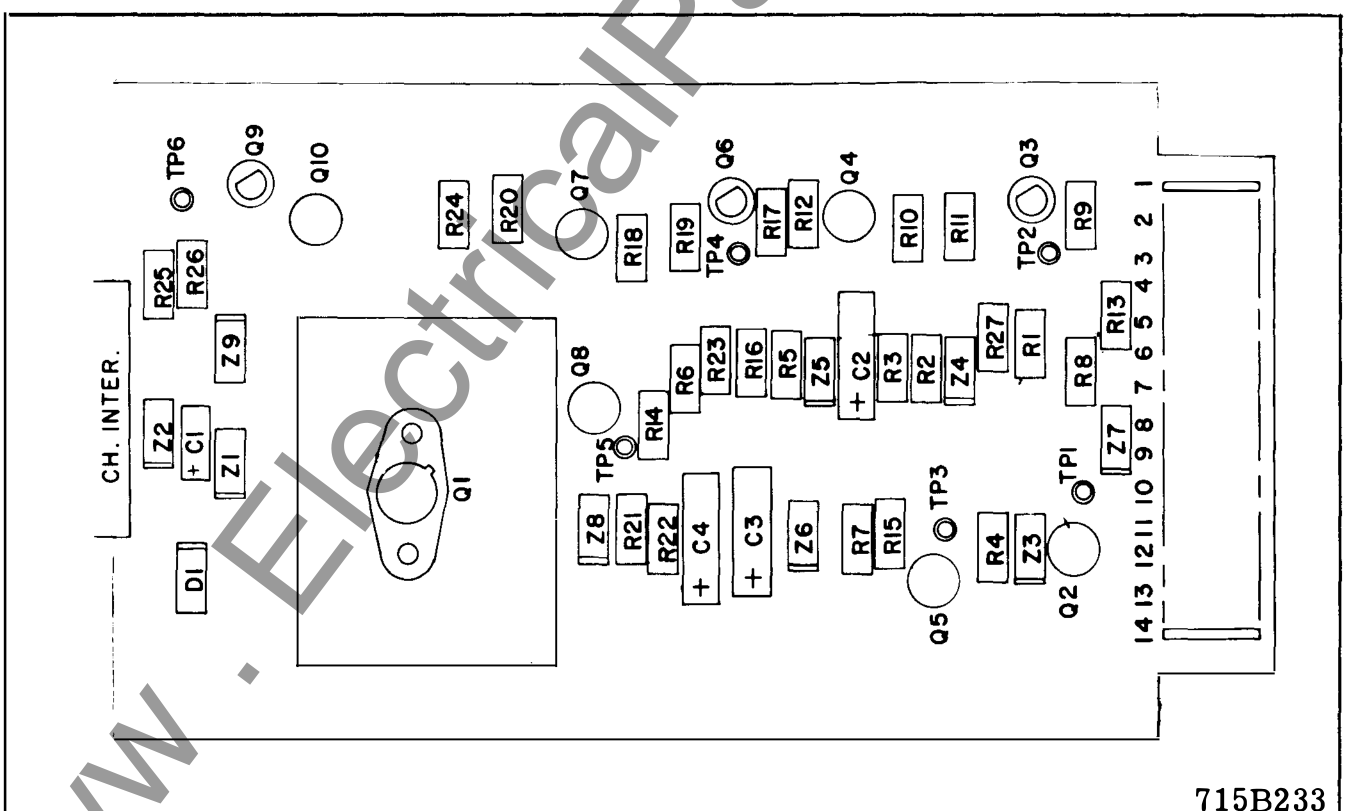


Fig. 6. Component Location on the Channel Interface Board for Lenkurt 937A Tone Channel

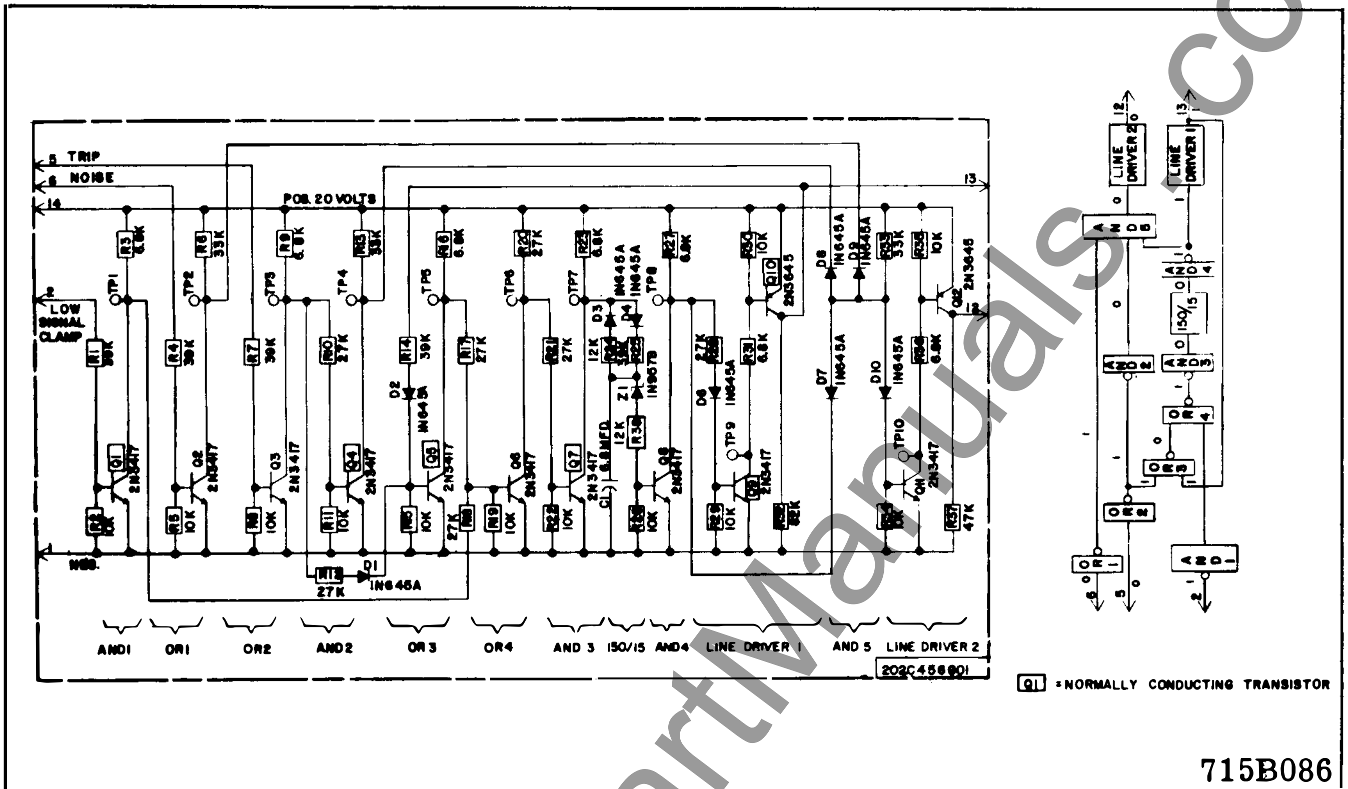


Fig. 7. Schematic Diagram of the Lockout Board for TA-3 and 937A Tone Channel

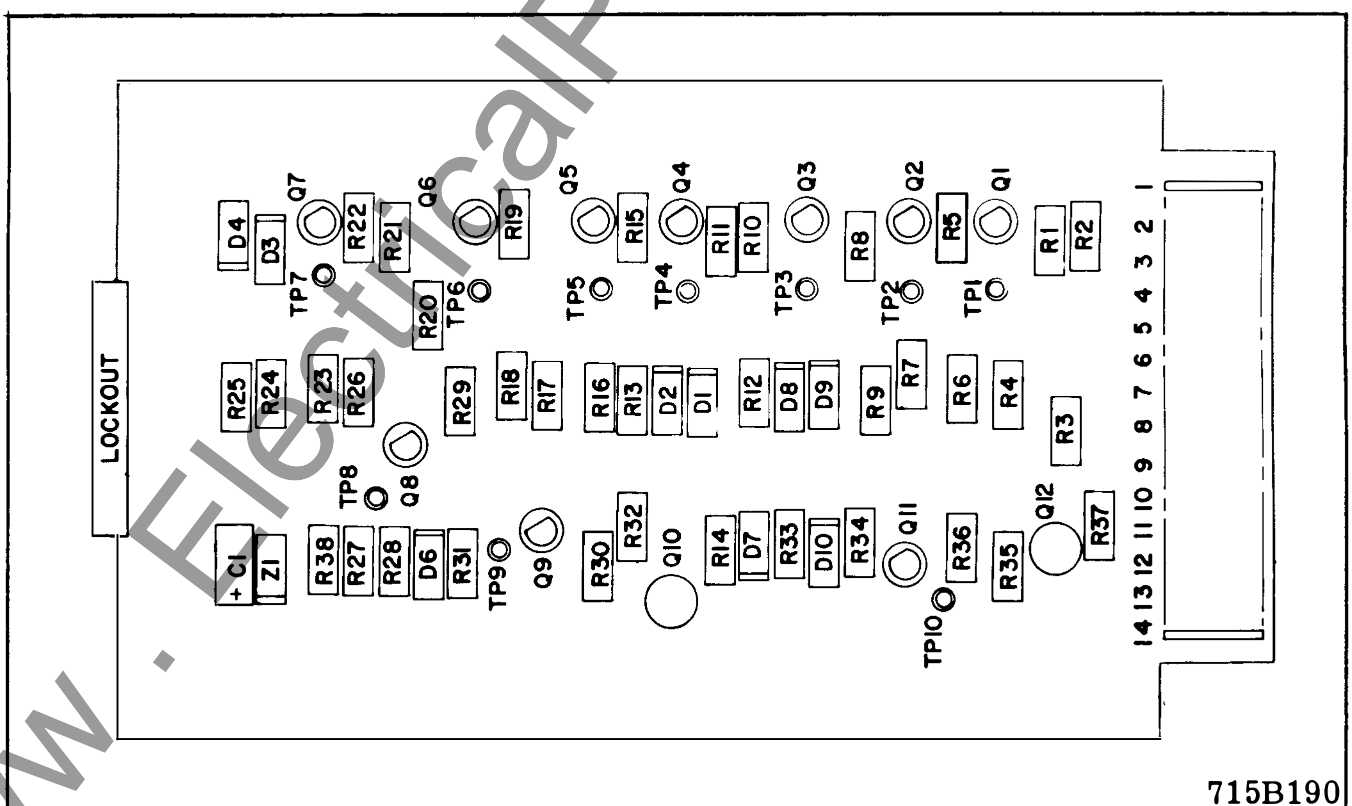


Fig. 8. Component Location on the Lockout Board of the STU–92 Relay for TA-3 and 937A Tone Channels

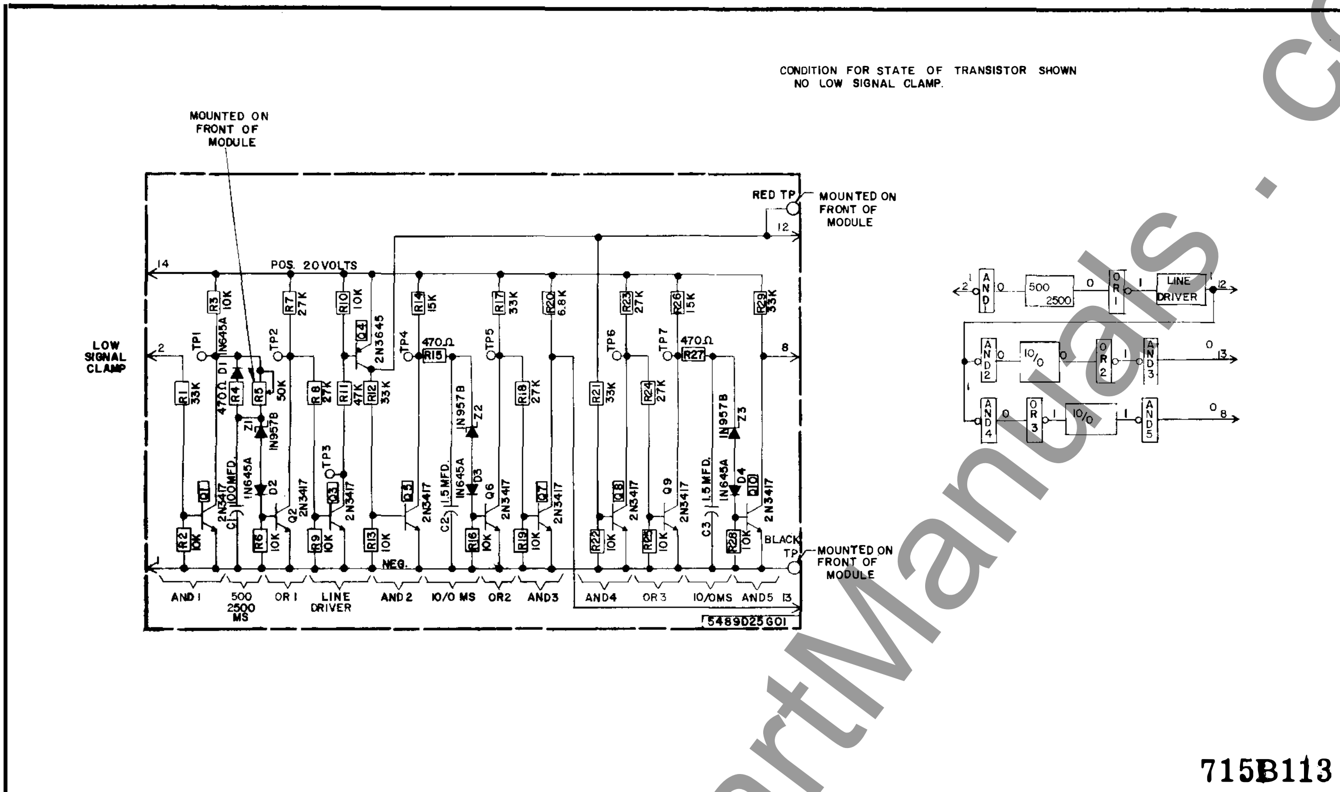


Fig. 9. Schematic Diagram of the Transfer Board of the STU-92 Relay

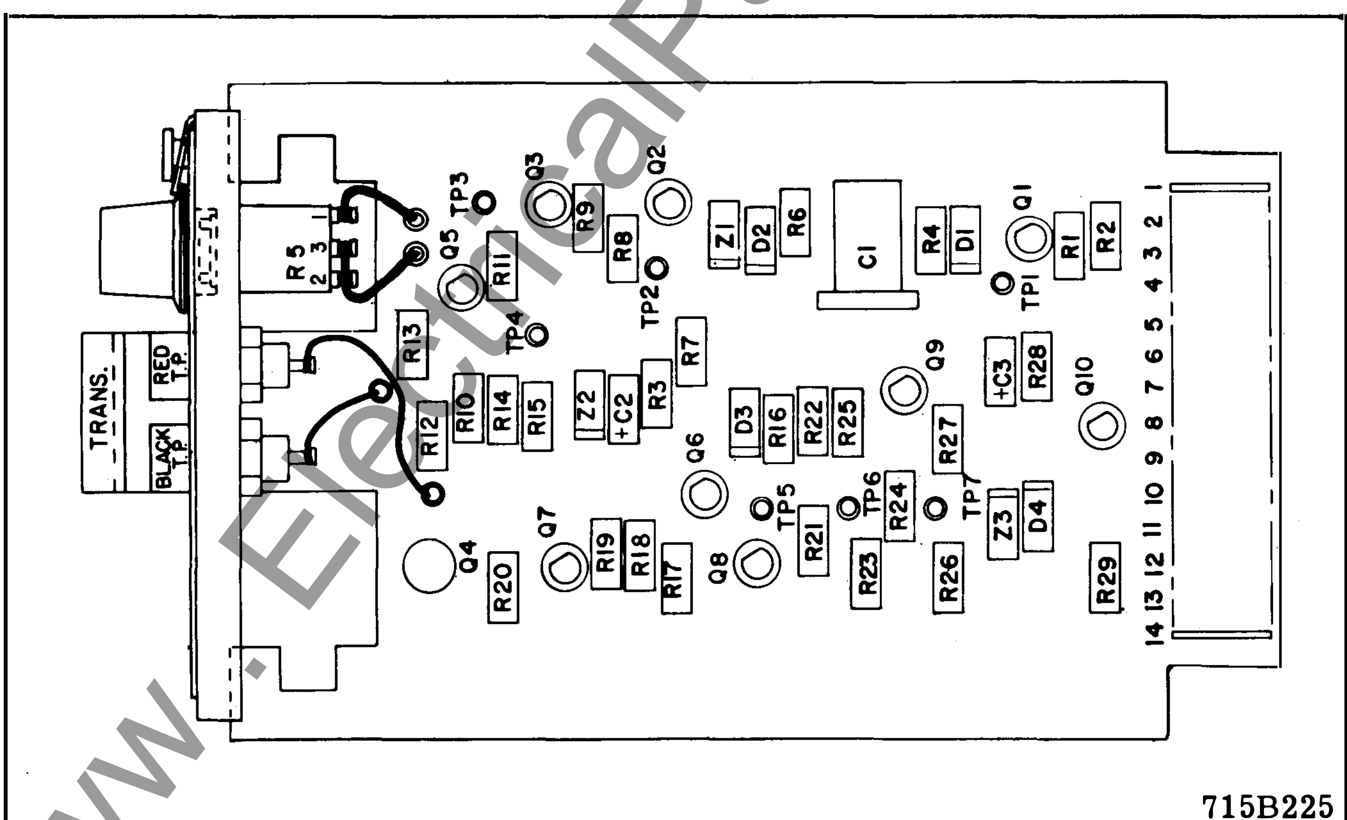


Fig. 10. Component Location on the Transfer Board

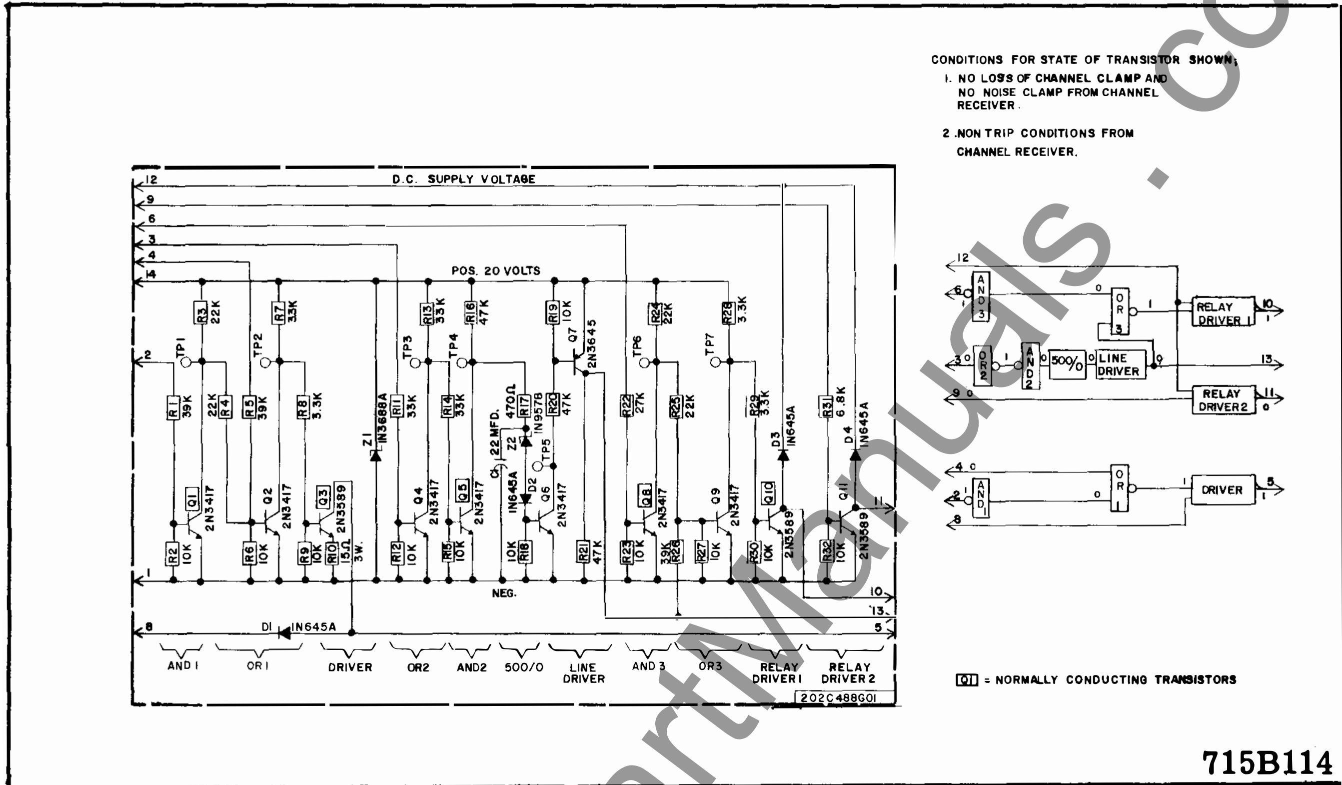


Fig. 11. Schematic Diagram of the Relay Driver Board

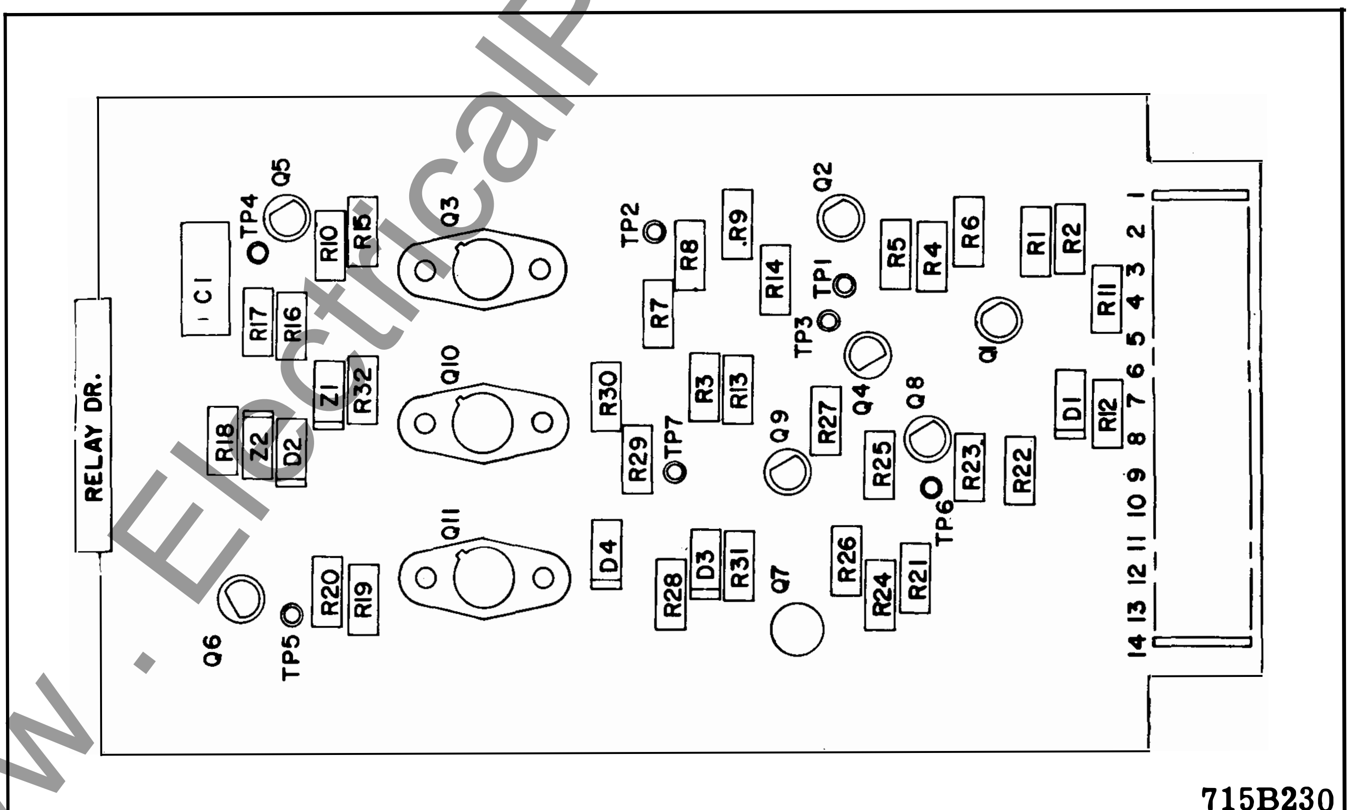


Fig. 12. Component Location on the Relay Driver Board

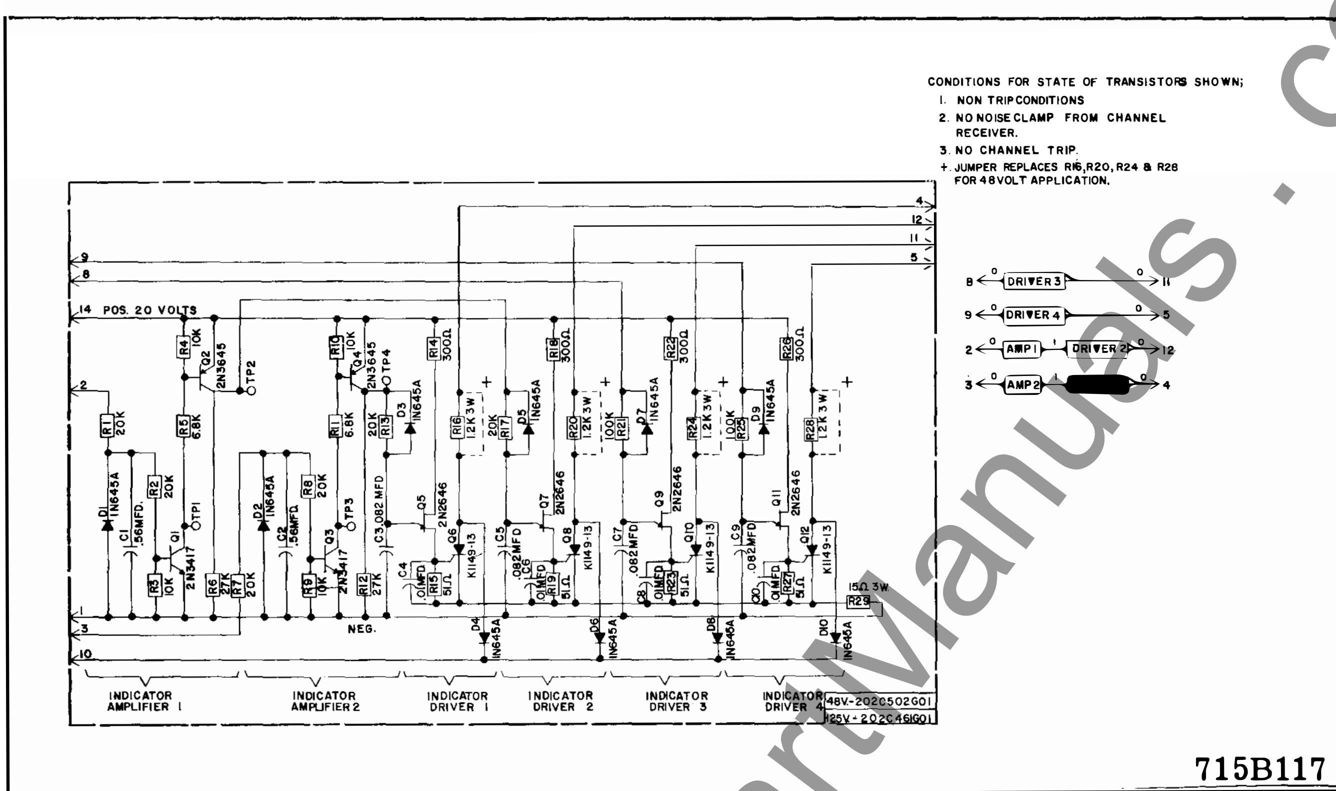


Fig. 13. Schematic Diagram of the Indicator Board

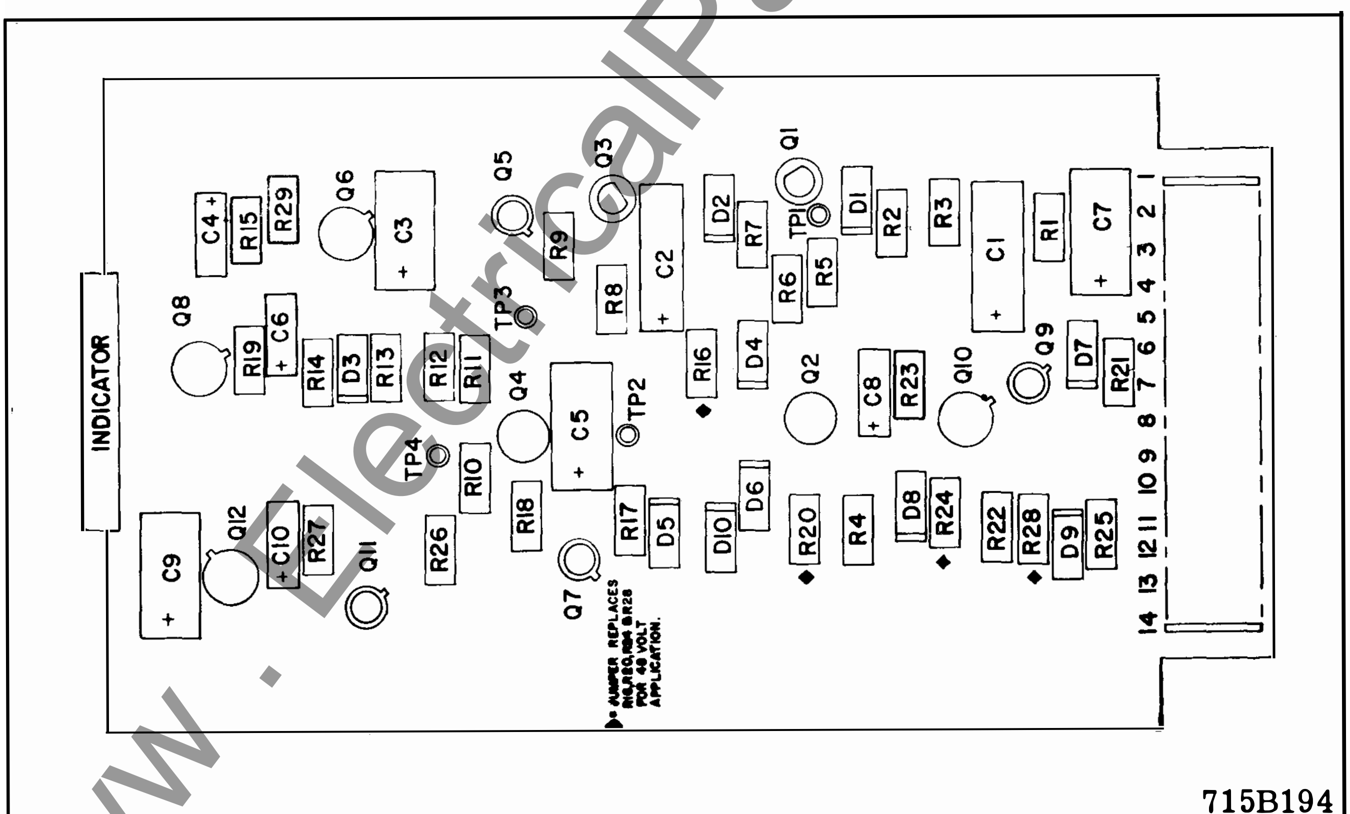


Fig. 14. Component Location on the Indicator Board

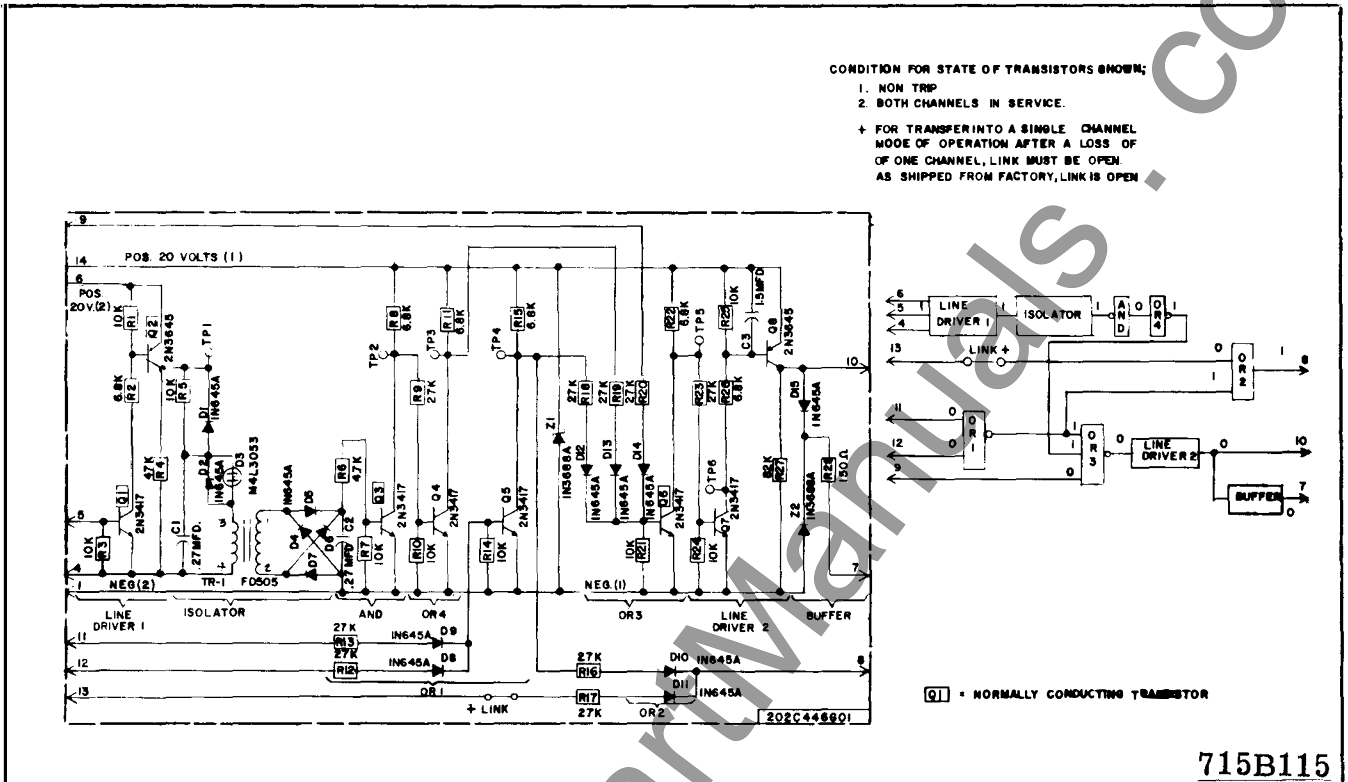


Fig. 15 Schematic Diagram of the OR Board of the STU–92 Relay

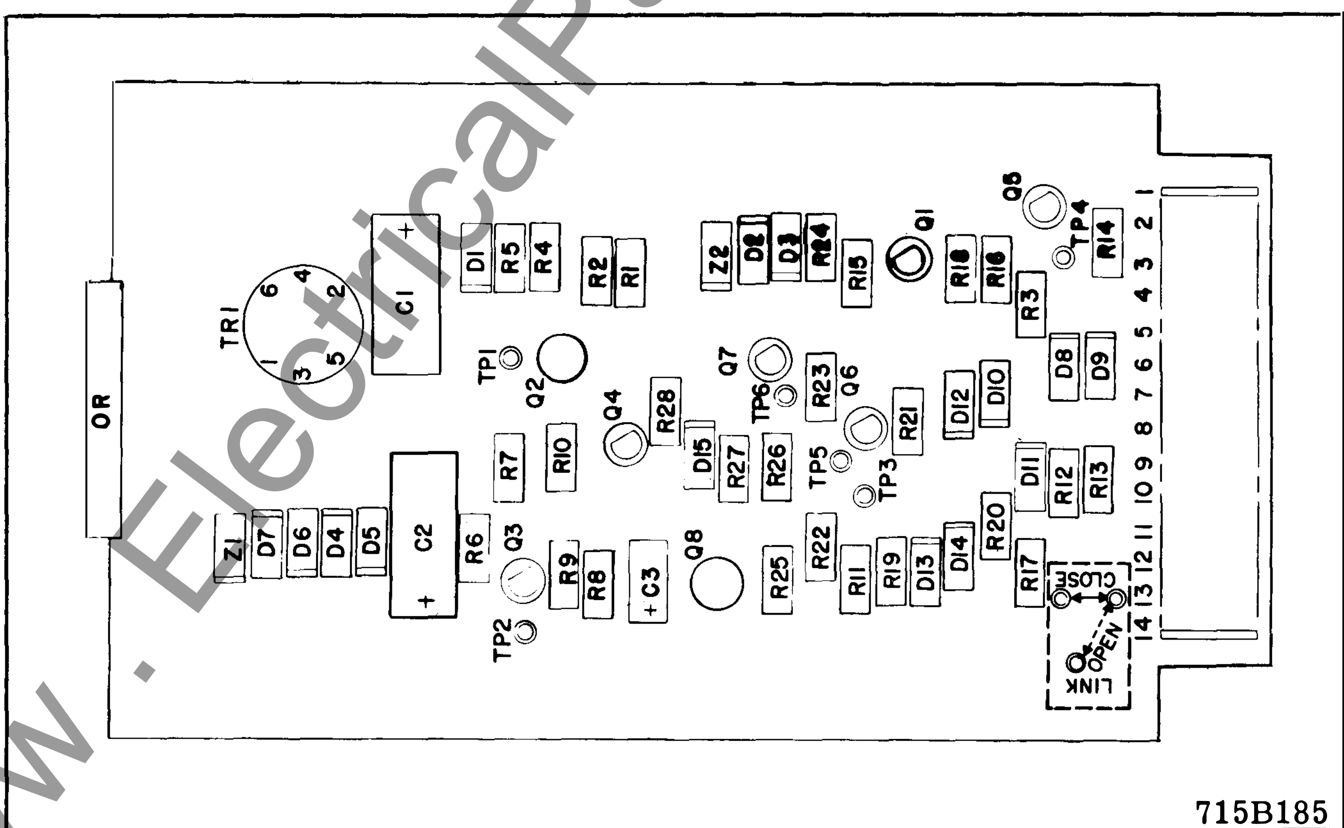


Fig. 16. Component Location on the OR Board of the STU–92 Relay

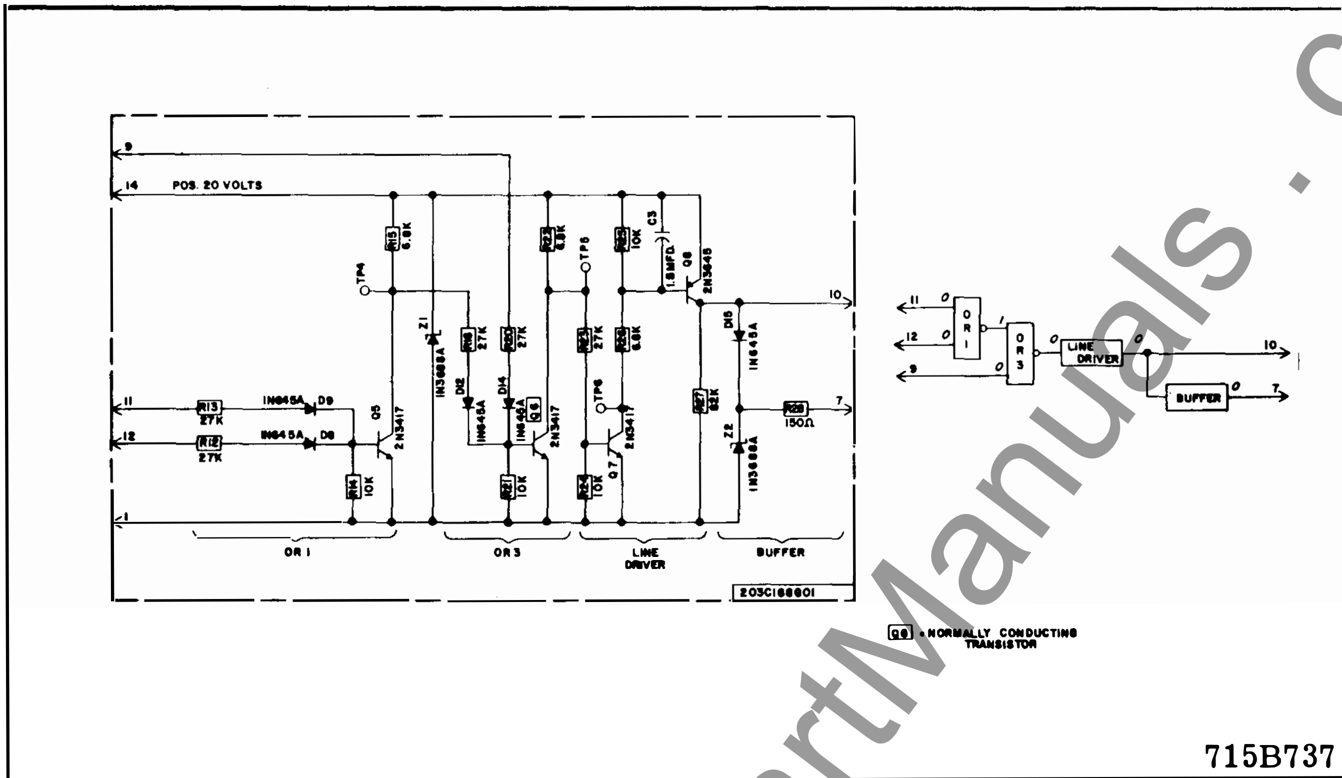


Fig. 17. Schematic Diagram of the OR Board of the STU–91 Relay

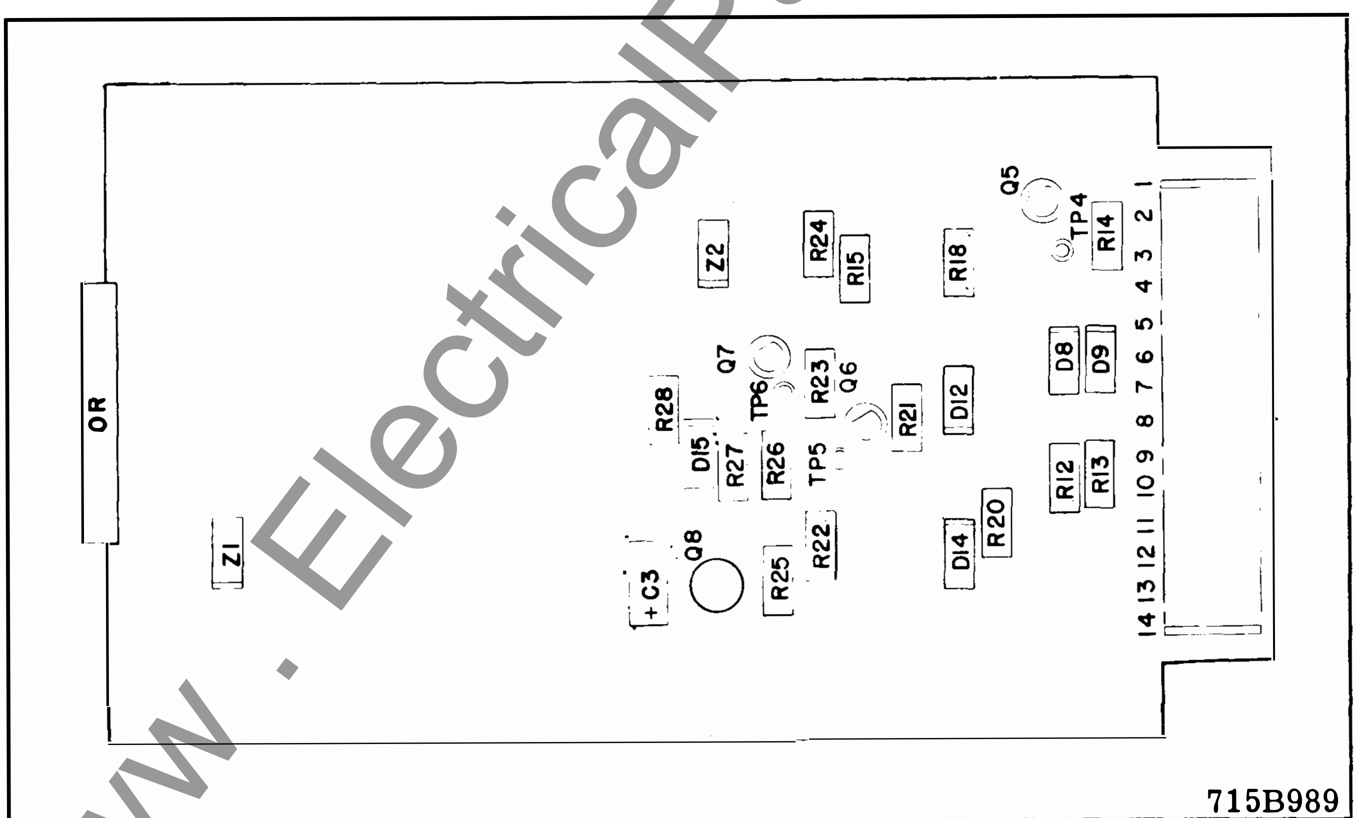
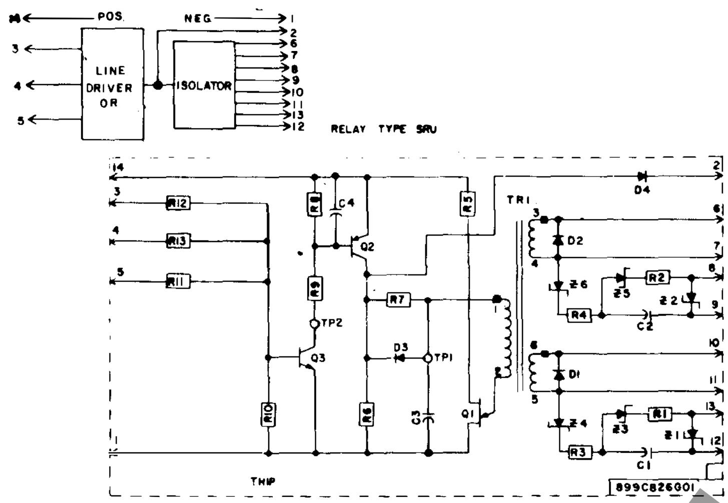


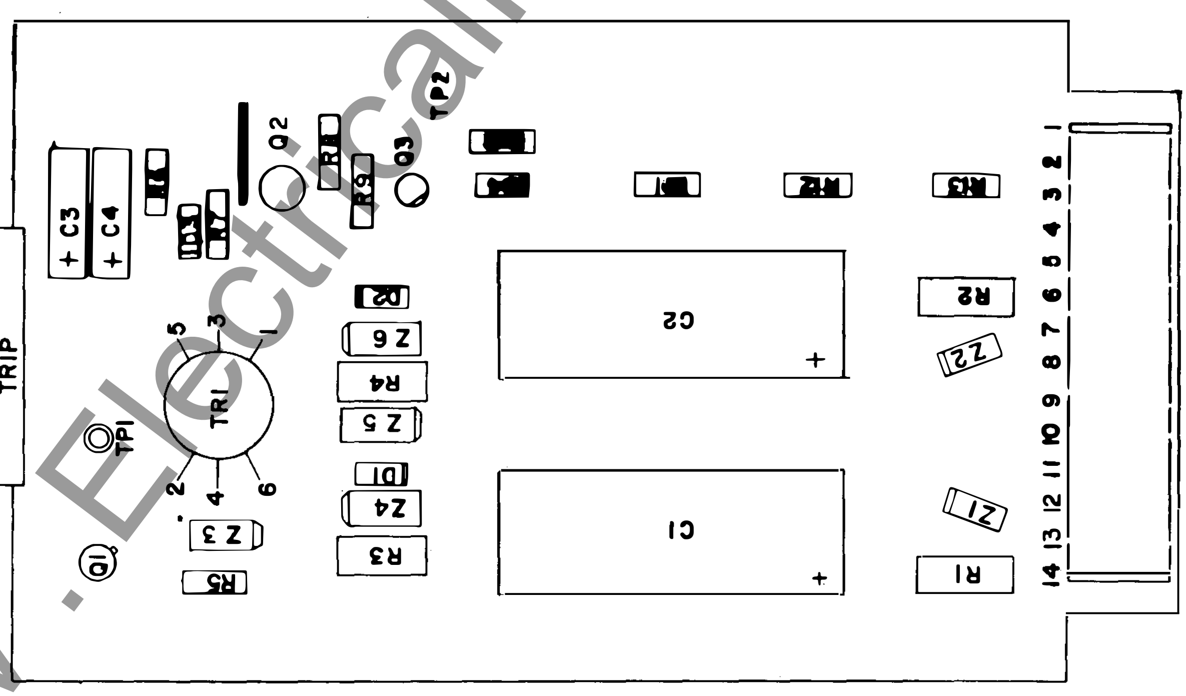
Fig. 18. Component Location on the OR Board of the STU–91 Relay



CAPACITOR	STYLE	REQ.	REF.	
C1 C2	187A624H05	2	2 MFD.	
C3 C4	188A669H05	2	27 MFD	
DIODE				
D1 TO D4	837A692H03	4	IN645A	
RESISTOR *				
R1 TO R4	187A643H19	4	470Ω-1W ±5%	
R5	629A531H19	1	300Ω	
R6	629A531H60	1	15K	
R7	629A531H44	1	3.3K	
R9	629A531H52	1	6.8K	
R10- R8	629A531H56	2	10K	
R11 TO R13	629A531H66	3	27K	
TRANSFORMER				
TR1	629A372H01	1	FD505	
TRANSISTOR				
Q1	629A435H02	1	40X5F695	
Q2	849A441H01	1	2N3645	
Q3	848A851H02	1	2N3417	
ZENER DIODE				
Z1 TO Z6	629A369H01	6	1R200	

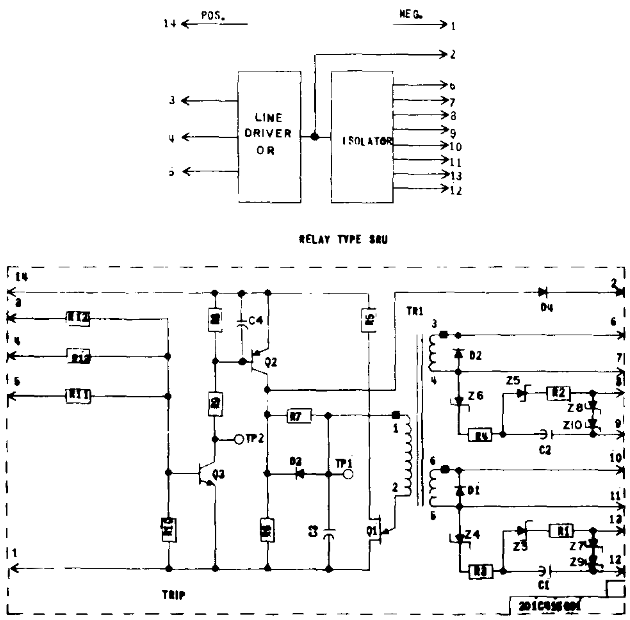
671B903

Fig. 19. Schematic of the Trip Board for 48/125 Volt DC Operation



715B246

Fig. 20. Component Location on the Trip Board for 48/125 Volt DC Operation

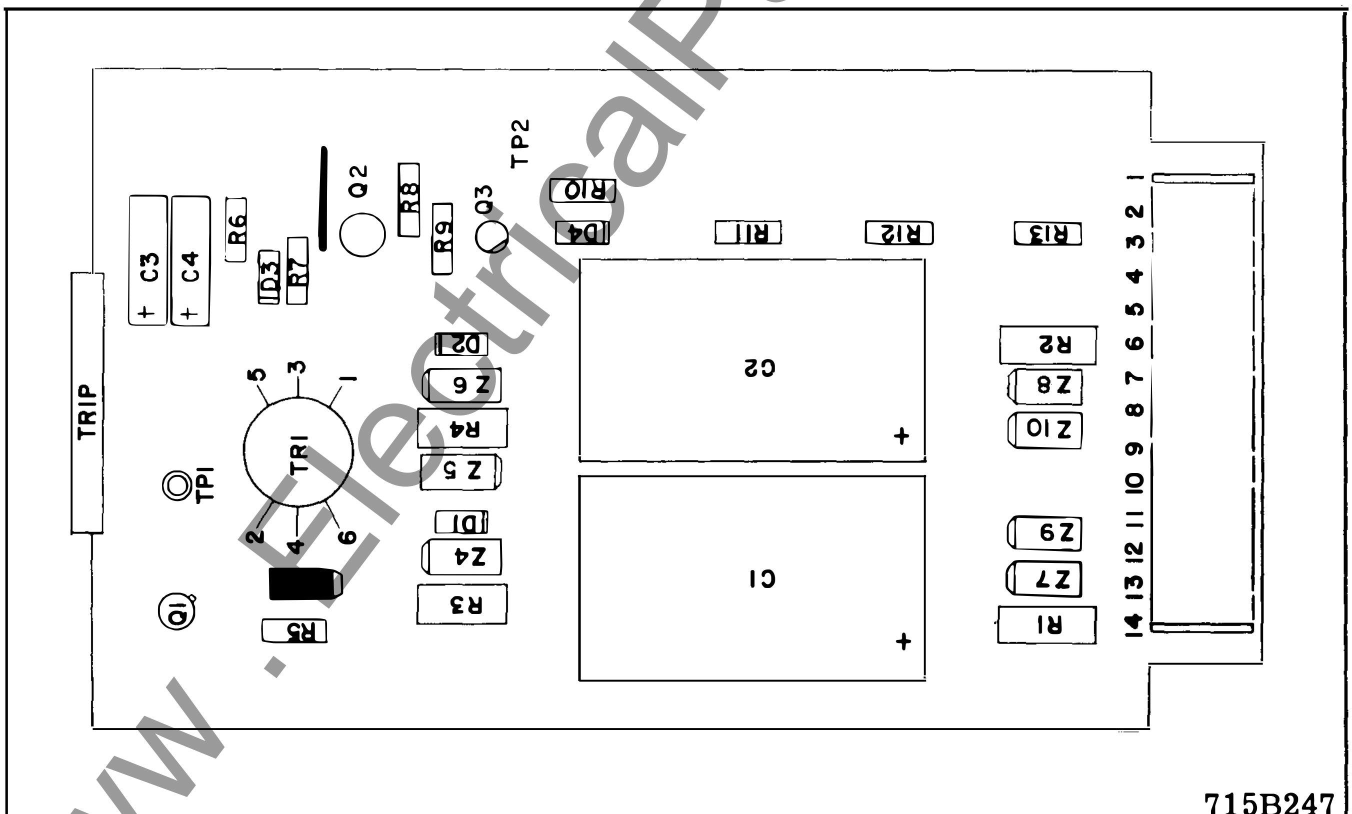


CAPACITOR	STYLE	REQ.	REF.
C1 - C2	188A669H07	2	1.0 MFD
C3 C4	188A669H05	2	.27 MFD
DIODE			
D1 TO D4	837A692H03	4	1N645A
RESISTOR *			
R1 - R2	187A643H27	2	1K-1W ±5%
R5	629A531H19	1	300 Ω
R6	629A531H60	1	15K
R7	629A531H44	1	3.3K
R9	629A531H52	1	6.8K
R10 - R8	629A531H56	2	10K
R11 TO R12	629A531H66	2	27K
R3 - R4	187A643H19	2	470 Ω-1W ±5%
TRANSFORMER			
TR1	629A372H01	1	[illegible]
TRANSISTOR			
Q1	629A435H02	1	4JX5E696
Q2	849A441H01	1	[illegible]
Q3	848A851H02	1	[illegible]
ZENER DIODE			
Z3 TO Z10	[illegible]	8	[illegible]

* = ALL RESISTORS TO BE 1/2 WATT ± 2% UNLESS OTHERWISE SPECIFIED.

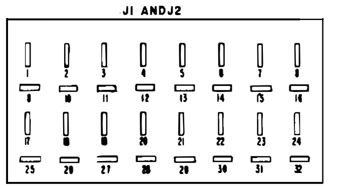
691B406

Fig. 21. Schematic of the Trip Board for 250 Volt DC Operation



715B247

Fig. 22. Component Location on the Trip Board for 250 Volt DC Operation



VARICON CONNECTOR AS VIEWED FROM REAR OF RELAY.

POWER SUPPLY RESISTORS			
	RA —— RC	RB —— RD	
48 VDC	S — 1267272 150 OHMS	S — 1201804 1.8 K	
125 VDC	S — 1267287 800 OHMS	S — 1205214 5 K	

AR RELAYS		
VOLT	4 - 8	24 – 28
125 VOLT — 2W	408C045608	408C045626
48 VOLT — 2W	671B472609	671B472611

TELEPHONE RELAYS		
AL	125 VOLT	541D514H13
	48 VOLT	541D514H11

DESCRIPTION	STYLE	LOCATION
THYRISTORS (SCR)	184A614H05	Q1 – Q2 – Q3 – Q4
PULSE TRANSFORMER	6100392G02	T1 – T2 – T3 – T4
48V LAMP	[illegible]	ALL LAMPS
125V LAMP	[illegible]	ALL LAMPS
MUTUAL REACTOR	[illegible]	L1–L2–L3–L4
ZENER DIODE 1N3350A	182A851H05	Z1-Z2-Z3-Z4

TRIP BOARD SCHEMATIC	
48/125 VDC	671B803
250 VDC	681B406

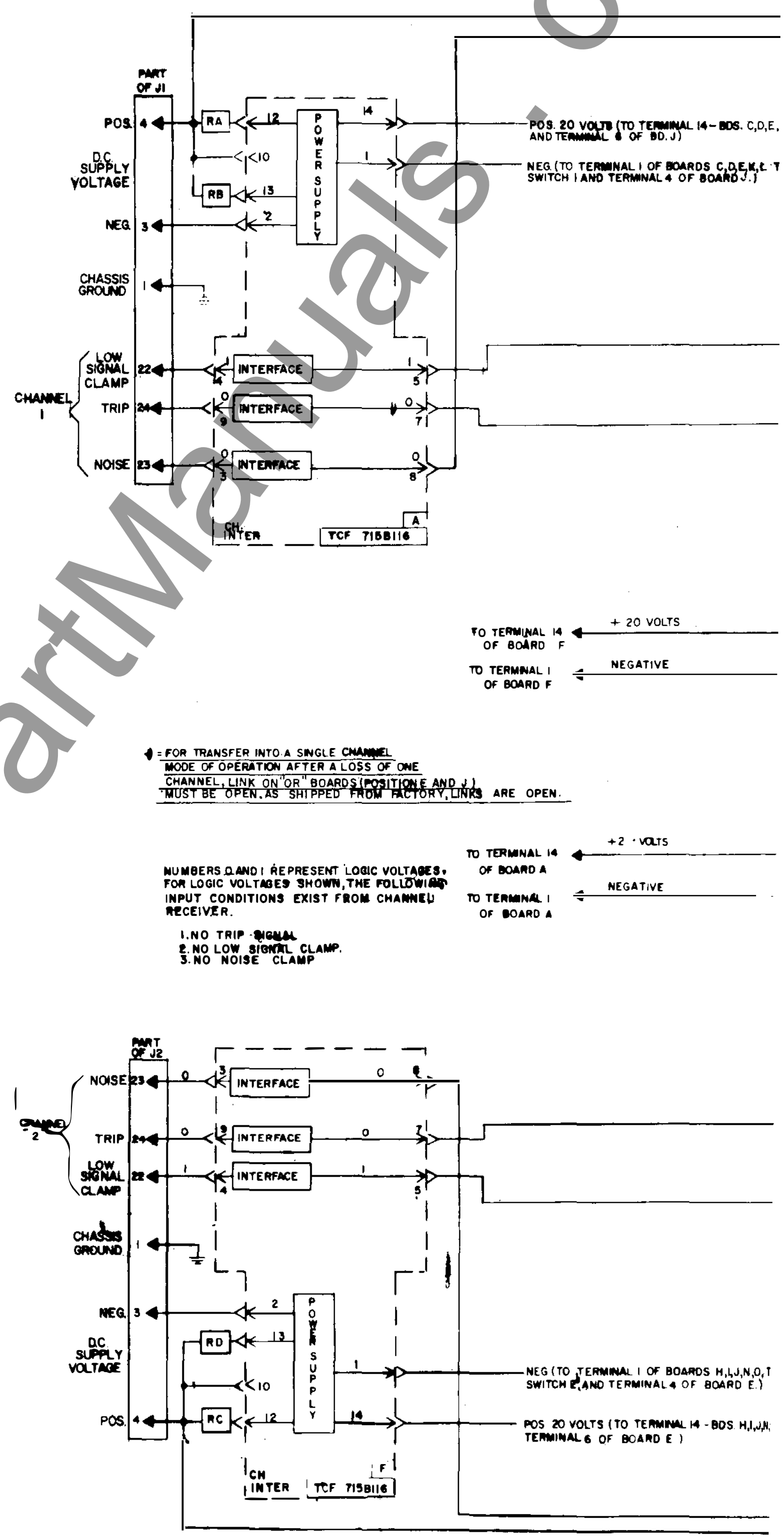
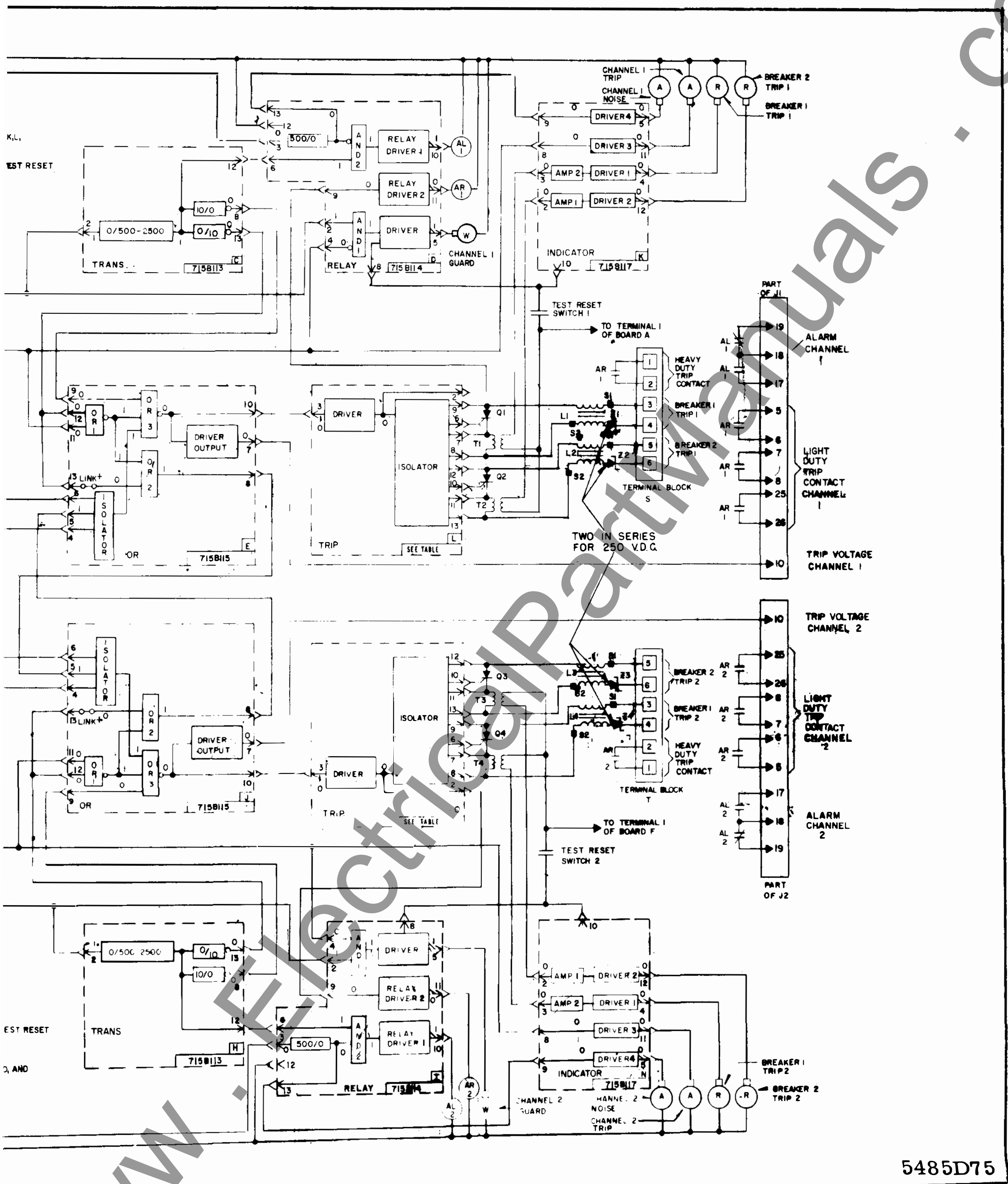
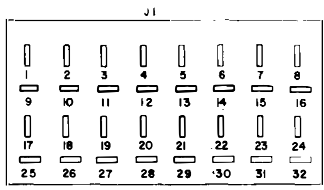


Fig. 24. Logic Diagram of the ST



U-92 Relay for Dual TCF Carrier Channel



CONNECTOR AS VIEWED FROM REAR OF RELAY.

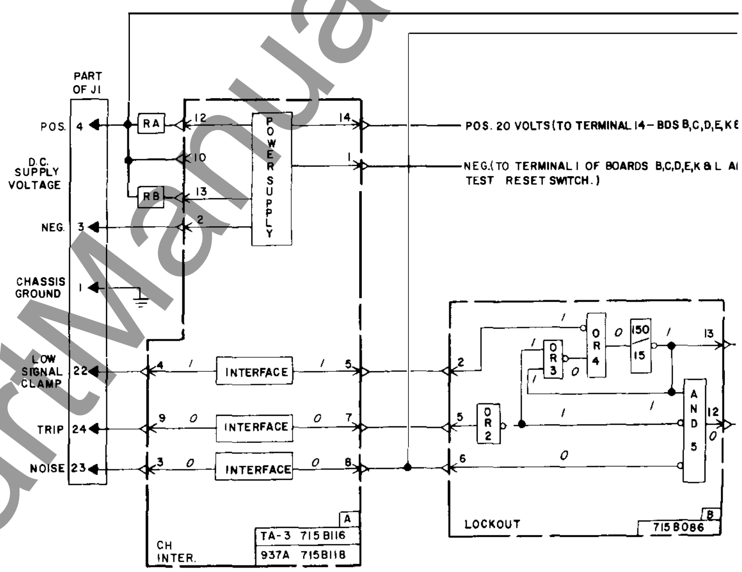
POWER SUPPLY RESISTOR			
	RA	RB	
48VDC	S- 1267272 150 OHMS	S-1201004 1.8K OHMS	
125VDC	S-1267287 900 OHMS	S-1205214 5K OHMS	

AR RELAY		
VOLT	4-M	2M-2B
125VOLT-2W	408C845G08	408C845G26
48 VOLT-2W	871B472G09	671B472G11

TELEPHONE RELAY		
AL	125 VOLT	541D514H13
	48 VOLT	541D514H11

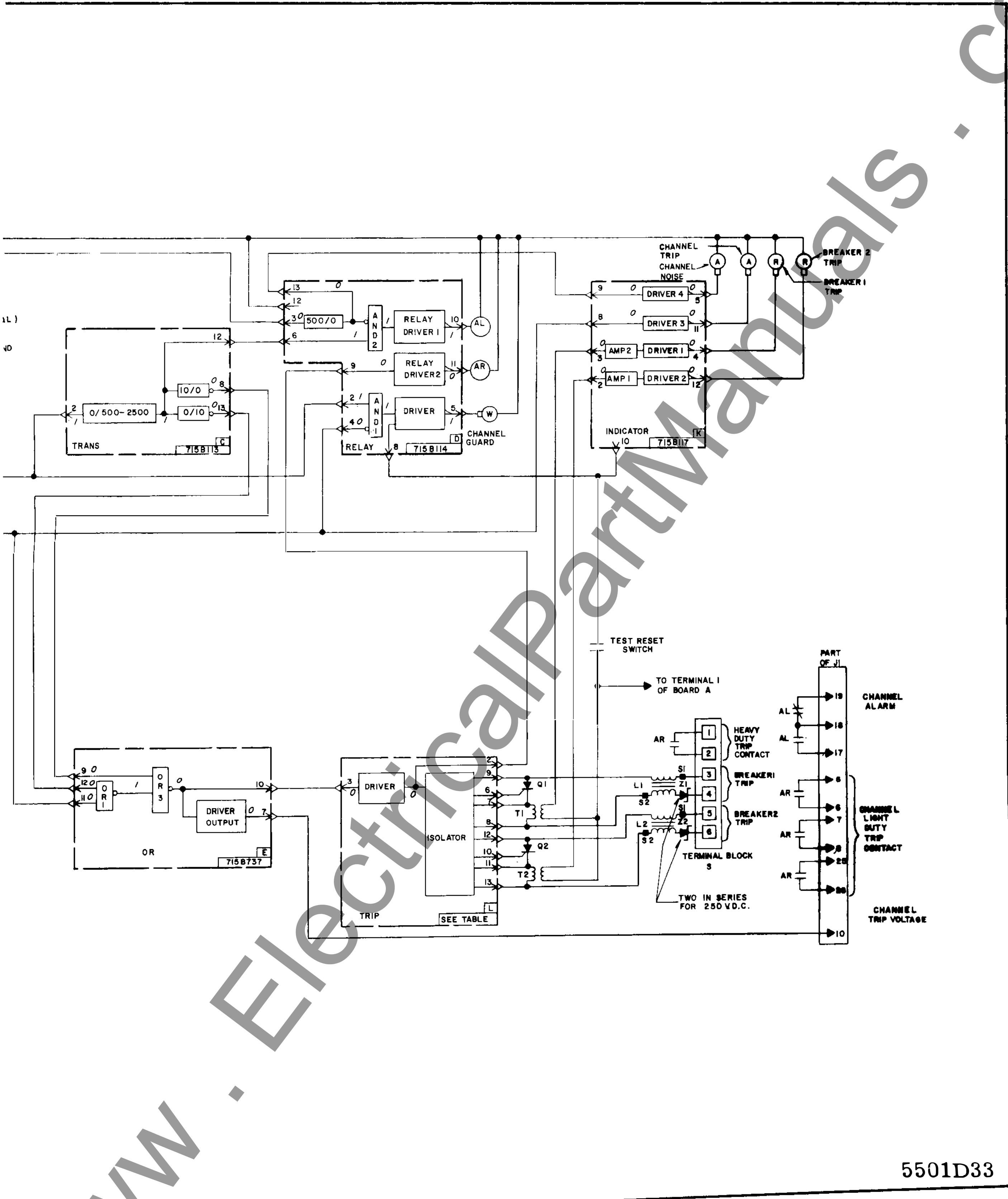
DESCRIPTION	STYLE	LOCATION
THYRISTORS (SCR)	184A614H05	Q1-Q2
PULSE TRANSFORMER	870B392G02	T1-T2
MUTUAL REACTORS	691B878G01	L1-L2
48V LAMP	837A832H02	ALL LAMPS
125V LAMP	837A832H07	ALL LAMPS
ZENER DIODE IN3350A	762A631H05	Z1-Z2

TRIP BOARD SCHEMATIC	
48/125VDC	671B903
250VDC	691B406



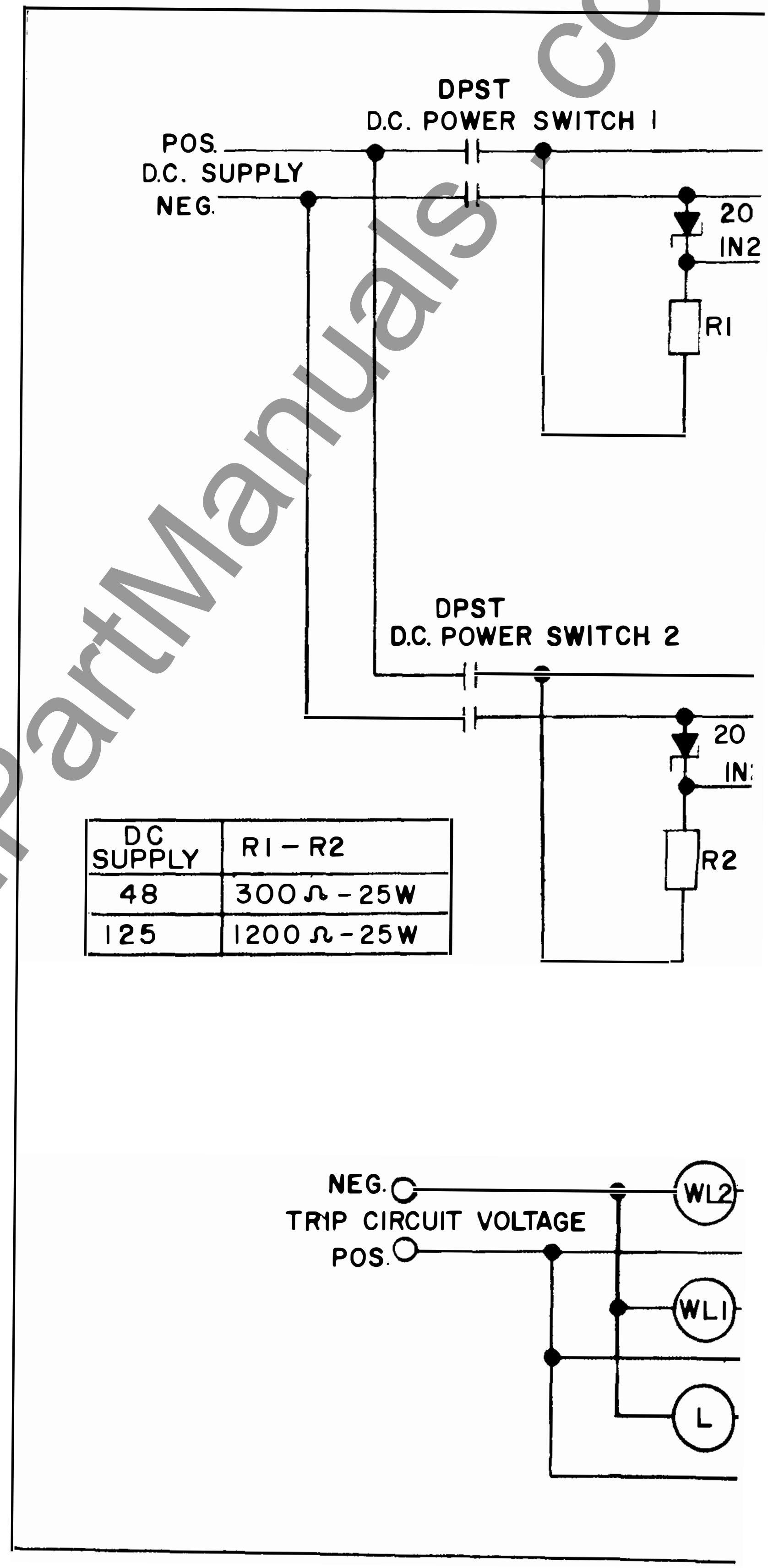
NUMBERS 1 AND 0 REPRESENT LOGIC VOLTAGES.
FOR LOGIC VOLTAGES SHOWN, THE FOLLOWING INPUT CONDITIONS EXIST FROM CHANNEL RECEIVER
1. NO TRIP SIGNAL
2. NO LOW SIGNAL CLAMP
3. NO NOISE CLAMP

Fig. 26. Logic Diagram of t



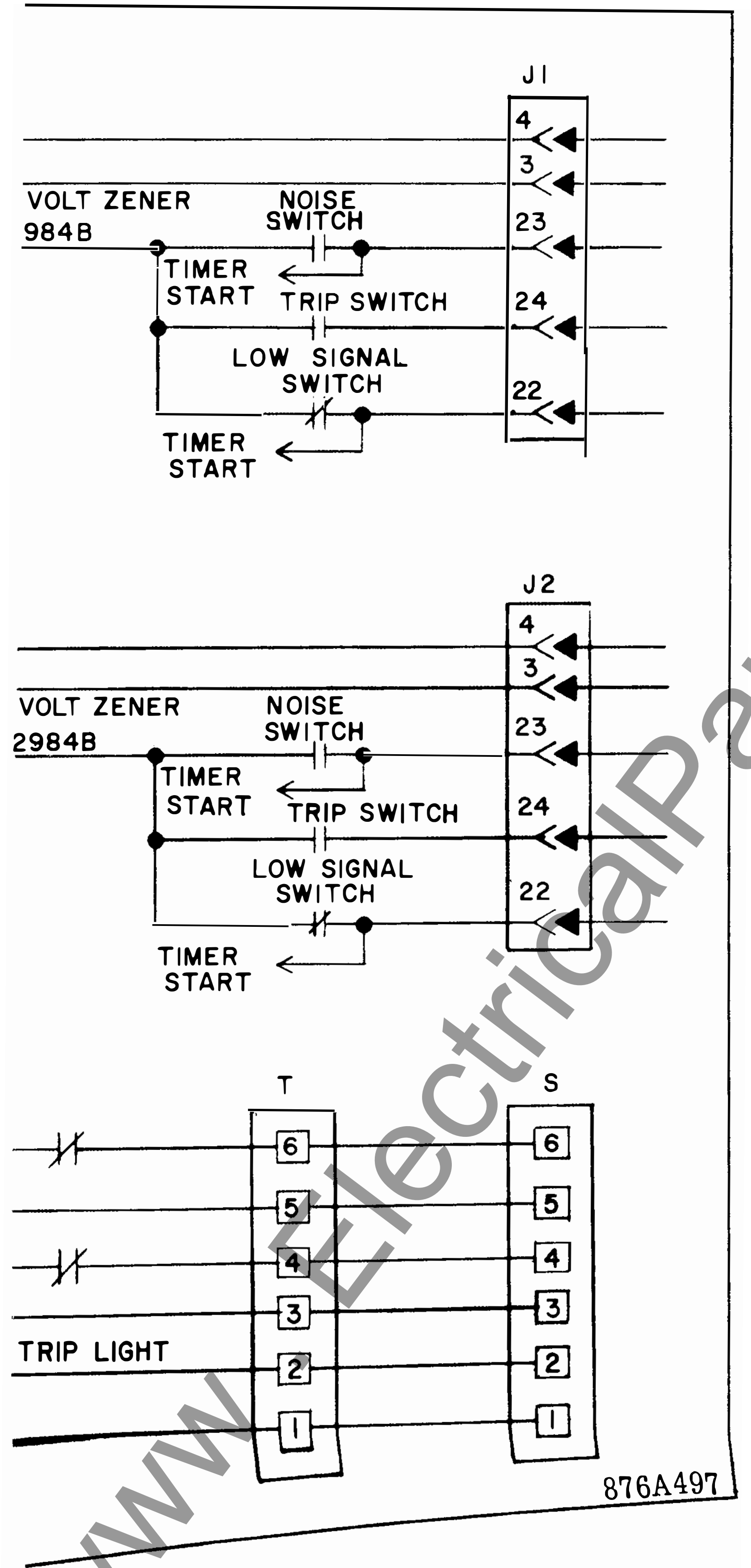
5501D33

the STU-91 Relay for a Tone Channel



DC SUPPLY	R1 – R2
48	300 Ω - 25W
125	1200 Ω - 25W

Fig. 28. Test Circui



t of STU-92 Relay

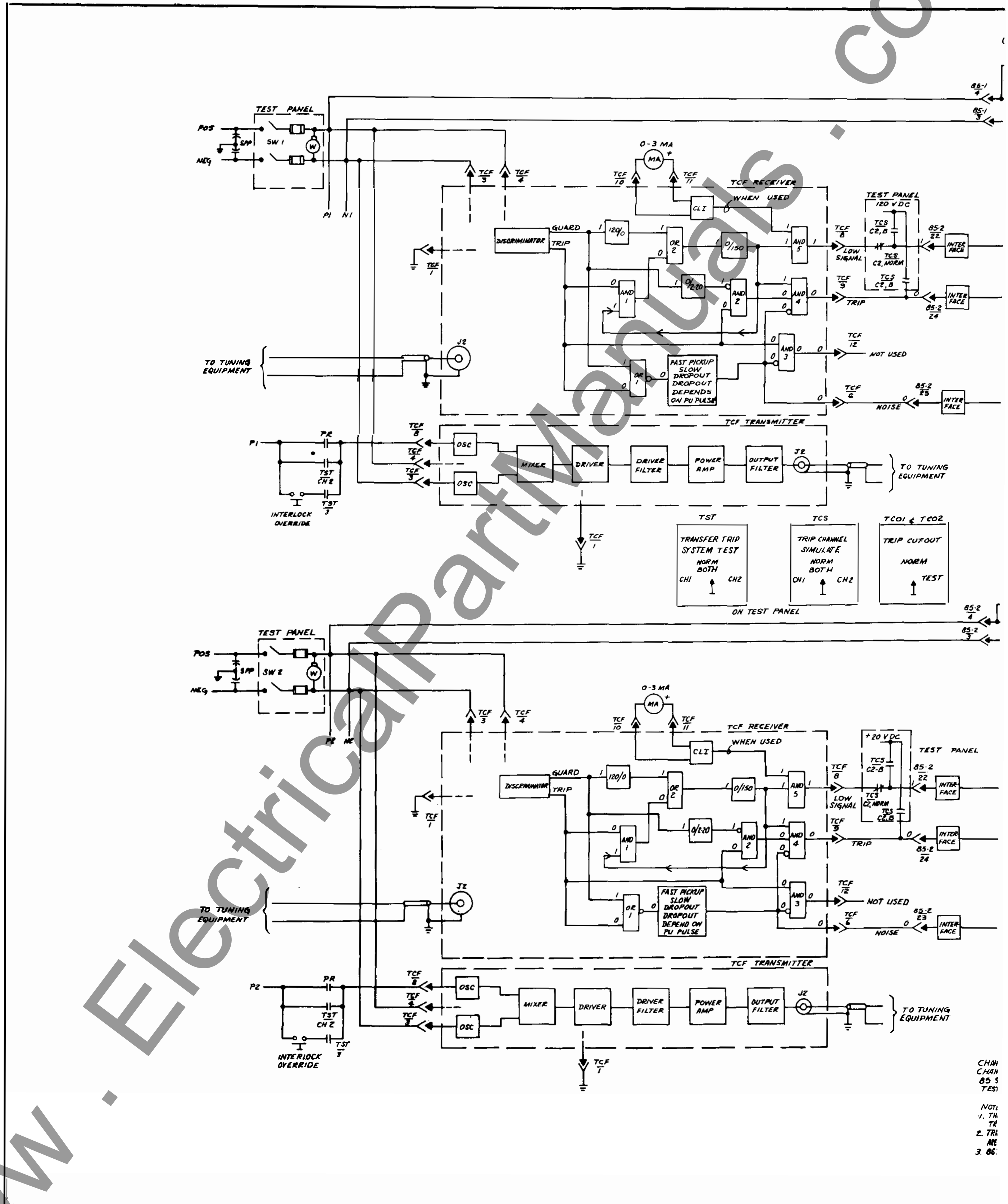
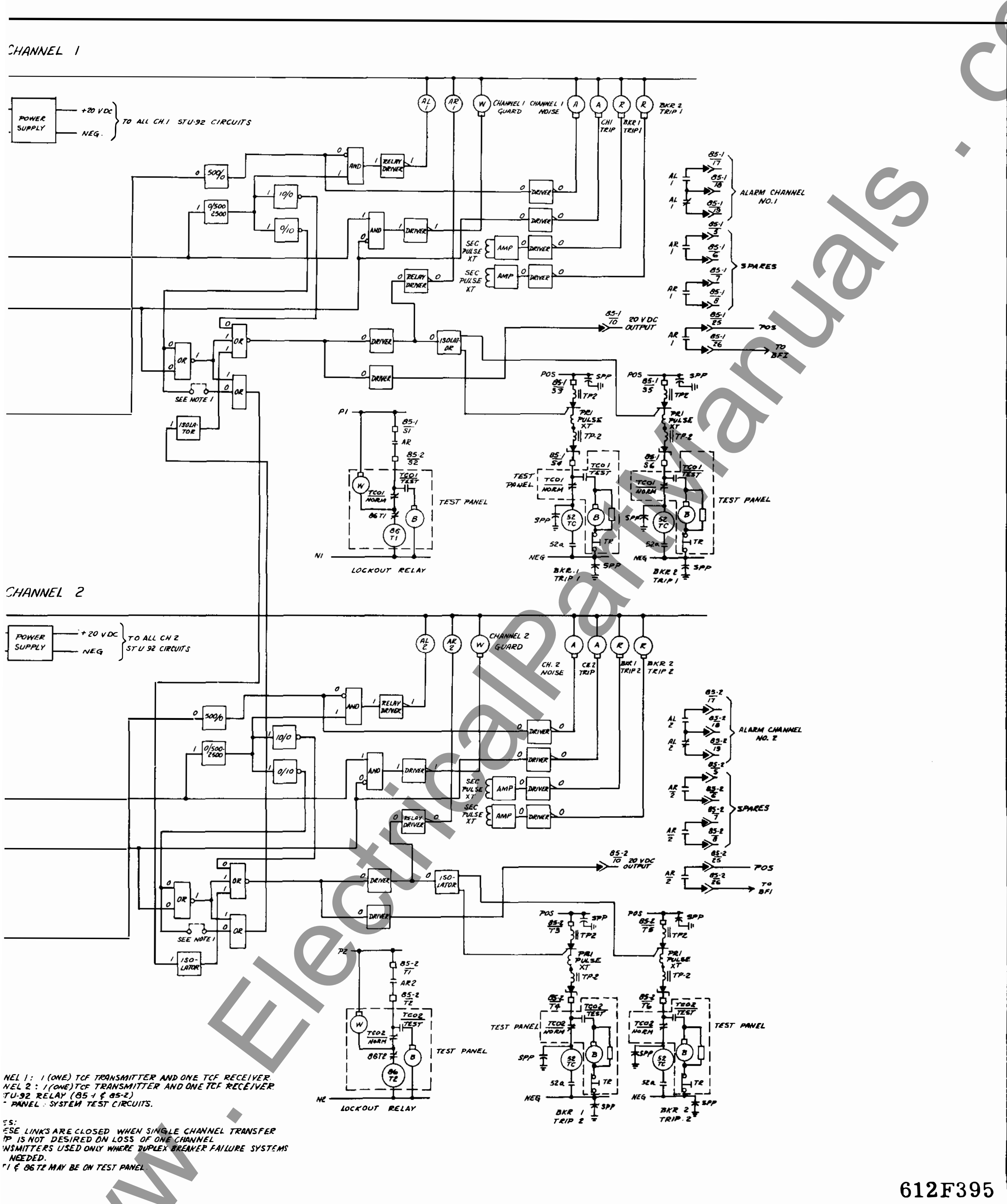


Fig. 30. Schematic Diagram of the STU–9



: Transfer Trip Scheme with TCF Power Line Carrier Channel

TRANSFER BOARD

CONDITION	AND-1 INPUT	AND-1 OUTPUT	500/2500 INPUT	500/2500 OUTPUT+	OR-1 INPUT+	OR-1 OUTPUT	LINE DRIVER 1 INPUT	LINE DRIVER 1 OUTPUT	AND-2 INPUT	AND-2 OUTPUT	10/0 INPUT	10/0 OUTPUT+	OR-2 INPUT+	OR-2 OUTPUT	AND-3 INPUT	AND-3 OUTPUT	AND-4 INPUT	AND-4 OUTPUT	OR-3 INPUT	OR-3 OUTPUT	10/0 INPUT	10/0 OUTPUT+	AND-5 INPUT+	AND-5 OUTPUT
NORMAL	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	0	1	0	0	1	1	1	1	0
LOSS OF CHANNEL	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0	1	1	0	0	0	0	1
VOLTS FOR 1 STATUS AT TP OR TERMINAL	20 TERM. 2	7 O TP 1	7 O TP 1	0.6 Q2	0.6 Q2	10 TP 2	10 TP 2	20 TERM. 12	20 TERM. 12	7 TP 4	7 TP 4	0.6 Q6	0.6 Q6	9 TP 5	9 TP 5	13.5 OO TERM. 13	20 TERM. 12	10 TP 8	10 TP 8	7 TP 7	7 TP 7	0.6 Q10	0.6 Q10	9 TERM. 8

+ = TEST POINTS NOT AVAILABLE. VOLTAGE MEASURED ON BASE OF TRANSISTOR SHOWN.
O = MEASURED ON MINIMUM SETTING.
OO = WITH LINK CLOSED.

RELAY DRIVER BOARD

CONDITION	AND-1 INPUT	AND-1 OUTPUT	OR-1 INPUT AND-1	OR-1 INPUT TERM.4	OR-1 OUTPUT	DRIVER INPUT	DRIVER OUTPUT O
NORMAL	1	0	0	0	1	1	1
TRIP	1	0	0	1	0	0	0
LOSS OF CHANNEL	0	1	1	0	0	0	0
NOISE	1	0	0	0	1	1	1
VOLTS FOR 1 STATUS AT TP OR TERMINAL	20 TERM. 2	10 TP 1	10 TP 1	20 TERM. 4	10 TP 2	10 TP 2	-48 TERM. 5

O = MEASURED WITH REFERENCE TO TERMINAL I
+ = TEST POINTS NOT AVAILABLE. VOLTAGE MEAS

CHANNEL INTERFACE BOARD

CONDITION	O BUFFER 1 INPUT	O BUFFER 1 OUTPUT+	LINE DRIVER 1 INPUT+	LINE DRIVER 1 OUTPUT	O BUFFER 2 INPUT	O BUFFER 2 OUTPUT+	LINE DRIVER 2 INPUT+	LINE DRIVER 2 OUTPUT	O BUFFER 3 INPUT	O BUFFER 3 OUTPUT+	LINE DRIVER 3 INPUT+	LINE DRIVER 3 OUTPUT
NORMAL	1	1	1	1	0	0	0	0	0	0	0	0
TRIP	1	1	1	1	1	1	1	1	0	0	0	0
NOISE	1	1	1	1	0	0	0	0	1	1	1	1
LOSS OF CHANNEL	0	0	0	0	0	0	0	0	0	0	0	0
VOLTS FOR 1 STATUS AT TP OR TERMINAL	20 TERM. 4	0.6 Q2 O Q2	0.6 Q2 O Q2	20 TERM. 5	20 TERM. 9	0.6 Q4 O Q5	0.6 Q4 O Q5	20 TERM. 7	20 TERM. 3	0.6 Q6 O Q8	0.6 Q6 O Q8	20 TERM. 8

+ = TEST POINTS NOT AVAILABLE. VOLTAGE MEASURED ON BASE OF TRANSISTOR SHOWN.
O = FOR 937A CHANNEL, INPUTS ARE MEASURED WITH REFERENCE TO POS. 48V.D.C., AND ARE NEGATIVE SIGNALS.

LOCKOUT BOARD (WHEN USED)

CONDITION	AND-1 INPUT	AND-1 OUTPUT	OR-1 INPUT	OR-1 OUTPUT	OR-2 INPUT	OR-2 OUTPUT	AND-2 INPUT	AND-2 OUTPUT	OR-3 INPUT OR-2	OR-3 INPUT LINE DRIVER 1	OR-3 OUTPUT	OR-4 INPUT AND-1	OR-4 INPUT OR-3
NORMAL	1	0	0	1	0	1	1	0	1	1	0	0	0
TRIP	1	0	0	1	1	0	0	1	0	1	0	0	0
NOISE	1	0	1	0	0	1	1	0	1	1	0	0	0
NOISE WITH TRIP	1	0	1	0	1	0	0	1	0	1	0	0	0
LOSS OF CHANNEL OO	0	1	0	1	0	1	1	0	1	0	0	1	0
LOSS OF CHANNEL THEN TRIP OO	0	1	0	1	1	0	0	1	0	0	1	1	1
LOSS OF CHANNEL THEN TRIP OO AND RETURN TO NORMAL CHANNEL	1	0	0	1	1	0	0	1	0	0	1	0	1
VOLTS FOR 1 STATUS AT TP OR TERMINAL	20 TERM. 2	16 TP 1	20 TERM. 6	20 TP 2	20 TERM. 5	13.5 TP 3	13.5 TP 3	20 TP 4	13.5 TP 3	20 TERM. 13	16 TP 5	16 TP 1	16 TP 5

+ = TEST POINTS NOT AVAILABLE. VOLTAGE MEASURED ON BASE OF TRANSISTOR SHOWN.
OO = 150 MILLISECONDS AFTER LOSS OF CHANNEL

Fig. 32. Tru

OR-2 INPUT	OR-2 OUTPUT	AND-2 INPUT	AND-2 OUTPUT	500/0 INPUT	500/0 OUTPUT+	LINE DRIVER INPUT+	LINE DRIVER OUTPUT	AND-3 INPUT	AND-3 OUTPUT	OR-3 INPUT LINE DRIVER	OR-3 INPUT AND-3	OR-3 OUTPUT	RELAY DRIVER 1 INPUT	RELAY DRIVER 1 OUTPUT°	RELAY DRIVER 2 INPUT TERM. 9	RELAY DRIVER 2 OUTPUT°
0	1	1	0	0	0	0	0	1	0	0	0	1	1	1	0	0
0	1	1	0	0	0	0	0	1	0	0	0	1	1	1	1	1
0	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0
1	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0
20 TERM. 3	10 TP 3	10 TP 3	7 TP 4	7 TP 4	0.6 Q6	0.6 Q6	20 TERM 13	20 TERM. 6	10 TP 6	20 TERM 13	10 TP 6	10 TP 7	10 TP 7	-48 TERM. 10	20 TERM. 9	-48 TERM 11

2. VOLTAGE SHOWN IS FOR 48 VOLT RELAY. VOLTAGE IS 125V FOR 125 VOLT RELAY.
URED ACROSS BASE OF TRANSISTOR SHOWN.

INDICATOR BOARD

CONDITION	AMP-1 INPUT+	AMP-1 OUTPUT+	DRIVER 2 INPUT+	DRIVER 2 OUTPUT°	AMP-2 INPUT+	AMP-2 OUTPUT+	DRIVER 1 INPUT+	DRIVER 1 OUTPUT°	DRIVER INPUT	DRIVER OUTPUT°	DRIVER 4 INPUT	DRIVER 4 OUTPUT°
NORMAL	0	0	0	0	0	0	0	0	0	0	0	0
TRIP	1	1	1	1	1	1	1	1	1	1	0	0
NOISE	0	0	0	0	0	0	0	0	0	0	1	1
VOLTS FOR 1 STATUS AT TP OR TERMINAL	— TERM 2	— TP 2	— TP 2	-48 (-125) TERM. 12	— TERM 3	— TP 4	— TP 4	-48 (-125) TERM. 4	20 TERM. 8	-48 (-125) TERM. 11	20 TERM. 9	-48 (-125) TERM. 5

+ = VOLTAGE IS A PULSE.
O = MEASURED WITH REFERENCE TO SOURCE VOLTAGE. (48 OR 125 VOLTS D.C.)

OUTPUT	AND 3 INPUT	AND 3 OUTPUT	150/15 INPUT	150/15 OUTPUT +	AND 4 INPUT +	AND 4 OUTPUT	LINE DRIVER 1 INPUT	LINE DRIVER 1 OUTPUT	AND-5 INPUT OR-1	AND-5 INPUT AND-2	AND-5 INPUT AND-4	AND-5 OUTPUT +	LINE DRIVER 2 INPUT +	LINE DRIVER 2 OUTPUT
1	1	0	0	0	0	1	1	1	1	0	1	0	0	0
1	1	0	0	0	0	1	1	1	1	1	1	1	1	1
1	1	0	0	0	0	1	1	1	0	0	1	0	0	0
1	1	0	0	0	0	1	1	1	0	1	1	0	0	0
0	0	1	1	1	1	0	0	0	1	0	0	0	0	0
0	0	1	1	1	1	0	0	0	1	1	0	0	0	0
0	0	1	1	1	1	0	0	0	1	1	0	0	0	0
10 TP 6	10 TP 6	18 TP 7	18 TP 7	0.6 Q8	0.6 Q8	16 TP 8	16 TP 8	20 TERM. 13	20 TP 2	20 TP 4	16 TP 8	0.6 Q11	0.6 Q11	20 TERM. 12

OR BOARD

CONDITION	LINE DRIVER 1 INPUT	LINE DRIVER 1 OUTPUT	ISOLATOR INPUT	ISOLATOR OUTPUT +	AND INPUT +	AND OUTPUT	OR-4 INPUT	OR-4 OUTPUT	OR-1 INPUT TERM. 11	OR-1 INPUT TERM. 12	OR-1 OUTPUT	OR-2 INPUT OR-1	OR-2 INPUT TERM. 13	OR-2 OUTPUT	OR-3 INPUT OR-1	OR-3 INPUT OR-4	OR-3 INPUT TERM. 9	OR-3 OUTPUT	LINE DRIVER 2 INPUT	LINE DRIVER 2 OUTPUT	BUFFER INPUT	BUFFER OUTPUT
NORMAL	1	1	1	1	1	0	0	1	0	0	1	1	0	1	1	1	0	0	0	0	0	0
TRIP	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1
LOSS OF CHANNEL LINK CLOSED	1	1	1	1	1	0	0	1	0	1	0	0	1	1	0	1	1	0	0	0	0	0
LOSS OF CHANNEL LINK OPEN	0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0
VOLTS FOR 1 STATUS AT TP OR TERMINAL	0.6 TERM. 5	20 TP 1	20 TP 1	0.6 Q3	0.6 Q3	16 TP 2	16 TP 2	16 TP 3	20 TERM. 11	13.5 TERM. 12	13.5 TP 4	13.5 TP 4	13.5° TERM. 13	0.8 TERM. 8	13.5 TP 4	16 TP 3	9 TERM 9	16 TP 5	16 TP 5	20 TERM. 10	20 TERM. 10	20 TERM. 7

O = 13.5 WITH LINK CLOSED, 16 VOLTS WITH LINK OPEN.
+ = TEST POINTS NOT AVAILABLE. VOLTAGE MEASURED ACROSS BASE OF TRANSISTOR SHOWN.

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h Table of STU-92 Relay

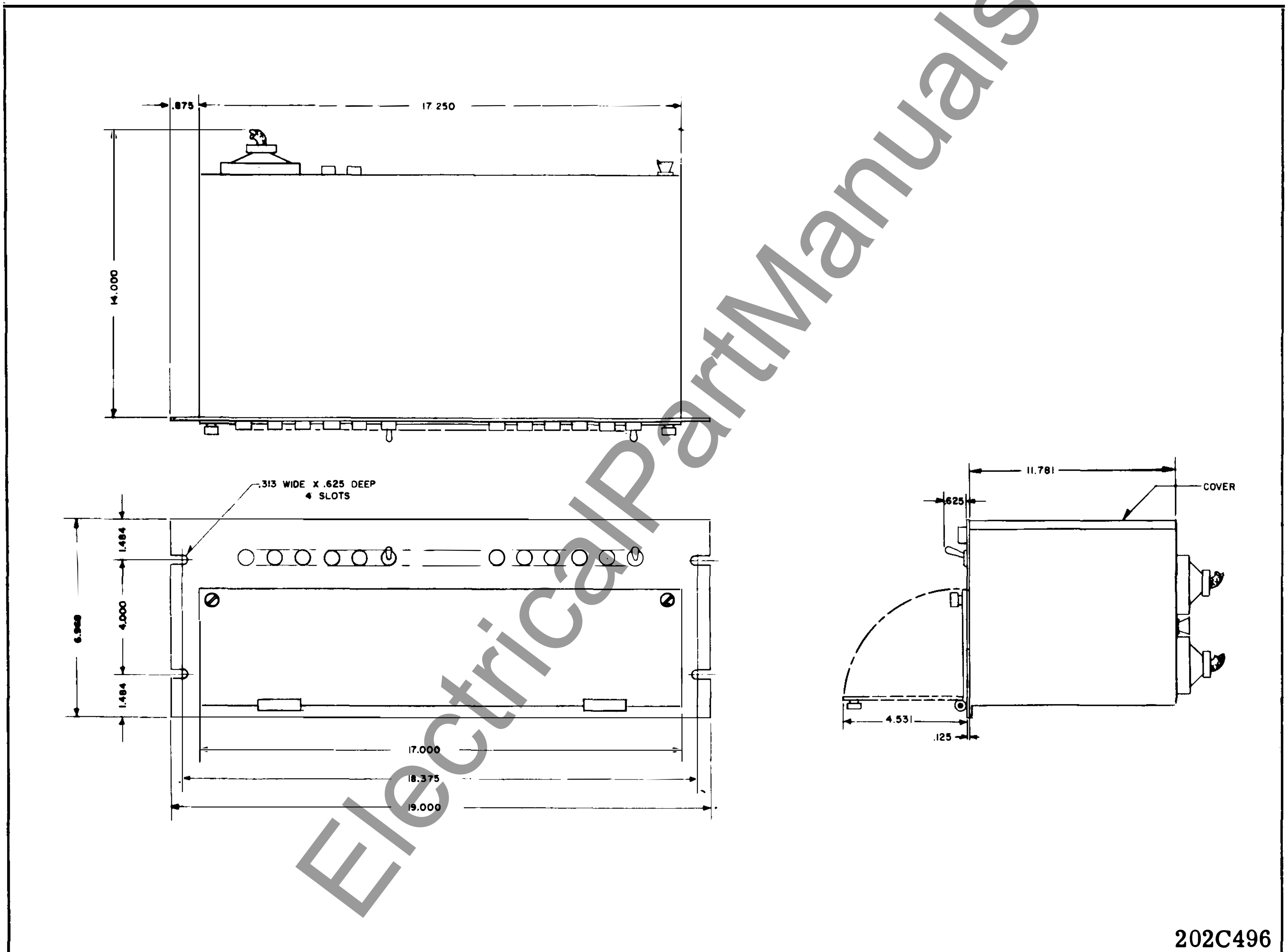


Fig. 33. Outline and Drilling Plan of the STU–92 and STU–91 Relays

WESTINGHOUSE ELECTRIC CORPORATION

RELAY-INSTRUMENT DIVISION **NEWARK, N. J.**

Printed in U.S.A.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE STU-9 DUAL CHANNEL TRANSFER - TRIP RELAY

CAUTION: It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet before energizing the equipment. Failure to observe this precaution may result in damage to the equipment. If the equipment is mounted in a cabinet, the cabinet must be bolted down to the floor or otherwise secured before swinging out the equipment rack to prevent its tipping over.

APPLICATION

The type STU-9 relay is a static auxiliary relay used in transfer-trip relaying, such as would be used to trip a remote breaker for a transformer fault at a station where no high voltage breaker is used. It is used in conjunction with dual channel frequency-shift equipment, either audio tone or power line carrier frequencies.

CONSTRUCTION

The type STU-9 relay consists of printed circuit boards, power supply, fuses, a pilot light, power switch, two channel monitoring lights, and adjustable controls mounted on a standard 19-inch wide panel, 8¾ inches high (5 rack units). Edge slots are provided for mounting the rack on a standard relay rack.

Printed Circuit Boards

The number of boards varies with the type channel used, but in general the STU-9 relay consists of five printed circuit boards; two channel interface boards, two transfer boards and a trip board. For TCF frequency shift power line carrier channels, the interface board is a part of the TCF receiver.

All of the circuitry that is suitable for mounting on printed circuit boards is contained in an enclosure that projects from the rear of the panel and is accessible by opening a hinged door on the front of the panel. The printed circuit boards slide into position in slotted guides at the top and bottom of each compartment, and the board terminals engage a terminal block at the rear of the compartment. Each board and terminal block is keyed so that if a board is placed in the wrong compartment, it cannot be inserted into the terminal block. A handle on the front of each board is labeled to identify its function in the relay.

1. Channel Interface Board

The interface board is the connecting link between the channel equipment and the transfer logic and consists of interface circuits, a lockout circuit, and the channel trip NAND. Each of the circuits performs designated functions with reference to the channel equipment. The interface circuits connect the lockout circuit and the channel trip NAND to the tone channel. In the normal state the trip NAND produces an output voltage due to the tone trip input being held at negative potential. This prevents base current from flowing into the transistor of the NAND and keeps the transistor turned off. As long as one of the three inputs is held at negative potential, a voltage output is obtained from the NAND. This voltage will exist until all inputs into the NAND are positive. Base current will then be applied to the NAND transistor and the transistor will turn on. This shorts the output of the NAND to negative potential. If the channel is lost, or if noise exists for extended periods of time, after 150 millisecond the lockout input will short the input of the NAND and hold the output in a non-operative condition. Also noise output from the tone channel will short the input of the NAND and hold the output in a non-operative condition.

This board will vary depending upon the make of frequency shift equipment used as the channel. In the case of TCF Frequency Shift Carrier equipment, the interface board is the logic board contained in the TCF receiver.

2. Transfer Logic Board

The transfer logic board contains the necessary logic to alarm on loss of channel, to transfer to a single channel operation, and to invert the trip output of the interface logic to the proper polarity for the trip board. This logic will start transferring the STU-9 relay to a single channel mode of operation upon receipt of a positive voltage from the NOT Lockout circuit of the interface board.

Additional circuitry is included in the module for the connection of two external mounted switchboard lights (one for each channel). The lights are used to monitor the trips of the individual channels and should be connected between the regulated 45-volt d.c. (terminal 2) of the STU-9 and terminal 21 (channel 1) and terminal 9 (channel 2). The style switchboard light used is either style 1589193 or 1589181 with bulb style 1124156.

3. Trip Board

The trip board contains the final output of the STU-9 relay and consists of an AND circuit and an AR type relay. Under normal channel conditions, the two inputs from the trip of the transfer
* logic are held at negative potential. The third input to the trip AND is a voltage from the transfer circuits of the transfer board. As a result the output transistor is not conducting and the AR relay does not pick up. In order for the final transistor to operate, all inputs to the AND must be above negative potential. This occurs when the AND receives a trip input from both transfer logics.

* For a loss of one channel, the trip input from the transfer logic of that channel removes its shorted input to negative, leaving the trip AND shorted to negative from the trip input of the remaining transfer logic. If both channels are lost, the trip inputs to the AND puts a positive voltage into the AND. However, the transfer input to the AND is put at negative potential to short the Input of the AND. A time delay is inserted in the transfer logic so that the transfer input to the AND is shorted to negative before the trip input switches to a positive output.

Other Circuits (when used)

As shown in Figure 1, the trip output may contain other circuits. An additional transistor may be connected to obtain a voltage output from the trip NAND. This voltage output is used to drive an externally connected SAR relay. The transistor will apply 45 volts to the input of the SAR when the STU-9 relay operates.

D256 and D258 are used where it is not desirable to use the switching mode of the STU-9 relay. By connecting these diodes with a jumper to the lockout terminals of the interface board (terminal 18) of the STU-9 relay, the STU-9 relay will lockout on a single channel failure and not switch to a single channel mode of operation. With this connection the STU-9 relay will be operated as an AND circuit with reference to the channel and not as an OR.

The style numbers of the different boards with reference to the assembly is as follows:

Style Number	Components
* 898C235G01	AR output 3 NO-1NC, D256 and D258 omitted as well as transsistor Q254 and associated resistors.
* 898C235G02	AR output 3 NO-1NC, D256 and D258 in the circuit but transistor Q254 and associated resistors omitted.
898C235G03	AR output 4 NO, D256 and D258 omitted, transistor Q254 included.
898C235G04	AR output 2NO-2NC, transistor Q254 and associated resistors included.

Power Supply

The STU-9 relay operates from a regulated 45 V.D.C. supply. This voltage is taken from a Zener diode mounted on a heat sink. Variation of the resistance values between the positive side of the unregulated D.C. supply and the 45 volt Zener diode adapt the receiver for operation on 48 or 125 volts d.c.

Card Extender

A card extender (Style No. 644B315G01) is available for facilitating circuit voltage measurements or major adjustments. After withdrawing any one of the circuit boards, the extender is inserted in that compartment. The board then is inserted into the terminal block on the front of the extender. This restores all circuit connections, and all components and test points on the board are readily accessible.

OPERATION

The signal to which the STU-9 relay responds is received from the receiver of the channel equipment. If both channels are serviceable both channel receivers must receive a trip signal from the remote terminal for the STU-9 relay to operate. If one channel fails, the STU-9 relay will lock this channel out (after an adjustable time delay) and switch into a single channel mode of operation. The system will then trip upon receipt of a trip signal from the remote terminal on the remaining channel. If both channels fail, the STU-9 locks out the trip circuit until one or both channels are restored to service. Circuits are included in the relay to alarm on the loss of a channel.

The signals from the channel receivers are applied to the STU-9 relay at the input terminals of the interface board. This signal is transmitted to the transfer board to either apply a trip signal to the trip board, to prevent the transmission of this signal, or to transmit a transfer signal to a single channel.

When the frequency shift channel equipment is transmitting a guard signal, the signals to the STU-9 relay are as shown in the logic diagram of Figure 1. The number "1" indicates that a voltage is obtained at that point while a "0" indicates that the voltage is approximately zero. As seen in the logic diagram, the STU-9 relay requires a "1" from the low signal clamp and "0" from the trip and noise clamps of the tone channels to indicate nominal operating conditions.

For the condition shown, the amber lights are on and the alarm relay is picked up. Also the input to the trip "AND" is shorted to negative through the "OR" circuits of the transfer logic.

Trip Sequence

If both channels are shifted to trip, the "0" from the tone channel changes to a "1". The trip interface of the STU-9 relay sees this change and puts a "1" into the channel trip "NAND". The output of the "NAND" goes to a "0" and the following occurs:

1. One input of the amber light AND is "0" and the light turns off.

2. The output of the NOT of the transfer logic changes to a "1" and applies a "1" to the trip AND through the OR of the transfer logic. Since all inputs to the trip AND are "1", an output is obtained to allow the AR to operate. Also the output transistor (where used) is turned on to give an output of approximately 45 volts. This voltage can be used to fire an external SAR relay to trip two breakers through Trinistor controlled rectifiers.

Loss of Signal

With reference to the logic diagram of Fig. 1, the channel equipment recognizes a loss of channel and its low signal output changes to a "0". The output of the low signal interface of the STU-9 then changes to a "1". Upon application of the "1" to the NOR circuit, a time delay is energized. If the loss of signal exists for 150 millisecond, the output of the NOR circuit changes to a "0" and the following occurs:

1. The input to the channel trip NAND is clamped to negative which locks the NAND output to a "1" state (non-trip).

2. One input to the amber light AND drops to zero and the amber light turns off.

3. The output of the NOT L_O changes to a "1", which energizes a timer. After a time delay of .5 to 2.5 sec., as determined by the timer setting, the timer times out and its output changes to a "0". The following then occurs:

   a. Alarm relay drops out to close its contacts.

   b. The output of the NOT changes to a 1 and energizes a 10-millisecond time delay circuit. After 10 milliseconds the input to the AND circuit is energized through the OR circuit.

4. Two voltages are applied to the trip "AND". The third input is clamped to negative by the output of the OR circuit on the good channel. The circuits of the STU-9 are set up for single channel operation and the system will operate if a trip signal is received from the output of the good channel.

Loss of Second Channel

If the second channel is lost while the STU-9 is set up in a single channel mode of operation, the following occurs:

1. The output of the low signal interface of the second channel changes to a 1.

2. The channel trip NAND is clamped to a "1". (non-trip).

3. The input to the amber light AND is de-energized and the amber light turns off.

4. The output of the NOT Lo changes to a 1, and the 2.5 second timer times out, and the following occurs:

   a. The alarm unit drops out to close its contacts.

   b. The input to the trip AND through terminal 11 drops to "0" instantaneously.

   c. The output of the NOT changes to a "1" and energizes a 10 millisecond delay.

   d. At the end of 10 milliseconds the input to the trip AND (through terminal 10) AND changes to a "1". Tripping cannot occur because the AND was clamped previously to negative through terminal 11.

For the condition where both channels are out of service and one or both channels are restored to service, the following occurs:

The time delay in the base of transistor Q251 in the trip logic is energized. This time delay maintains the "0" on the trip AND through diode D252, for ½ millisecond after the voltage from either D253 or D251 drops to "0" from a "1" condition.

Noise

If an output is obtained from the noise clamp of the channel equipment, the input to the noise interface changes to a "1", and energizes a NOT and a NOR circuit. The output of the NOT changes to a "0" and shorts the input to the channel trip NAND to negative. This puts the NAND in a non-operating condition. If the noise condition exists for 150 milliseconds, the STU-9 relay will recognize the condition as a loss of channel and switch into a single channel mode of operation.

CHARACTERISTICS

The type STU-9 relay is available for frequency shift channels, either tone, carrier, or a combination of both. The schematic and logic diagram for frequency-shift tone channels is shown in Figure 1.

If TCF frequency shift carrier is used as the channel equipment, the logic diagram and schematic diagram of Figures 2 and 3 apply. This logic is the same as that of Fig. 1, except that the interface board is omitted. The lockout, not lockout, and trip inputs the STU-9 transfer boards are obtained from the logic board of the TCF receiver. These quantities are the same as received from the interface logic Fig. 1.

When the STU-9 relay is used with both TCF frequency shift Carrier and frequency shift tone channels, the relay is connected as shown in Figure 4.

* For the STU-9 for use with frequency shift tone channels and an SRU output package, refer to figures 5 and 6. For these relays the trip output is a voltage.

Lockout time	150 milliseconds
Transfer time	0.5 to 2.5 seconds
Operating time	3 milliseconds with AR — 75 microseconds to obtain voltage contact.
Voltage Output Relay (when used) Maximum Output	60 milliamperes, 45 V. d.c.
* Ambient temperature range	−20°C to 55°C

Battery Voltage Variations

Rated Voltage	Allowance Variation
48 V.D.C.	42 - 56 V.D.C.
125 V.D.C.	105 - 140 V.D.C.

Battery Drain	235 milliamperes - 48 V.D.C. 275 milliamperes - 125 V.D.C.
Dimensions	Panel Height — 8¾ inch or 5 rack units. Panel Width - 19 inches

SETTING

The only setting required is the setting of the timer for transfering to a single channel mode of operation upon a loss of one channel. This setting is made by means of the timer knobs on the front panel of the relay. The knob should be locked after the setting is made.

INSTALLATION

The STU-9 relay is generally supplied in a cabinet or on a relay rack as part of a complete assembly. The location must be free from dust, excessive humidity, vibration, corrosive fumes, or heat. The maximum temperature around the chassis * must not exceed 55°C.

Routine Maintenance

Periodic checks of the relaying system as described in the assembly instructions are desirable to indicate impending failure so that the equipment can be taken out of service for correction.

All contacts should be periodically cleaned. A contact burnisher S#182A836H01 is recommended for this purpose. The use of abrasive material for cleaning contacts is not recommended because of the danger of embedding small particles in the face of the soft silver and thus impairing the contact.

Trouble-Shooting

The components of the STU-9 are operated well within their ratings, and under normal conditions they should give long, trouble-free service. However, if a relay has given an indication of trouble in service or during routine checks, the voltages tabulated in TABLE I should be checked to determine the faulty circuit. The test point and component location * on the boards are given in Figures 7, 8, 9, 10, and 11. Refer to electrical parts list for the proper component location.

TABLE I

Test point voltages to negative except where specified to positive 45 volts D.C.

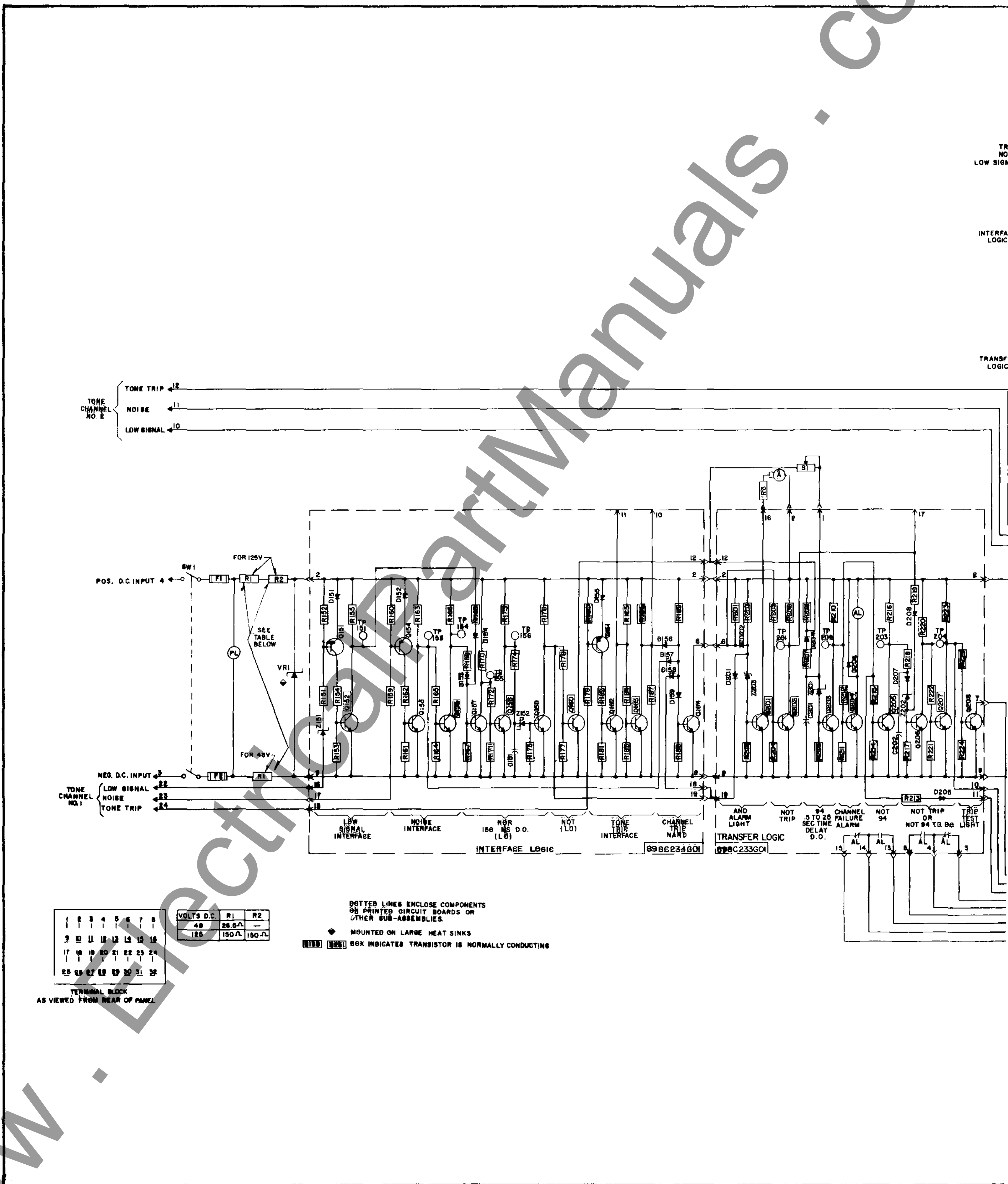
BOARD	TEST POINT	NORMAL CHANNEL	WITH NOISE ONLY	WITH LOSS OF CHANNEL ONLY		WITH TRIP ONLY
CHANNEL INTERFACE	term 16 to pos	-16	-16	-2		-16
	TP151	0.05	0.05	15		0.05
	term 17 to pos	0	—16	0		0
	TP153	15	0.05	15		15
	TP154	0.05	15	0.05		0.05
	TP155	15	0.05	0.05		15
	TP156	0.05	21	21		0.05
	term 18	10	0.10	0.10		10
	term 12	0.05	4	(with max. setting 4)		0.05
	term 15 to pos	0	0	0		-16
	term 11	15	15	15		0.05
	term 10	0.05	0.05	0.05		15
	term 6	15	15	15		0.2
TRANSFER	term 12	0.05	4	(with max. setting 4)		0.05
	term 16	0.05	45	45		45
	TP201	0.05	0.05	0.05		10
	TP202	9	0.1	0.1		9
	TP203	0.05	20	20		0.05
	TP204	13	0.05	0.05		0.05
	term 10	0.15	10	10		10
	term 11	0.7	0.7	0.7		0.7
	term 7	45	0.3	0.3		0.3
				Single CH	Both CH	
TRIP	TP251	0.05	0.05	0.05	15	0.05
	TP252	15	15	15	0.07	15
	term 10	0.15	10	10	10	10
	term 11	0.15	10	10	10	10
	term 19	0.05	0.05	0.05	0.05	43

Renewal Part

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing the repair work. When ordering parts, always give the complete nameplate data, and component style No. given in the electrical parts list.

*ELECTRICAL PARTS LIST

Circuit Symbol	Description	(W) Style No.
PANEL MOUNTED COMPONENTS		
Power Supply		
SW1	Switch	183A856H01
PL	Pilot Light 125 V.D.C.	183A825G01
	Pilot Light 48 V.D.C.	183A825G04
F1–F2	1.5 Ampere Fuse	11D9195H26
R1	26.5 Ω 40w. 48 V.D.C.	04D1299H44
R1–R2	150 Ω 40 w. 125 V.D.C.	1201499
VR1	Zener Diode, IN2828B, 50W.	184A854H06
Alarm		
A	Amber Light	183A825G08
R3–R4	330 Ω 3W.	185A207H15
Potentiometer		
S1–S2	50 K Ω	185A086H22
CHANNEL INTERFACE BOARD (898C234G01) Component Location – Fig. 7		
Capacitor		
C 151	6.8MFD 35 V.D.C.	184A661H25
Diodes		
D151	IN457A	184A855H07
Transistors		
Q151-Q154-Q161 Q152-Q155-Q156 Q157-Q158-Q162	2N2043	184A638H21
Q163	2N696	762A585H01
Q159	2N697	184A638H18
Q160-Q164	2N699	184A638H19
Resistors		
R151-R159-R179	6.8K Ω–½W.	184A763H47
R152-R160-R174 R180	1K Ω–½W.	184A763H27
R153-R161-R164 R167-R171	10K Ω–½W.	184A763H51
Resistors (Cont.)		
R175-R177-R181-R183-R188-R154-R162-R182-R189	100K Ω–½W.	184A763H75
R155-R163-R166-R170-R185-R186	68K Ω–½W.	184A763H71
R165-R168-R169-R172-R184-R187	33K Ω–½W.	184A763H63
R173	39K Ω–½W.	184A763H65
R176	12K Ω–½W.	184A763H53
R178	3.3KΩ–½W.	184A763H39
Zener Diodes		
Z151	IN957B 6.7V	186A797H06
Z152	IN3686B 20V	185A212H06
TRANSFER BOARD (898C233G01) Component location – Fig. 8		
Capacitors		
C201	68MFD 35 V.D.C.	187A508H02
C202	0.5MFD	187A624H11
Diodes		
D201, D202 D204 to D208	IN457A	184A638H07
Transistors		
Q201-Q202-Q204-Q208	2N699	184A638H19
Q203-Q207	2N697	184A638H18
Q205-Q206	2N696	762A585H01
Resistors		
R201-R206-R216-R220	68K Ω–½W.	184A763H71
R202-R204-R208-R209-R211-R214-R217-R221-R224	10K Ω–½W.	184A763H51
R203	10K Ω–1W.	187A643H51
R205-218-R219-R222	33K Ω–½W.	184A763H63
R207	1K Ω–½W.	184A763H27
R210-R223	12K Ω–½W.	184A763H53
R212-R225	3.3KΩ–½W.	184A763H39
R213-R215	22K Ω–½W.	184A763H59

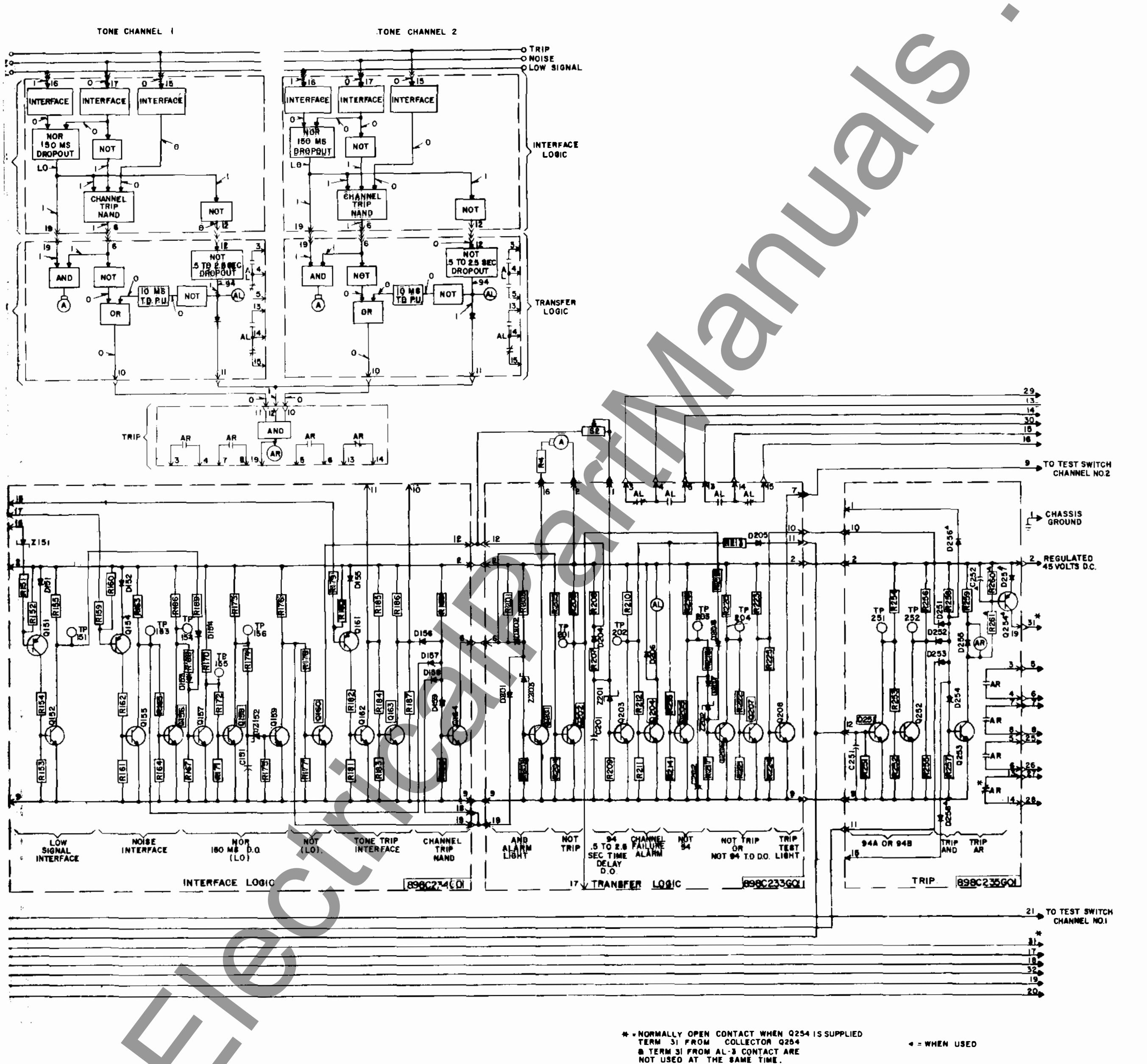


* *Fig. 1. Internal Schematic of Type STU-9 Relay*

*ELECTRICAL PARTS LIST (Continued)

Circuit Symbol	Description	(W) Style No.
TRANSFER BOARD (898C233G01) (Cont.)		
Zener Diodes		
Z201	IN3686B 20V	185A212H06
Z202, Z203	IN957B 6.8V	186A797H06
Alarm Unit		
AL	Telephone Relay	408C062H07
TRANSFER BOARD (899C712G01) Component location – Fig. 9		
Capacitors		
C201	68 mfd, 35 Vdc	187A508H02
C202	0.5 mfd	187A624H11
Diodes		
D201, D202, D204-D208	1N475A	184A638H07
Transistors		
Q201-Q202-Q204-Q208	2N699	184A638H19
Q203-Q207	2N697	184A638H18
Q205-Q206	2N696	762A585H01
Resistors		
R201-R206-R216-R220	68 K-Ω,½W.	184A763H71
R202-R204-R208-R209-R211-R214-R217-R221-R224	10 K-Ω,½W.	184A763H51
R203	10 K-Ω,1W.	187A643H51
R205-R218-R219-R222	33 K-Ω,½W.	184A763H63
R207	1 K-Ω, ½W.	184A763H27
R210-R212	22 K-Ω,½W.	184A763H59
R213-R215	22 K-Ω,½W.	184A763H59
R223	12 K-Ω,½W.	184A763H53
R225	3.3 K-Ω,½W.	184A763H39
Zener Diodes		
Z201	1N3686B,20V	185A212H06
Z202,Z203	1N957B, 6.8V	186A797H06
TRIP BOARD (898C235G01) Component location – Fig. 10		
Capacitors		
C251-C252	.25 uf	187A624H02

Circuit Symbol	Description	(W) Style No.
Diodes		
D251 to D255	IN457A	184A855H07
D252 to D253 (when used)	IN457A	184A855H07
Transistors		
Q251-Q252	2N696	762A585H01
Q253	2N699	184A638H19
Q254 (when used)	2N2043	184A638H21
Resistors		
R251-R252-R257	10KΩ–½W.	184A763H51
R253-R255	33KΩ–½W.	184A763H63
R254-R256	68KΩ–½W.	184A763H71
R258	10KΩ–1W.	184A643H51
R259	800Ω–3W.	184A859H06
R260 (when used)	1K Ω–½W.	184A763H27
R261 (when used)	10KΩ–½W.	184A763H51
AR Unit		
AR (when used)	3NO–INC contacts	408C845G23
AR (when used)	4NO-contacts	408C845G13
AR (when used)	2NO-2NC contacts	408C845G09
TRIP BOARD (899C700G01) Component location – Fig. 11		
Capacitor		
C251-C252	0.25 UF	187A624H02
D251 to D255-D258-D260	1N475A	184A855H07
D256-D257-D259-D261	CER-69	188A342H06
Transistors		
Q251-Q252	2N696	762A585H01
Q253	2N699	184A638H19
Q254-Q255-Q256	2N4356	849A441H02
Resistors		
R251-R252-R257-R259-R263-R266	10K, ½W.	184A763H51
R253-R255	33K, ½W.	184A763H63
R254-R256	68K, ½W.	184A763H71
R258	100K, ½W.	184A763H75
R261-R264-R267	2.25K, 3W.	184A636H03
R260-R262-R265	1K, ½W.	184A763H27
Zener Diodes		
Z251	1N3686B	185A212H06



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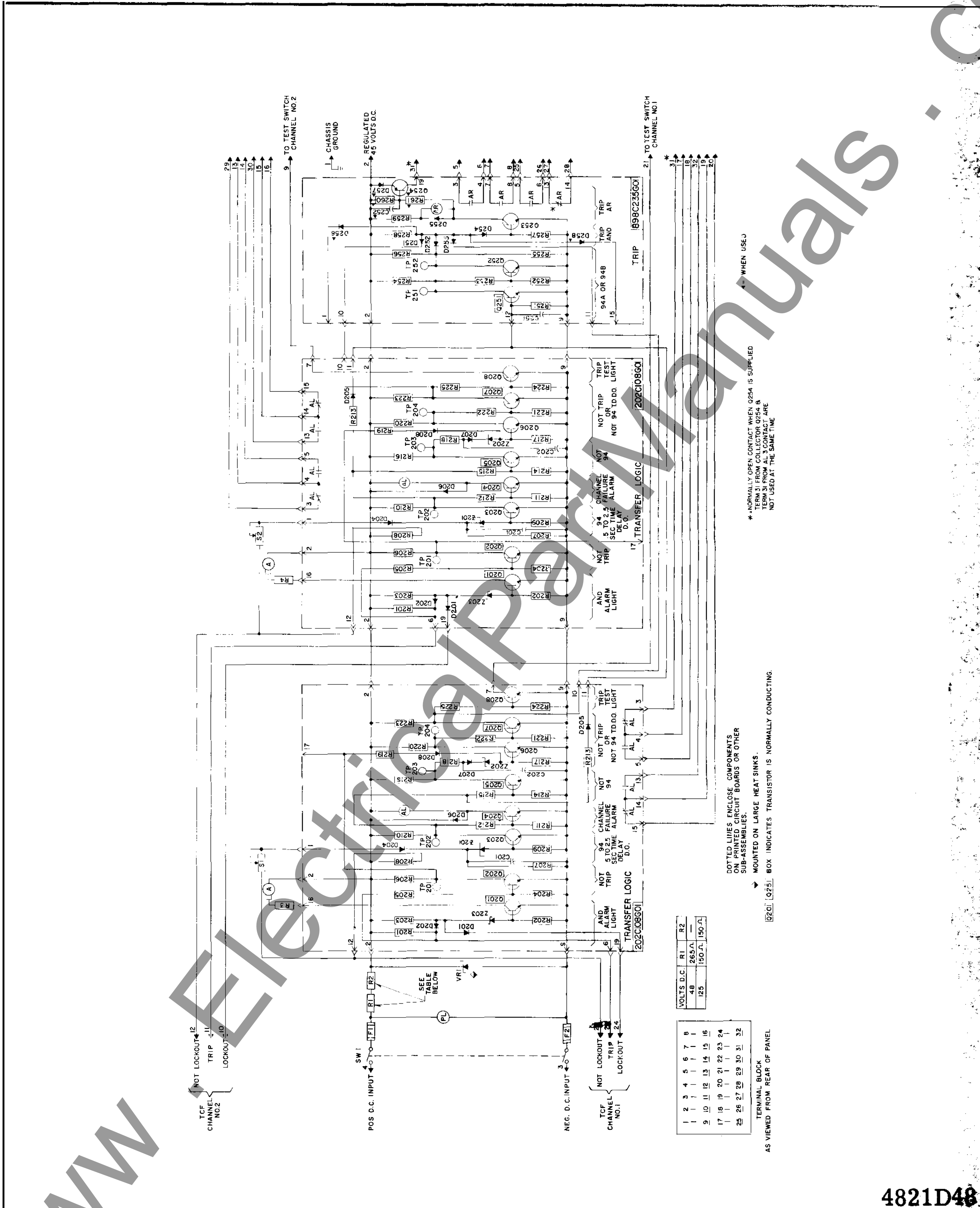
for Frequency Shift Tone Channels



* *Fig. 2. Internal Schematic of Type STU-9 Relay for TCF Frequency Shift Carrier Channel*

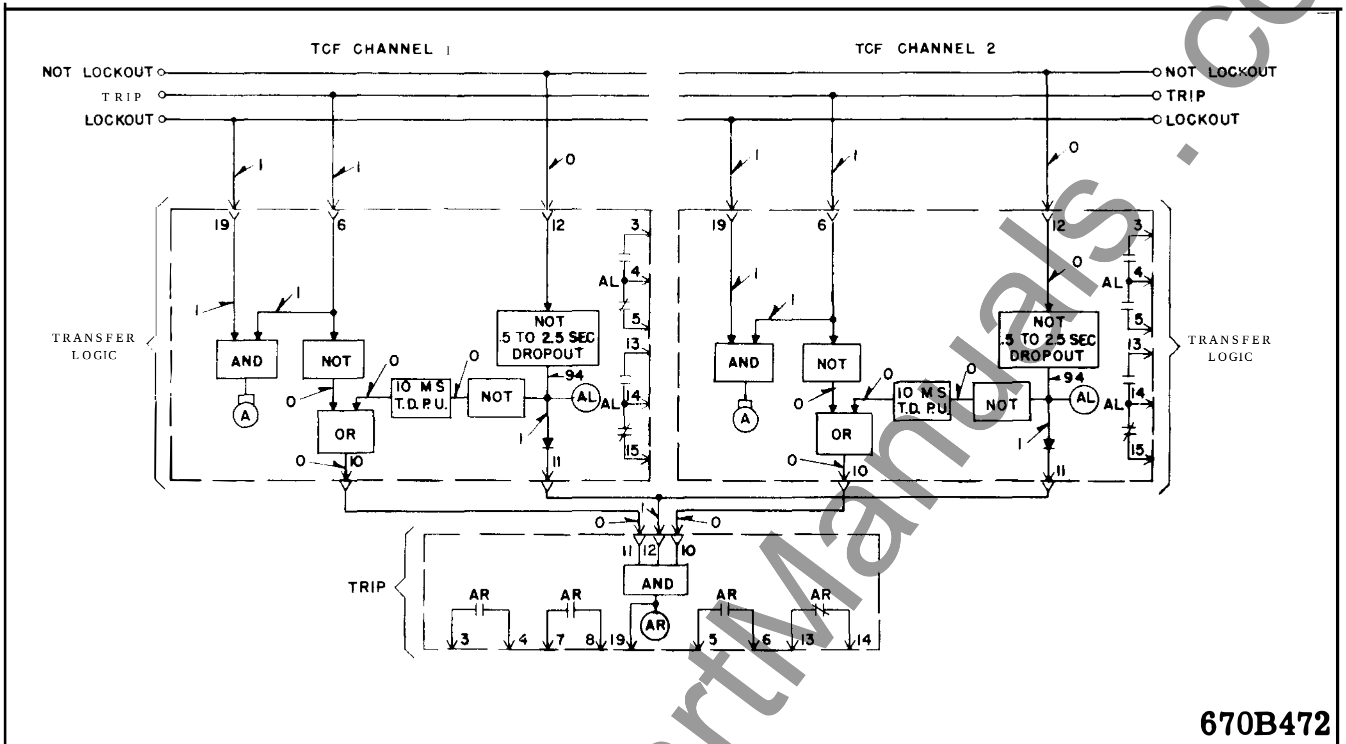
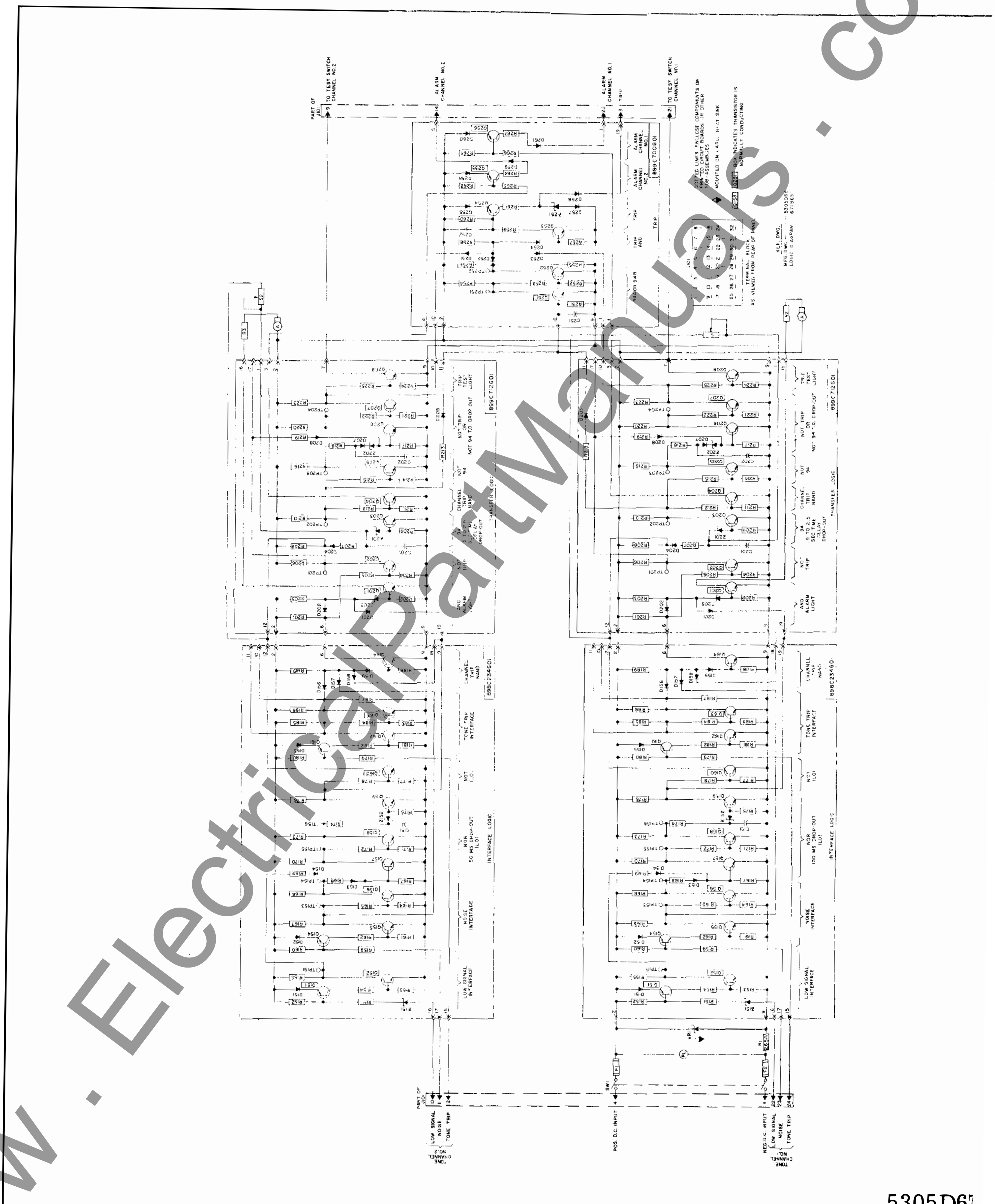
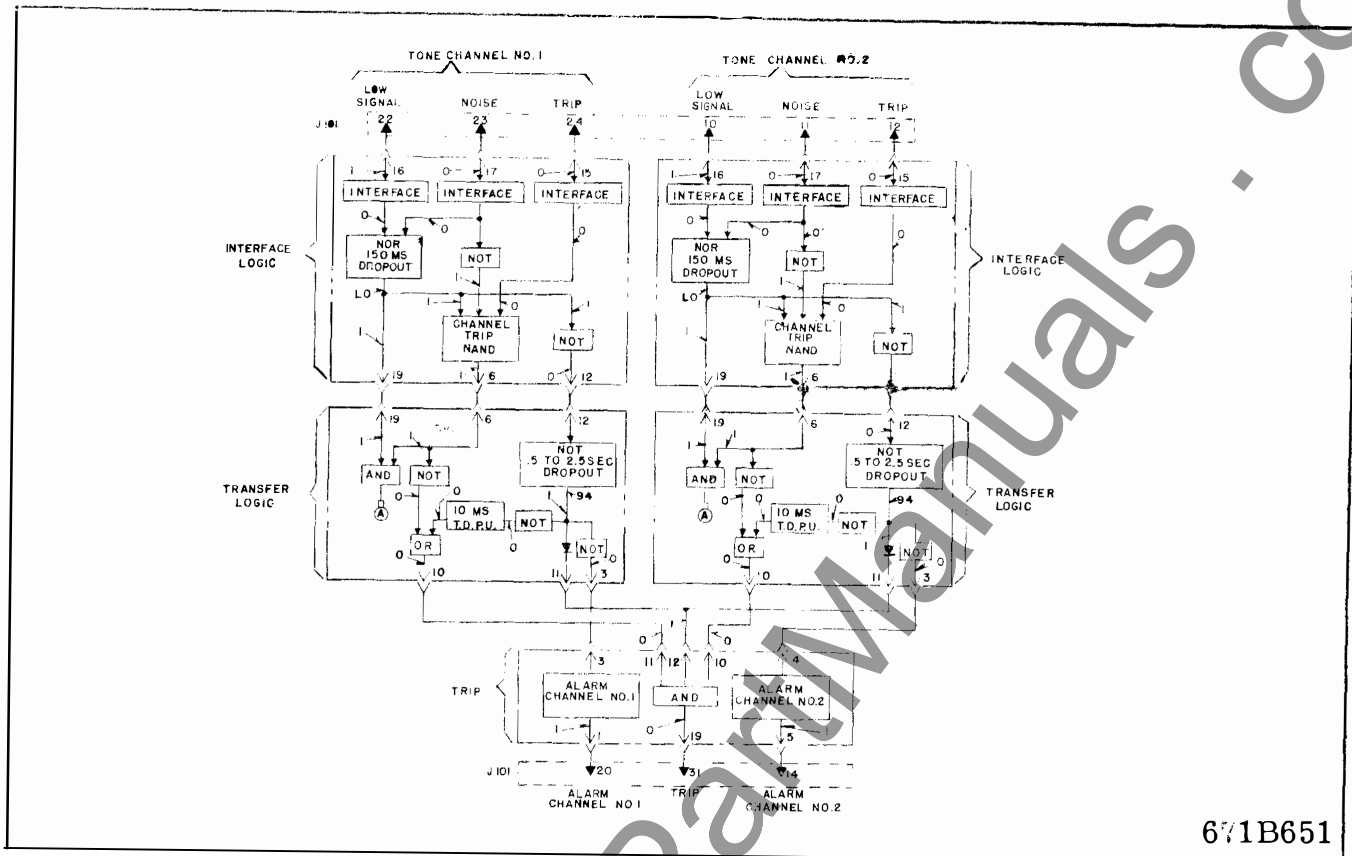


Fig. 3. Logic Diagram of Type STU-9 Relay for TCF Frequency Shift Carrier Channel



* *Fig. 5.*



* Fig. 6.

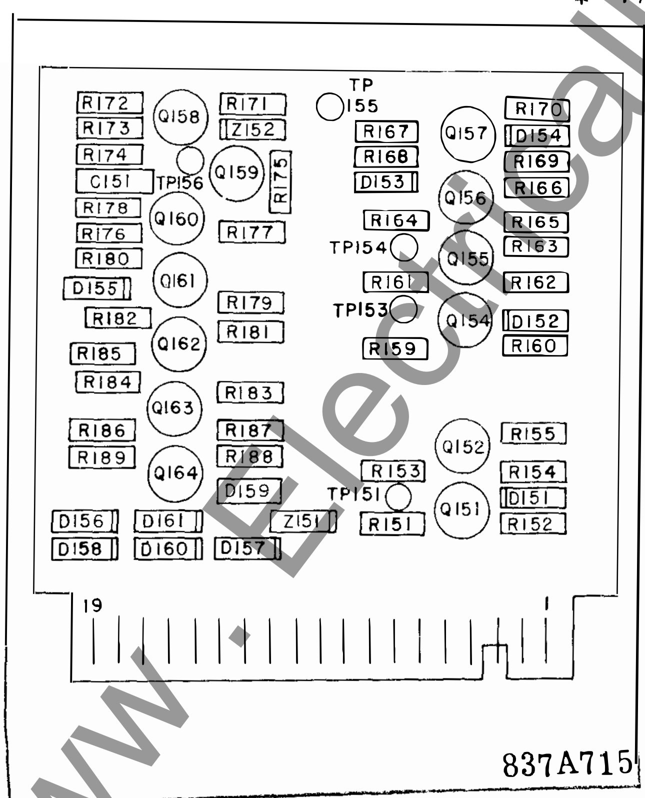
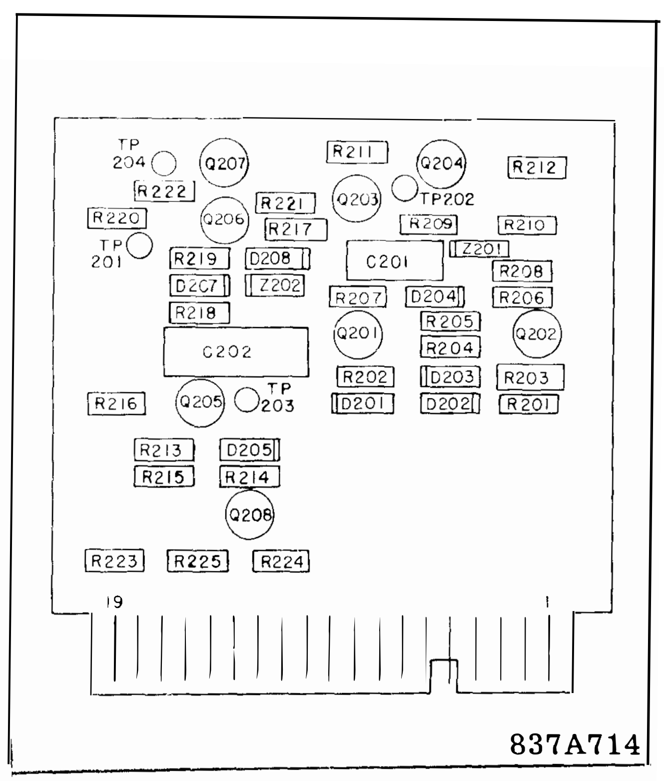
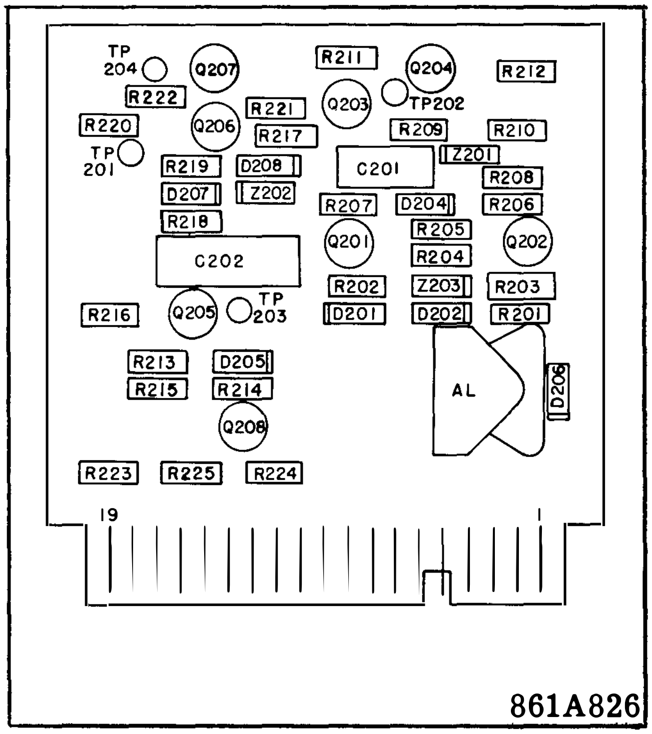


Fig. 7. Component Locations on the Interface Logic Board



* Fig. 8. Component Location on the Transfer Logic Board



* Fig. 9.

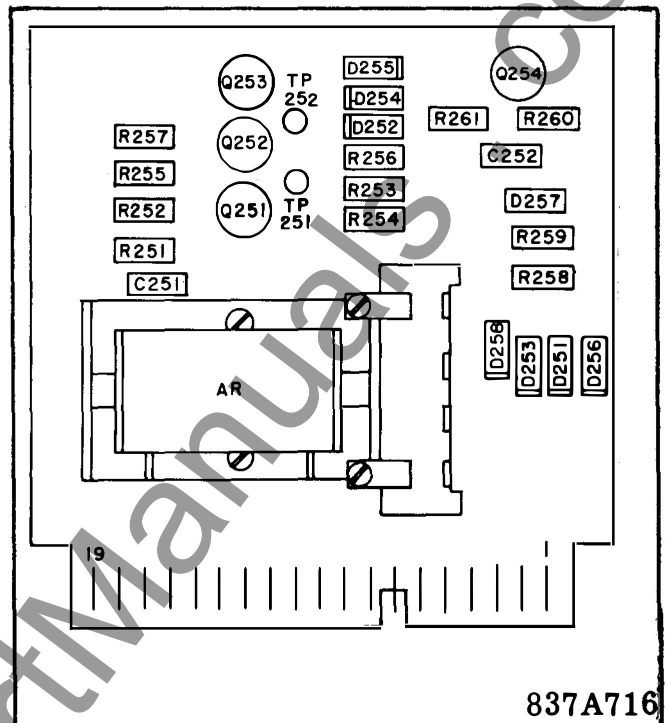
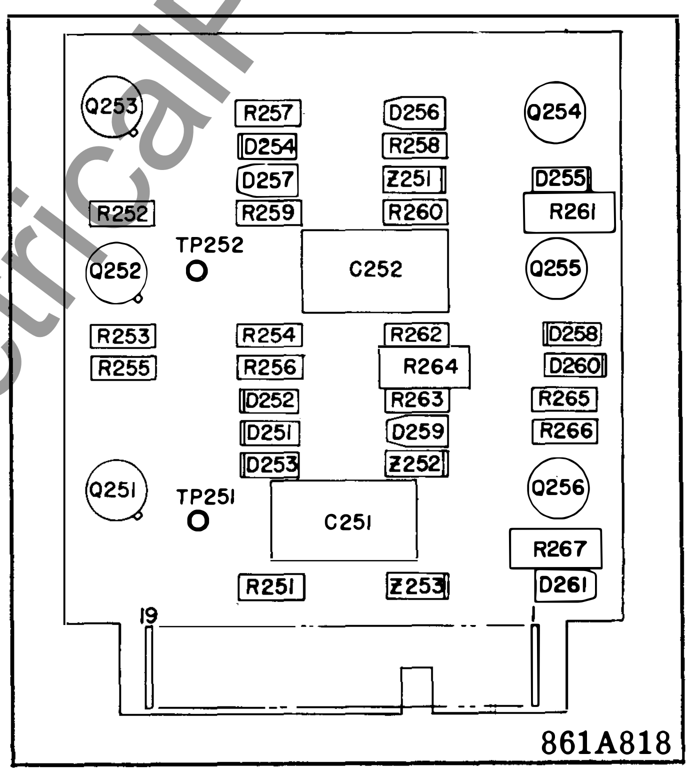


Fig. 10. Component Location on the Trip Board



* Fig. 11.

WESTINGHOUSE ELECTRIC CORPORATION

RELAY-INSTRUMENT DIVISION **NEWARK, N. J.**

Printed in U.S.A.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE STU-9 DUAL CHANNEL TRANSFER - TRIP RELAY

CAUTION: It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet before energizing the equipment. Failure to observe this precaution may result in damage to the equipment. If the equipment is mounted in a cabinet, the cabinet must be bolted down to the floor or otherwise secured before swinging out the equipment rack to prevent its tipping over.

APPLICATION

The type STU-9 relay is a static auxiliary relay used in transfer-trip relaying, such as would be used to trip a remote breaker for a transformer fault at a station where no high voltage breaker is used. It is used in conjunction with dual channel frequency-shift equipment, either audio tone or power line carrier frequencies.

CONSTRUCTION

The type STU-9 relay consists of printed circuit boards, power supply, fuses, a pilot light, power switch, two channel monitoring lights, and adjustable controls mounted on a standard 19-inch wide panel, 8¾ inches high (5 rack units). Edge slots are provided for mounting the rack on a standard relay rack. The components are connected as shown in Fig. 1.

Printed Circuit Boards

The number of boards varies with the type channel used, but in general the STU-9 relay consists of five printed circuit boards; two channel interface boards, two transfer boards and a trip board. For TCF frequency shift power line carrier channels, the interface board is a part of the TCF receiver.

All of the circuitry that is suitable for mounting on printed circuit boards is contained in an enclosure that projects from the rear of the panel and is accessible by opening a hinged door on the front of the panel. The printed circuit boards slide into position in slotted guides at the top and bottom of each compartment, and the board terminals engage a terminal block at the rear of the compartment. Each board and terminal block is keyed so that if a board is placed in the wrong compartment, it cannot be inserted into the terminal block. A handle on the front of each board is labeled to identify its function in the relay.

1. Channel Interface Board

The interface board is the connecting link between the channel equipment and the transfer logic and consists of interface circuits, a lockout circuit, and the channel trip NAND. Each of the circuits performs designated functions with reference to the channel equipment. The interface circuits connect the lockout circuit and the channel trip NAND to the tone channel. In the normal state the trip NAND produces an output voltage due to the tone trip input being held at negative potential. This prevents base current from flowing into the transistor of the NAND and keeps the transistor turned off. As long as one of the three inputs is held at negative potential, a voltage output is obtained from the NAND. This voltage will exist until all inputs into the NAND are positive. Base current will then be applied to the NAND transistor and the transistor will turn on. This shorts the output of the NAND to negative potential. If the channel is lost, or if noise exists for extended periods of time, after 150 millisecond the lockout input will short the input of the NAND and hold the output in a non-operative condition. Also noise output from the tone channel will short the input of the NAND and hold the output in a non-operative condition.

This board will vary depending upon the make of frequency shift equipment used as the channel. In the case of TCF Frequency Shift Carrier equipment, the interface board is the logic board contained in the TCF receiver.

2. Transfer Logic Board

The transfer logic board contains the necessary

SUPERSEDES I.L. 41-959.2A
*Denotes Change From Superseded Issue.

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logic to alarm on loss of channel, to transfer to a single channel operation, and to invert the trip output of the interface logic to the proper polarity for the trip board. This logic will start transferring the STU-9 relay to a single channel mode of operation upon receipt of a positive voltage from the NOT Lockout circuit of the interface board.

Additional circuitry is included in the module for the connection of two external mounted switchboard lights (one for each channel). The lights are used to monitor the trips of the individual channels and should be connected between the regulated 45-volt d.c. (terminal 2) of the STU-9 and terminal 21 (channel 1) and terminal 9 (channel 2). The style switchboard light used is either style 1589193 or 1589181 with bulb style 1124156.

3. Trip Board

The trip board contains the final output of the STU-9 relay and consists of an AND circuit and an AR type relay. Under normal channel conditions, the two inputs from the trip of the transfer logic is held at negative potential. The third input to the trip AND is a voltage from the transfer circuits of the transfer board. As a result the output transistor is not conducting and the AR relay does not pick up. In order for the final transistor to operate, all inputs to the AND must be above negative potential. This occurs when the AND receives a trip input from both transfer logics.

For a lost of one channel, the trip input from the transfer logic of that channel removes its shorted input to negative, leaving the trip AND shorted to negative from the trip input of the remaining transfer logic. If both channels are lost, the trip inputs to the AND puts a positive voltage into the AND. However, the transfer input to the AND is put at negative potential to short the Input of the AND. A time delay is inserted in the transfer logic so that the transfer input to the AND is shorted to negative before the trip input switches to a positive output.

Other Circuits (when used)

As shown in Figure 1, the trip output may contain other circuits. An additional transistor may be connected to obtain a voltage output from the trip NAND. This voltage output is used to drive an externally connected SAR relay. The transistor will apply 45 volts to the input of the SAR when the STU-9 relay operates.

D256 and D258 are used where it is not desirable to use the switching mode of the STU-9 relay. By connecting these diodes with a jumper to the lockout terminals of the interface board (terminal 18) of the STU-9 relay, the STU-9 relay will lockout on a single channel failure and not switch to a single channel mode of operation. With this connection the STU-9 relay will be operated as an AND circuit with reference to the channel and not as an OR.

The style numbers of the different boards with reference to the assembly is as follows:

Style Number	Components
898C235G01	AR output 3 NO-INC, D256 and D258 omitted as well as transsistor Q254 and associated resistors.
898C235G02	AR output 3 NO-INC, D256 and D258 in the circuit but transistor Q254 and associated resistors omitted.
898C235G03	AR output 4 NO, D256 and D258 omitted, transistor Q254 included.
898C235G04	AR output 2NO-2NC, transistor Q254 and associated resistors included.

Power Supply

The STU-9 relay operates from a regulated 45 V.D.C. supply. This voltage is taken from a Zener diode mounted on a heat sink. Variation of the resistance values between the positive side of the unregulated D.C. supply and the 45 volt Zener diode adapt the receiver for operation on 48 or 125 volts d.c.

Card Extender

A card extender (Style No. 644B315G01) is available for facilitating circuit voltage measurements or major adjustments. After withdrawing any one of the circuit boards, the extender is inserted in that compartment. The board then is inserted into the terminal block on the front of the extender. This restores all circuit connections, and all components and test points on the board are readily accessible.

OPERATION

The signal to which the STU-9 relay responds is received from the receiver of the channel equipment. If both channels are serviceable both channel receivers must receive a trip signal from the remote terminal for the STU-9 relay to operate. If one channel fails, the STU-9 relay will lock this channel out (after an adjustable time delay) and switch into a single channel mode of operation. The system will then trip upon receipt of a trip signal from the remote terminal on the remaining channel. If both channels fail, the STU-9 locks out the trip circuit until one or both channels are restored to service. Circuits are included in the relay to alarm on the loss of a channel.

The signals from the channel receivers are applied to the STU-9 relay at the input terminals of the interface board. This signal is transmitted to the transfer board to either apply a trip signal to the trip board, to prevent the transmission of this signal, or to transmit a transfer signal to a single channel.

When the frequency shift channel equipment is transmitting a guard signal, the signals to the STU-9 relay are as shown in the logic diagram of Figure 1. The number "1" indicates that a voltage is obtained at that point while a "0" indicates that the voltage is approximately zero. As seen in the logic diagram, the STU-9 relay requires a "1" from the low signal clamp and "0" from the trip and noise clamps of the tone channels to indicate nominal operating conditions.

For the condition shown, the amber lights are on and the alarm relay is picked up. Also the input to the trip "AND" is shorted to negative through the "OR" circuits of the transfer logic.

Trip Sequence

If both channels are shifted to trip, the "0" from the tone channel changes to a "1". The trip interface of the STU-9 relay sees this change and puts a "1" into the channel trip "NAND". The output of the "NAND" goes to a "0" and the following occurs:

1. One input of the amber light AND is "0" and the light turns off.

2. The output of the NOT of the transfer logic changes to a "1" and applies a "1" to the trip AND through the OR of the transfer logic. Since all inputs to the trip AND are "1", an output is obtained to allow the AR to operate. Also the output transistor (where used) is turned on to give an output of approximately 45 volts. This voltage can be used to fire an external SAR relay to trip two breakers through Trinistor controlled rectifiers.

Loss of Signal

With reference to the logic diagram of Fig. 1, the channel equipment recognizes a loss of channel and its low signal output changes to a "0". The output of the low signal interface of the STU-9 then changes to a "1". Upon application of the "1" to the NOR circuit, a time delay is energized. If the loss of signal exists for 150 millisecond, the output of the NOR circuit changes to a "0" and the following occurs:

1. The input to the channel trip NAND is clamped to negative which locks the NAND output to a "1" state (non-trip).

2. One input to the amber light AND drops to zero and the amber light turns off.

3. The output of the NOT L_O changes to a "1", which energizes a timer. After a time delay of .5 to 2.5 sec., as determined by the timer setting, the timer times out and its output changes to a "0". The following then occurs:

   a. Alarm relay drops out to close its contacts.

   b. The output of the NOT changes to a 1 and energizes a 10-millisecond time delay circuit. After 10 milliseconds the input to the AND circuit is energized through the OR circuit.

4. Two voltages are applied to the trip "AND". The third input is clamped to negative by the output of the OR circuit on the good channel. The circuits of the STU-9 are set up for single channel operation and the system will operate if a trip signal is received from the output of the good channel.

Loss of Second Channel

If the second channel is lost while the STU-9 is set up in a single channel mode of operation, the following occurs:

1. The output of the low signal interface of the second channel changes to a 1.

2. The channel trip NAND is clamped to a "1". (non-trip).

3. The input to the amber light AND is de-energized and the amber light turns off.

4. The output of the NOT Lo changes to a 1, and the 2.5 second timer times out, and the following occurs:

   a. The alarm unit drops out to close its contacts.

   b. The input to the trip AND through terminal 11 drops to "0" instantaneously.

   c. The output of the NOT changes to a "1" and energizes a 10 millisecond delay.

   d. At the end of 10 milliseconds the input to the trip AND (through terminal 10) AND changes to a "1". Tripping cannot occur because the AND was clamped previously to negative through terminal 11.

For the condition where both channels are out of service and one or both channels are restored to service, the following occurs:

The time delay in the base of transistor Q251 in the trip logic is energized. This time delay maintains the "0" on the trip AND through diode D252, for ½ millisecond after the voltage from either D253 or D251 drops to "0" from a "1" condition.

Noise

If an output is obtained from the noise clamp of the channel equipment, the input to the noise interface changes to a "1", and energizes a NOT and a NOR circuit. The output of the NOT changes to a "0" and shorts the input to the channel trip NAND to negative. This puts the NAND in a non-operating condition. If the noise condition exists for 150 milliseconds, the STU-9 relay will recognize the condition as a loss of channel and switch into a single channel mode of operation.

CHARACTERISTICS

The type STU-9 relay is available for frequency shift channels, either tone, carrier, or a combination of both. The schematic and logic diagram for frequency-shift tone channels is shown in Figure 1.

If TCF frequency shift carrier is used as the channel equipment, the logic diagram and schematic diagram of Figures 2 and 3 apply. This logic is the same as that of Fig. 1, except that the interface board is omitted. The lockout, not lockout, and trip inputs the STU-9 transfer boards are obtained from the logic board of the TCF receiver. These quantities are the same as received from the interface logic Fig. 1.

When the STU-9 relay is used with both TCF frequency shift Carrier and frequency shift tone channels, the relay is connected as shown in Figure 4.

Lockout time	150 milliseconds
Transfer time	0.5 to 2.5 seconds
Operating time	3 milliseconds with AR — 75 microseconds to obtain voltage contact.
Voltage Output Relay (when used) Maximum Output	60 milliamperes, 45 V. d.c.
Ambient temperature range	-20 °C to +60 °C

Battery Voltage Variations

Rated Voltage	Allowance Variation
48 V.D.C.	42 - 56 V.D.C.
125 V.D.C.	105 - 140 V.D.C.

Battery Drain	235 milliamperes-48 V.D.C. 275 milliamperes - 125 V.D.C.
Dimensions	Panel Height — 8¾ inch or 5 rack units. Panel Width-19 inches

SETTING

The only setting required is the setting of the timer for transfering to a single channel mode of operation upon a loss of one channel. This setting is made by means of the timer knobs on the front panel of the relay. The knob should be locked after the setting is made.

INSTALLATION

The STU-9 relay is generally supplied in a cabinet or on a relay rack as part of a complete assembly. The location must be free from dust, excessive humidity, vibration, corrosive fumes, or heat. The maximum temperature around the chassis must not exceed 60 °C.

Routine Maintenance

Periodic checks of the relaying system as described in the assembly instructions are desirable to indicate impending failure so that the equipment can be taken out of service for correction.

All contacts should be periodically cleaned. A contact burnisher S#182A836H01 is recommended for this purpose. The use of abrasive material for cleaning contacts is not recommended because of the danger of embedding small particles in the face of the soft silver and thus impairing the contact.

Trouble-Shooting

The components of the STU-9 are operated well within their ratings, and under normal conditions they should give long, trouble-free service. However, if a relay has given an indication of trouble in service or during routine checks, the voltages tabulated in TABLE I should be checked to determine the faulty circuit. The test point and component location on the boards are given in Figures 5, 6, and 7.

TABLE I

Test point voltages to negative except where specified to positive 45 volts D.C.

BOARD	TEST POINT	NORMAL CHANNEL	WITH NOISE ONLY	WITH LOSS OF CHANNEL ONLY		WITH TRIP ONLY
CHANNEL INTERFACE	term 16 to pos	-16	-16	-2		-16
	TP151	0.05	0.05	15		0.05
	term 17 to pos	0	-16	0		0
	TP153	15	0.05	15		15
	TP154	0.05	15	0.05		0.05
	TP155	15	0.05	0.05		15
	TP156	0.05	21	21		0.05
	term 18	10	0.10	0.10		10
	term 12	0.05	4	(with max. setting 4)		0.05
	term 15 to pos	0	0	0		-16
	term 11	15	15	15		0.05
	term 10	0.05	0.05	0.05		15
	term 6	15	15	15		0.2
TRANSFER	term 12	0.05	4	(with max. setting 4)		0.05
	term 16	0.05	45	45		45
	TP201	0.05	0.05	0.05		10
	TP202	9	0.1	0.1		9
	TP203	0.05	20	20		0.05
	TP204	13	0.05	0.05		0.05
	term 10	0.15	10	10		10
	term 11	0.7	0.7	0.7		0.7
	term 7	45	0.3	0.3		0.3
				Single CH	Both CH	
TRIP	TP251	0.05	0.05	0.05	15	0.05
	TP252	15	15	15	0.07	15
	term 10	0.15	10	10	10	10
	term 11	0.15	10	10	10	10
	term 19	0.05	0.05	0.05	0.05	43

Renewal Part

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing the repair work. When ordering parts, always give the complete nameplate data, and component style No. given in the electrical parts list.

ELECTRICAL PARTS LIST

PANEL MOUNTED COMPONENTS

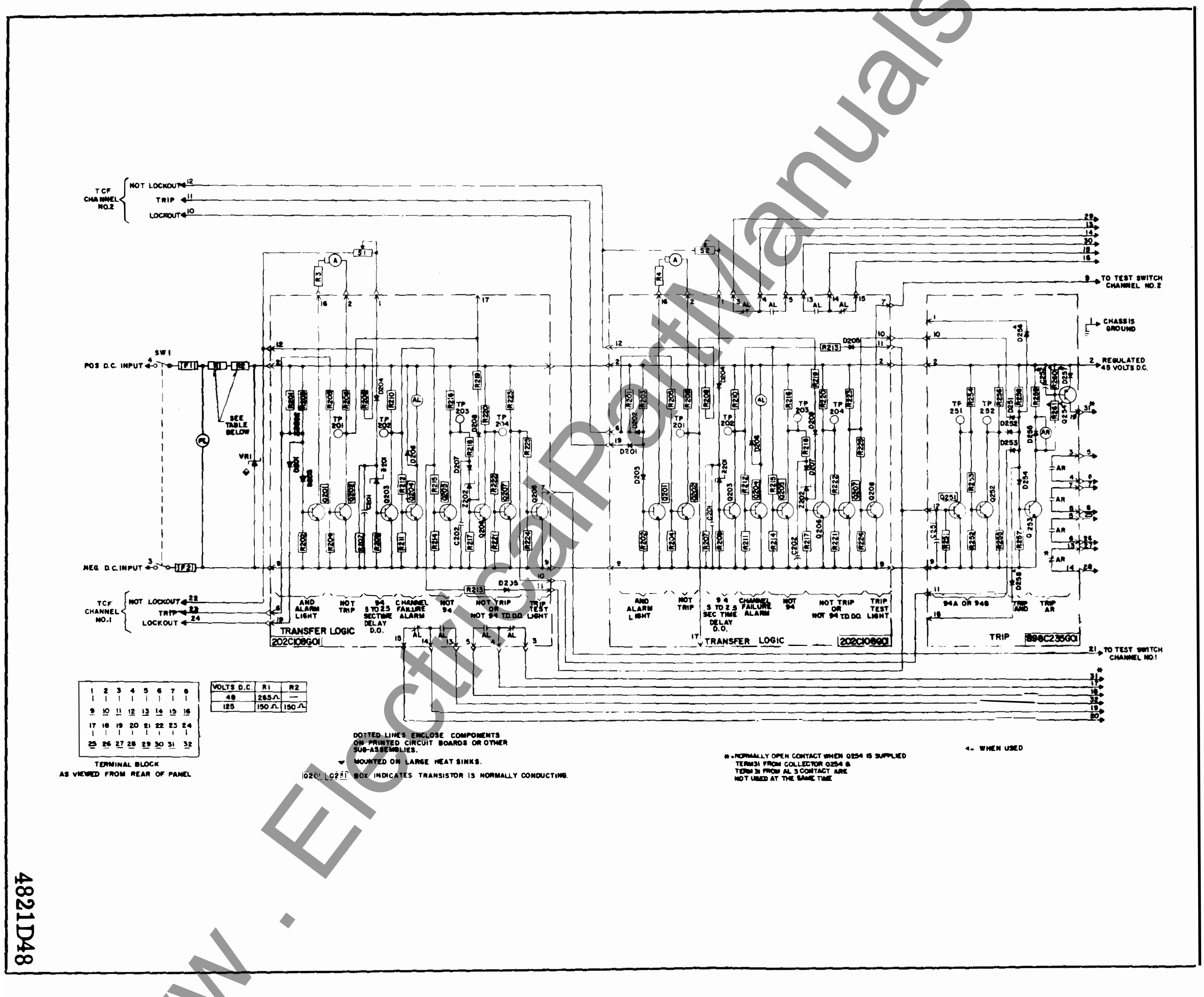
Circuit Symbol	Description	(W) Style No.
	Power Supply	
SW1	Switch	183A856H01
PL	Pilot Light 125 V.D.C.	183A825G01
	Pilot Light 48 V.D.C.	183A825G04
F1-F2	1.5 Ampere Fuse	11D9195H26
R1	26.5 Ω 40w. 48 V.D.C.	04D1299H44
R1-R2	150 Ω 40 w. 125 V.D.C.	1201499
VR1	Zener Diode, IN2828B, 50W.	184A854H06
	Alarm	
A	Amber Light	183A825G08
R3-R4	330 Ω 3W.	185A207H15
	Potentiometer	
S1-S2	50 K Ω	185A086H22

CHANNEL INTERFACE BOARD

Circuit Symbol	Description	(W) Style No.
	Capacitor	
C151	6.8MFD 35 V.D.C.	184A661H25
	Diodes	
D151	IN457A	184A855H07
	Transistors	
Q151-Q154-Q161 Q152-Q155-Q156 Q157-Q158-Q162	2N2043	184A638H21
Q163	2N696	762A585H01
Q159	2N697	184A638H18
Q160-Q164	2N699	184A638H19
	Resistors	
R151-R159-R179	6.8K Ω -½W	184A763H47
R152-R160-R174 R180	1K Ω -½W.	184A763H27
R153-R161-R164 R167-R171	10K Ω -½W.	184A763H51
R175-R177-R181- R183-R188-R154- R162-R182-R189	100K Ω-½W.	184A763H75
R155-R163-R166- R170-R185-R186	68K Ω -½W.	184A763H71
R165-R168-R169- R172-R184-R187	33K Ω -½W.	184A763H63
R173	39K Ω -½W.	184A763H65
R176	12K Ω -½W.	184A763H53
R178	3.3K Ω-½W.	184A763H39
	Zener Diodes	
Z151	IN957B 6.7V	186A797H06
Z152	IN3686B 20V	185A212H06

TRANSFER BOARD

Circuit Symbol	Description	(W) Style No.
	Capacitors	
C201	68MFD 35 V.D.C.	187A508H02
C202	0.5MFD	187A624H11
	Diodes	
D201 to D208	IN457A	184A638H07
	Transistors	
Q201-Q202-Q204- Q208	2N699	184A638H19
Q203-Q207	2N697	184A638H18
Q205-Q206	2N696	762A585H01
	Resistors	
R201-R206-R216- R220	68K Ω -½W.	184A763H71
R202-R204-R208- R209-R211-R214- R217-R221-R224	10K Ω -½W.	184A763H51
R203	10K Ω - 1W	187A643H51
R205-R218-R219- R222	33K Ω -½W.	184A763H63
R207	1K Ω -½W.	184A763H27



* *Fig. 2. Internal Schematic of Type STU-9 Relay for TCF Frequency Shift Carrier Channel*

R210 - R223	12K Ω -½W.	184A763H53
R212 - R225	3.3K Ω -½W.	184A763H39
R213 - R215	22K Ω -½W.	184A763H59

Zener Diodes

Z201	IN3686B 20V	185A212H06
Z202	IN957B 6.8V	186A797H06

Alarm Unit

AL	Telephone Relay	408C062H07

TRIP BOARD

Capacitors

C251 - C252	.25 uf	187A624H02

Diodes

D251 to D255	IN457A	184A855H07
D252 to D253 (when used)	IN457A	184A855H07

Transistors

Q251 - Q252	2N696	762A585H01
Q253	2N699	184A638H19
Q254 (when used)	2N2043	184A638H21

Resistors

R251 - R252 - R257	10K Ω -½W.	184A763H51
R253 - R255	33K Ω -½W.	184A763H63
R254 - R256	68K Ω -½W.	184A763H71
R258	10K Ω -1W.	184A643H51
R259	800 Ω -3W.	184A859H06
R260 (when used)	1K Ω -½W.	184A763H27
R261 (when used)	10K Ω -½W.	184A763H51

AR Unit

AR (when used)	3NO - INC contacts	408C845G23
AR (when used)	4NO - contacts	408C845G13
AR (when used)	2NO - 2NC contacts	408C845G09

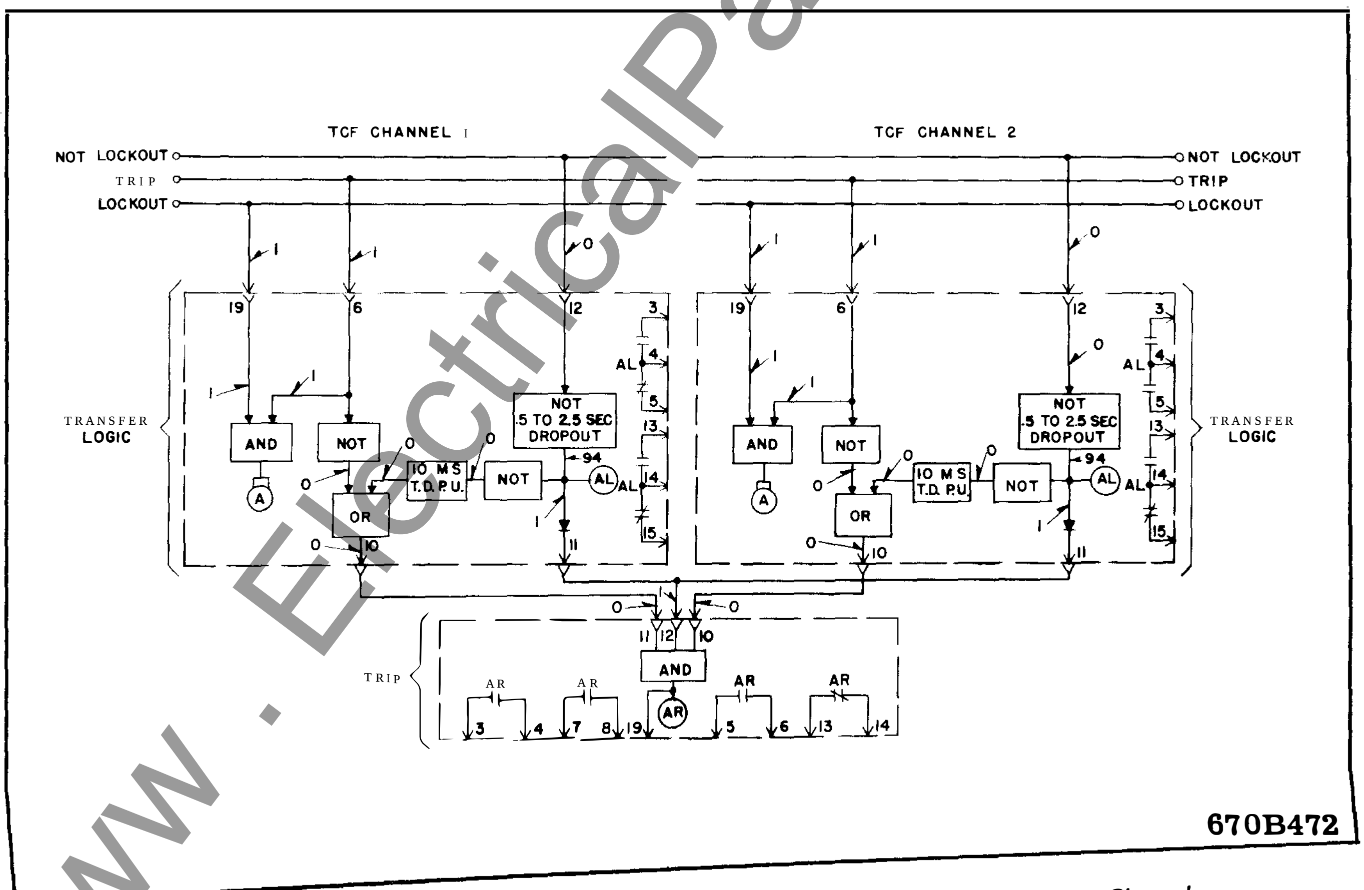


Fig. 3. Logic Diagram of Type STU-9 Relay for TCF Frequency Shift Carrier Channel

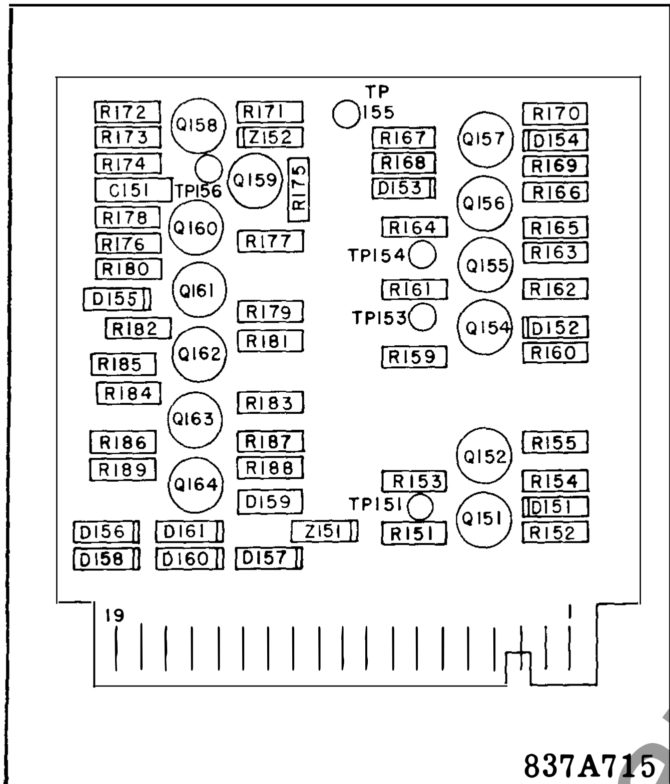


Fig. 5 Component Locations on the Interface Logic Board

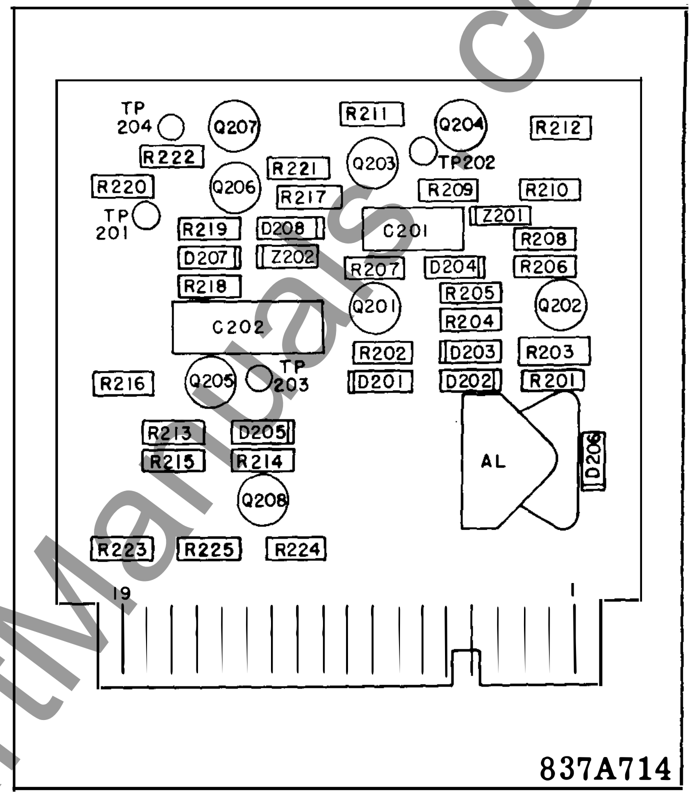


Fig. 6. Component Location on the Transfer Logic Board

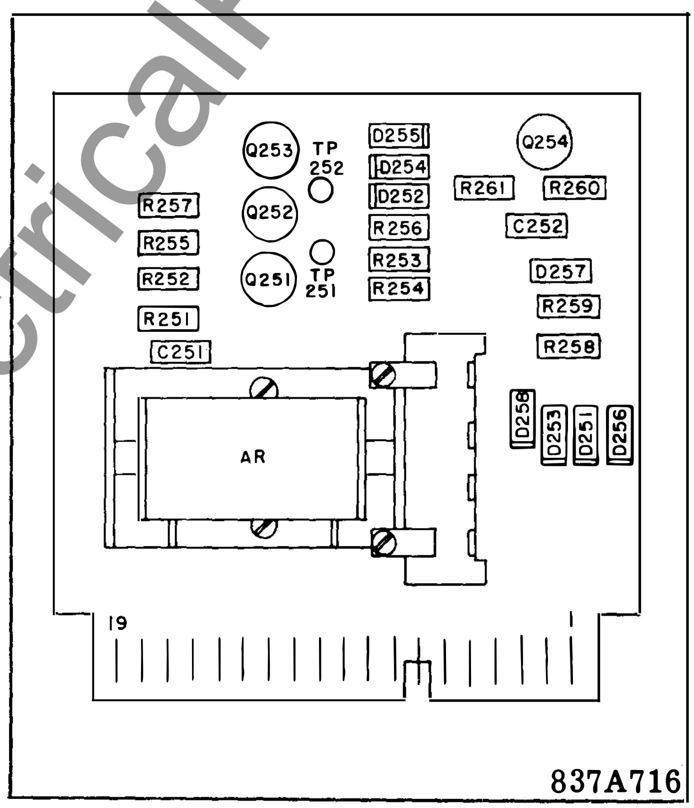
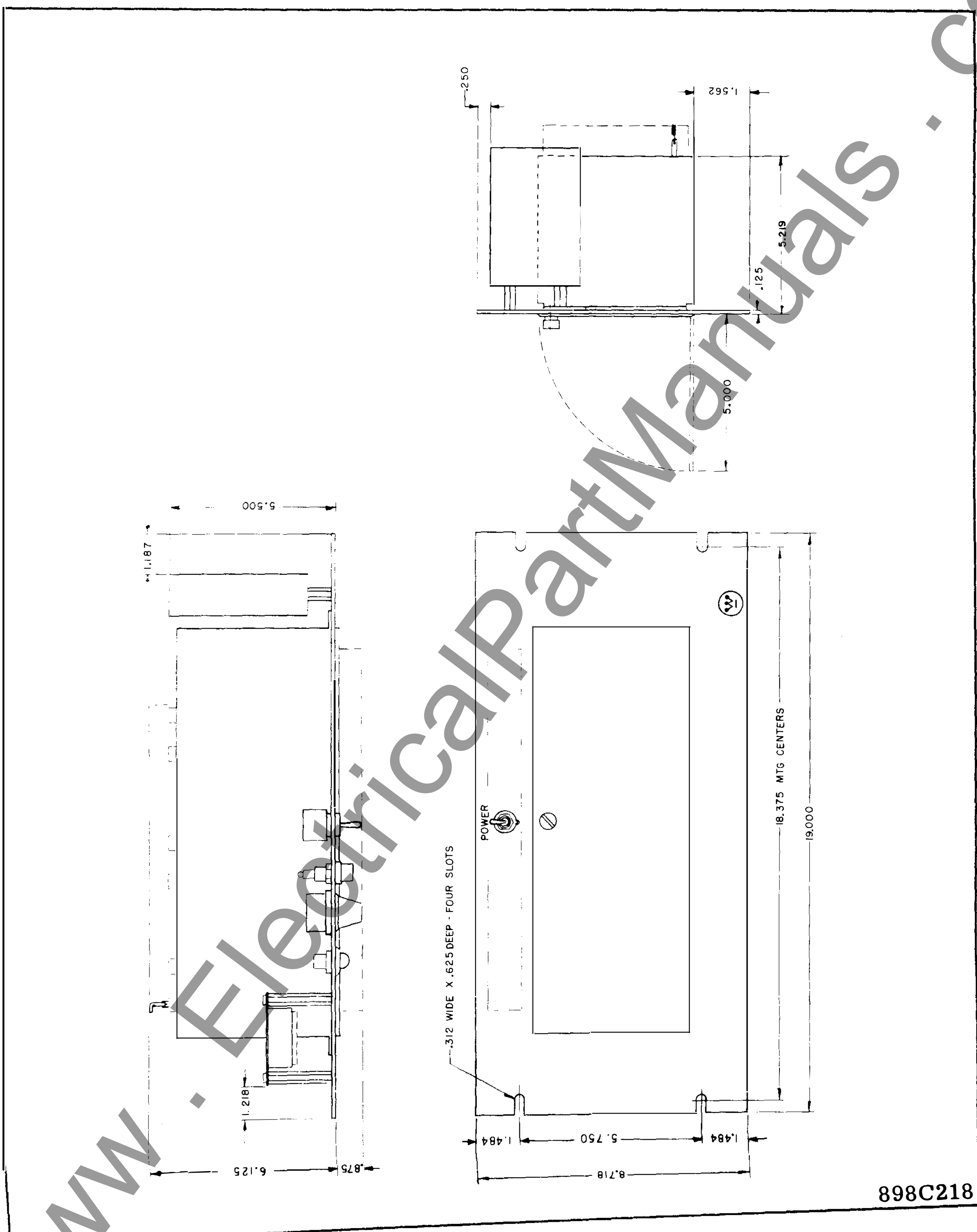


Fig. 7. Component Location on the Trip Board



898C218

Fig. 8. *Outline and Drilling Plan for the Type STU-9 Relay*

WESTINGHOUSE ELECTRIC CORPORATION

RELAY-INSTRUMENT DIVISION **NEWARK, N. J.**

Printed in U.S.A.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE TT-9 AUXILIARY RELAY

CAUTION Before putting relays into service, remove all blocking which may have been inserted for the purpose of securing the parts during shipment, make sure that all moving parts operate freely, inspect the contacts to see that they are clean and close properly, and operate the relay to check the settings and electrical connections.

APPLICATION

The type TT-9 relay is an auxiliary relay used in transfer trip relaying, such as would be used to trip a remote breaker for a transformer fault at a station where no high voltage breaker is used. It can be used in conjunction with single channel or dual channel equipment.

CONSTRUCTION

The type TT-9 relay consists of one lockout unit, two blocking diodes, and one indicating contactor switch.

Lockout Unit - LO

The lockout unit LC is a telephone type relay. In this relay, an electromagnet attracts a right-angle iron bracket which in turn operates a set of make and break contacts.

The lockout unit is of slow release type. The delay in release is obtained by a copper slug located at the end opposite from the armature. When the coil becomes de-energized, the change in flux through the slug results in an electromotive force and associated current in it. This current produces a flux which aids the main flux and delays the release of the armature. When the coil is energized, the operation of the relay is not appreciably delayed because the armature is operated by flux not linking the slug.

Blocking Diodes

Blocking diodes are zener type silicon rectifiers.

Indicating Contactor Switch (ICS)

The indicator is a small d-c operated clapper type device. A magnetic armature is attracted to the magnetic core upon energization of the switch. During this operation two fingers on the armature deflect a spring located on the front of the switch, which allows the operation indicator to drop. Also during this operation, moving contacts bridge two stationary contacts completing trip circuit. The target is reset from outside the case by pushrod located at the bottom of the cover.

OPERATION

Lockout Unit - LO

The lockout unit is energized by a 94G contact. One contact of LO-unit is in trip circuit, a second contact is in alarm circuit and a third one is in series with the trip relay contact (94T).

Blocking Diode

The diode in series with the lockout relay coil is used to block an undesirable path to the indicating lamp under normal system conditions. Without the diode, a path would be present from the station battery positive through 94G and LO-contacts to energize the indicating light. The diode is a zener type diode rated at one watt, 200 volts (J.E.D.E.C. No. IN3051).

CHARACTERISTICS

The various characteristics of the various units of the relay are as follows:

	48V Ohms	125V Ohms	250V Ohms
LO Unit Coil	1300	1300	1300
LO-Series Resistor	- -	5000* †	15000 †

LO unit pickup time — less than 1.5 cycles.
LO unit dropout time — 4 cycles.
† Adjustable

SUPERSEDES I.L. 41-959.1B
*Denotes changes from superseded issue.

EFFECTIVE DECEMBER 1968

SETTINGS

Lockout Unit

The telephone relay requires correct setting for the correct control voltage. For 48V d-c, the series resistor is bypassed by connecting the lead to the rear terminal of the resistor. For 125V d-c or 250V d-c rated relays the connection is made to the adjust terminal of the series resistor.

INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration, and heat. Mount the relay vertically by means of the four mounting holes on the flange for semi-flush mounting or by means of the rear mounting stud or studs for projection mounting. Either a mounting stud or the mounting screws may be utilized for grounding the relay. The electrical connections may be made directly to the terminals by means of screws for steel panel mounting or to the terminal studs furnished with the relay for thick panel mounting. The terminal studs may be easily removed or inserted by locking two nuts on the stud and then turning the proper nut with a wrench. For detailed information, refer to IL.41-076.

ADJUSTMENTS AND MAINTENANCE

The proper adjustments to insure correct operation of this relay have been made at the factory. Upon receipt of the relay, no customer adjustments other than those covered under "SETTINGS" should be required.

Acceptance Check

The following check is recommended to insure that the relay is in proper working order.

A. Indicating Contactor Switch

Apply direct current to the relay terminals. The indicating switch should pick up and drop the indicator target between 1 - 1.2 amp.

B. Lockout Unit - LO

Apply rated voltage to the lockout unit and observe contact action. If desired, the timing of the operation can be checked as outlined under calibration procedure.

Routine Maintenance

All relays should be inspected periodically and the operation should be checked at least once every year or at such other time intervals as may be dictated by experience to be suitable to the particular application.

All contacts should be periodically cleaned. A contact burnisher S#182A836H01 is recommended for this purpose. The use of abrasive material for cleaning contacts is not recommended because of the danger of embedding small particles in the face of the soft silver and thus impairing the contact.

NOTE When making a dielectric test on the relay, the high voltage may be applied at the relay terminals, from all circuits to ground, between coil and contact circuits, and between isolated coil circuits. However, the test voltage should not be applied across relay contacts and rectifier circuits.

Use the following procedure for calibrating the relay if the relay has been taken apart for repairs or the adjustments have been disturbed. This procedure should not be used unless it is apparent that the relay is not in proper working order.

Calibration Procedure

A. Lockout Unit - LO

The operating time of LO should be checked with an electronic timer.

For 125V d-c or 250V d-c control voltage, the coil of the relay should be connected in series with the internal resistor. This resistance should be set initially for:

3500 ohms ± 10% for 125V d-c
12000 ohms ± 10% for 250V d-c

With the armature closed, adjust the air gap to be .002" - .003". Contact gaps should measure from .020" to .035". The coil is energized across terminals 6 and 9.

Check for the specified 4 cycles dropout time across terminals 4 and 5. If necessary, the dropout time can be adjusted by changing the air gap. After final adjustment, the air gap should be a minimum of .002". Check pickup. It should be below 1.5 cps. If necessary, adjust series resistor.

B. Zener Blocking Diode (For 48, 125, and 250 Volts Relays)

The zener type blocking diodes have a one watt, 200 volt rating (JEDEC No. IN3051, two diodes in series used on 250 volt relays).

1. Reverse Characteristics:

Breakdown voltage is the value of voltage at which the current just exceeds 0.25 milliamperes and should be between 160 to 240 volts for each diode. The breakdown voltage is determined by slowly increasing voltage until reverse current exceeds 0.25 milliamperes and starts to increase rapidly. Do not exceed 3 milliamperes reverse current.

2. Forward Characteristic:

With 200 milliamperes flowing in forward direction, the forward voltage across each diode should not exceed 1.5 volts.

C. Indicating Contactor Switch

Pass sufficient d-c current through the trip circuit to close the contacts of the ICS. This value of current should be between 1.0 - 1.2 amp. The operation indicator target should drop freely. The contact gap should be approximately .047'' between the bridging moving contact and the adjustable stationary contacts. The bridging moving contact should touch both stationary contacts simultaneously.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data.

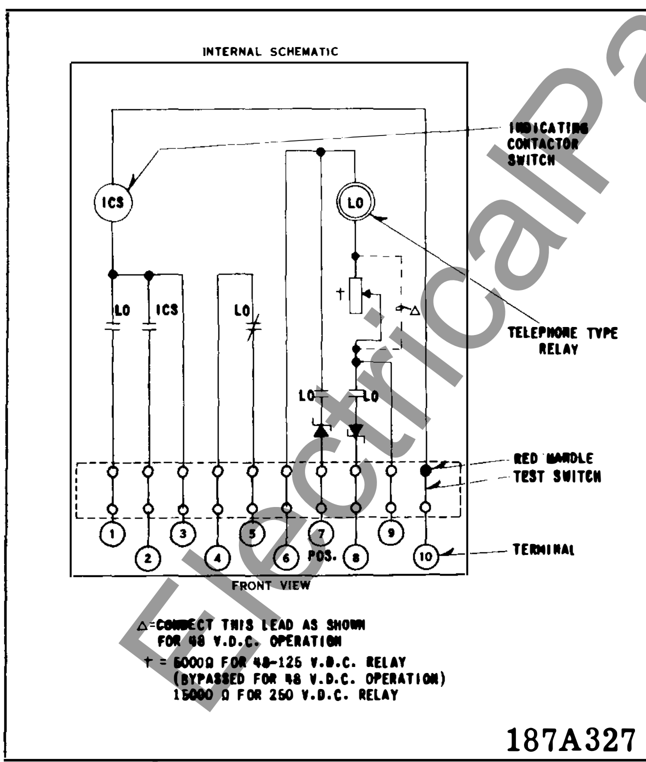
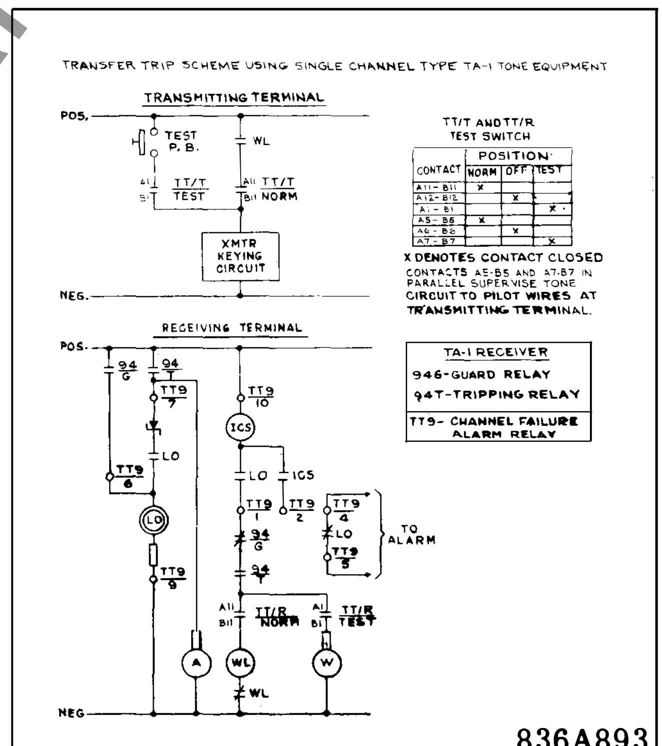
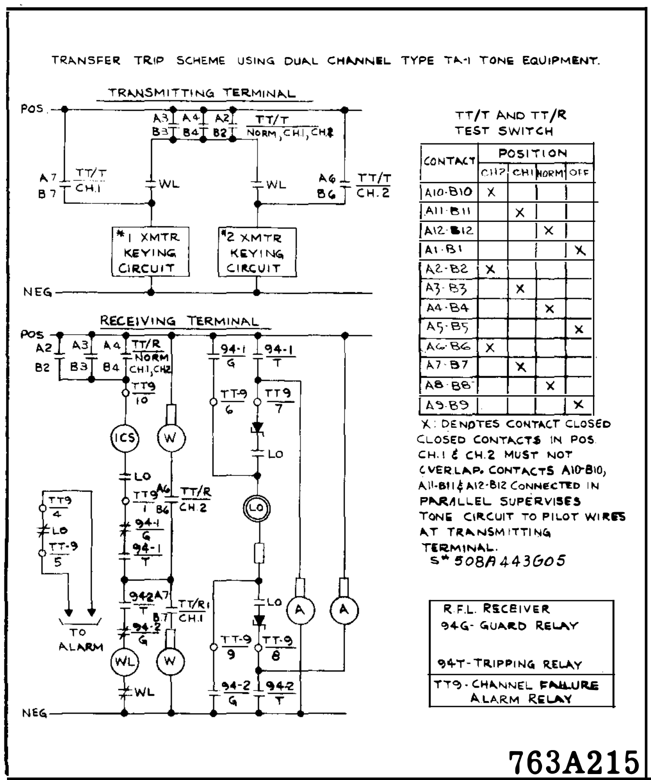


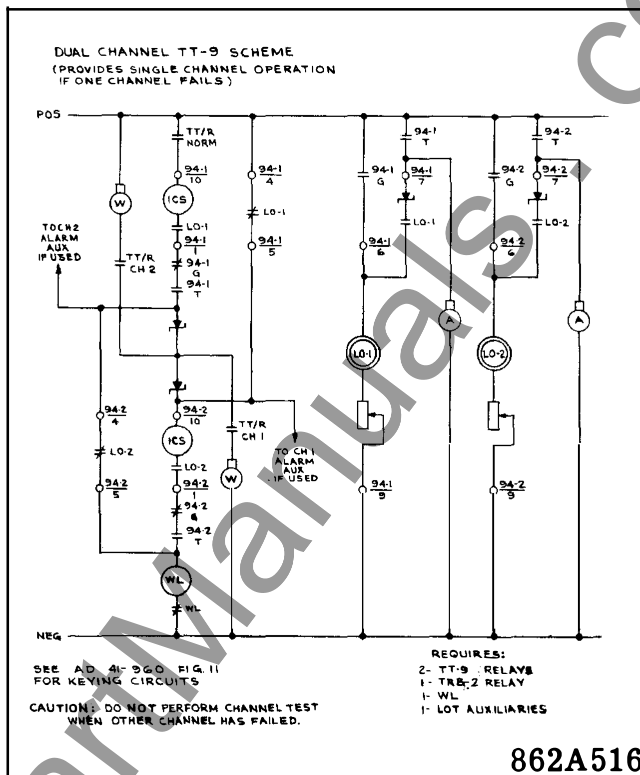
Fig. 1 Internal Schematic for TT-9 Auxiliary Relay in FT-11 case.



* *Fig. 2 Transfer Trip Scheme using single channel with TT-9 Relay.*



* *Fig. 3 Transfer Trip Scheme using dual channel with TT-9 Relay.*



* *Fig. 4 Transfer trip scheme using dual channel, with a single channel operation if one channel fails, with TT9 Relay.*

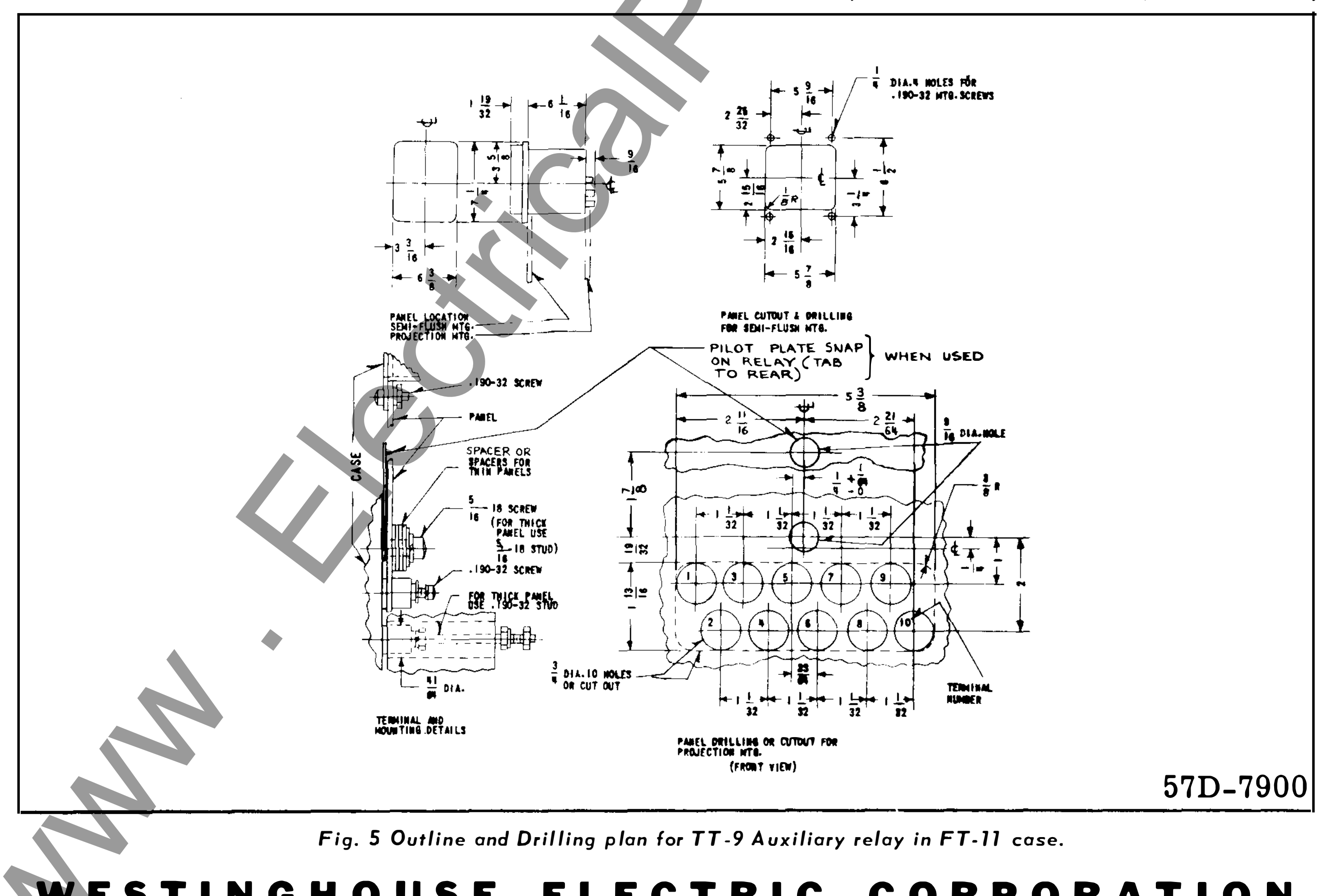


Fig. 5 Outline and Drilling plan for TT-9 Auxiliary relay in FT-11 case.

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INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE STU UNBLOCK RELAY FOR USE WITH SOLID STATE RELAY

CAUTION: It is recommended that the user of this equipment become thoroughly acquainted with the information in these instructions before energizing this relay. Failure to observe this precaution may result in damage to the equipment. If the equipment is mounted in a cabinet, the cabinet must be bolted down to the floor or otherwise secured before swinging out the equipment rack to prevent its tipping over.

APPLICATION

The type STU relay is a completely solid-state carrier unblock auxiliary relay for use with solid-state relays and a type TCF frequency shift channel to prevent tripping for faults external to the line section to which it is applied and to permit instantaneous and simultaneous tripping for internal faults. The relay is arranged to respond to indications of fault direction, distance and power provided by the phase and ground distance, and overcurrent relays thereby controlling the transmission of an unblocking or trip signal and the initiation of high speed tripping for internal faults. Either two or three terminal line applications may be used.

CONSTRUCTION

The STU relay is mounted on a standard 19" wide panel, 8-3/4" high (5 rack units) with edge slots for mounting on a standard relay rack or panel. All components not on printed circuit boards are mounted on the panel and extend to the rear. For the outline and drilling plan, refer to Fig. 8.

All of the circuitry suitable for printed circuit board mounting is contained in an enclosure that projects from the rear of the panel and is accessible by opening the door on the front. The dotted lines enclosing separate areas of Fig. 1 indicate that the components thus enclosed are all on the same printed circuit board.

The printed circuit boards slide into position in slotted guides at the top and bottom of the enclosure, and the board terminals engage a terminal block at the rear of the compartment. Each board and terminal block are keyed so that if a board is placed in the wrong compartment, it cannot be inserted into the terminal block. The printed circuit boards are labeled from left to right respectively: Protective Relay Interface, Timing, Channel, Arming, Output and Test.

SUPERSEDES I. L. 41-959
* Denotes change from superseded issue.

EFFECTIVE AUGUST 1969

A board extender (Style No. 644B315G01) is available for facilitating circuit voltage measurements or major adjustments. After withdrawing any one of the circuit boards, the extender is inserted in that compartment. The board then is inserted into the terminal block on the front of the extender. This restores all circuit connections; and all components, test points and printed circuit terminals are readily accessible.

* Most of the relay operates from a zener regulated 20 volts d-c supply (Z1 on Fig. 1) which is mounted on a heatsink at the rear of the panel. The 20 volt zener and a portion of the relay works from a 45 volt d-c input supply. External connections to the relay are made through a 32 terminal circuit receptacle, J101 in Fig. 1.

SYSTEM OPERATION

The type STU unblock relay is used in a directional unblock relay scheme for power line protection. High-speed tripping is obtained for two or three terminal line applications for faults anywhere in the protected line. The signals to which the STU relay responds are obtained from the receiver of the TCF frequency shift channel and the output of the local protective relays.

Since distance relays may operate on a loss of a-c potential, the STU relay provides alarm and lockout of tripping 3000 milliseconds after this condition occurs. The 3000/100 MS timer picks up and the output from NOT 1 drops out an AL loss of potential alarm mounted elsewhere in the relaying system. This also prevents output from A 2 since there is no signal from NOT 1.

The output of A 2 initiates keying of the local transmitter through operation of OR 2, by shifting the transmitter from the blocking frequency to the unblocking or trip frequency. In 10 milliseconds after a primary pilot trip operation, the 10/150-400 millisecond timer picks up and also maintains the unblocking frequency keying for 150 to 400 milliseconds after a loss of the trip signal. This time is adjustable to allow for the breaker failure timer setting at the remote terminal.

In addition, the 52b contact initiates the trip frequency transmission 30 milliseconds after the local circuit breaker opens and until such time as the circuit breaker is reclosed. The 30/0 millisecond timer delays the transmission of trip frequency to obtain coordination for bus fault tripping of the local circuit breaker where tripping of the remote breaker would be incorrect and might cause undesired interruption to tapped transformer terminals. Transmission of the trip or unblocking frequency is necessary to permit tripping of the remote terminal should the remote circuit breaker be closed into a fault or should a fault develop in the protected line while the local circuit breaker is open.

Internal Fault

* The operation of any or all the protective relays PR-1, PR-2 or PR-3 for an Internal Fault perform the following (refer to the block diagram, Fig. 2):

1. Energizes the 3 second timer and A2 thereby giving an output from A2 for up to 3 seconds.

2. "Arms" A6 or puts it in a "ready" condition for up to 3 seconds by removing a blocking bias voltage.

3. Energize the transient blocking circuit at OR 4 up to 3 seconds.

4. Key the TCF transmitter for 3 seconds through OR 2 to shift the frequency from a blocking to an unblocking or trip condition.

For an internal fault, the TCF Receivers will produce a "1" output unblock signal to energize A1 thereby producing a "1" input from the channel to A3. This together with the signal from PR-1, PR-2 or PR-3 at A3 will cause tripping 2 milliseconds later. This operation will be completed before the transient blocking becomes effective.

External Fault

If no unblocking or trip signal is received from the remote terminal when PR-1, PR-2, or PR-3 operates (as for an External Fault), there will be no tripping output from A1. If tripping does not take place within 25 milliseconds after the protective relays operate, the transient blocking circuit energized through OR 4 will desensitize A6 to prevent possible undesired tripping during transients occurring at the clearing (elsewhere) of an external fault.

The above procedure also holds true if the TCF unblocking or trip signals are received from the remote terminals and the protective relays do not operate. This also is an external fault.

Sequential Faults

Occasionally an External Fault will be followed by an internal fault before the former is cleared. In order to prevent a long delay in clearing such an internal fault, a "transient unblocking" feature is included. Although transient blocking has been set up by the initial external fault, the presence of an Internal Fault will cause an output from A3 which will energize the transient unblocking circuit. After 25 milliseconds, A6 will be resensitized and tripping will be permitted.

RELAY OPERATION

The complete detailed relay circuit is shown on the internal schematic, Fig. 1. The operation of the logic elements shown on Fig. 2, and the individual circuit components will be described in the following paragraphs.

Protective Relay Interface Board

The Protective Relay printed circuit board contains the required circuits for interface with the protective relays, PR-1, PR-2 and PR-3. These logic blocks are the protective relay input OR 1 and its associated Buffer B3, for surge protection, the 3000/100 millisecond time delay for loss of a-c potential, and A2.

Under normal conditions, J101 terminals 30, 31 and 32, the inputs to the STU relay from PR-1, PR-2 and PR-3 respectively, are held at negative (zero volts) thereby holding transistor Q101, the output of B3, non-conductive. With Q101 off, transistors Q102 and Q109 have base drive holding them both conductive. Since Q109 is turned on, this represents a "0" output from A2. Transistor Q107 is normally on representing a "1" signal from NOT 1 to the AL loss of potential alarm elsewhere in the relaying system.

When one or more of the protective relays, PR-1, PR-2 or PR-3 operate and positive 20 volts d-c is applied to J101 terminals 30, 31 or 32, then transistor Q101 will conduct and immediately turn off Q102 and Q109. Transistor Q109 is the output stage of A2, and for A2 to assume a "1" output, both transistors Q101 (output of buffer B3) and Q108 (output of NOT 1) must be conducting thereby holding Q109 non-conductive. Therefore, immediately following reception of a protective relay "1" signal, A2 will yield a "1" output.

Transistors Q102 to Q105 are associated with the 3000/100 millisecond time delay, and Q106 to Q108 with NOT 1. Normally, transistors Q102, Q104, Q107 and Q108 are conducting and Q103 and Q105 non-conductive. Therefore, capacitor C102 in the three (3) second timer is fully discharged through transistor Q104. Since Q108 is conducting, this represents a "1" input to A2 from NOT 1.

Since distance relays may operate on loss of a-c potential, the 3000/100 millisecond timer provides alarm and blocks A2 three (3) seconds after loss of primary protection and blown a-c potential fuse. As mentioned above, output from any or all the protective relays turns off transistor Q102. Therefore, providing the timer disable switch between J101 terminals 12 and 13 is closed, transistor Q103 has base drive to cause it to conduct and turn off transistor Q104. When this occurs, capacitor C102 will begin to charge from positive 20 volt d-c through resistors R114 and R116 and, in 3000 milliseconds, reaches a sufficient potential to breakdown zener diode Z103 and cause transistor Q105 to conduct. With Q105 conducting, base drive is removed from transistors Q106 and Q108 to make them non-conductive. Therefore, with Q108 off, the "1" input from NOT 1 becomes a "0" and blocks A2. In addition, since Q106 is off, no base drive is available for Q107 so it becomes non-conductive and provides a "0" signal to the AL alarm for indication of loss of a-c potential. Upon loss of the protective relay signal, transistor Q104 will turn on and permit capacitor C102 to discharge in 100 milliseconds below the breakdown of zener diode Z103 and turn off transistor Q105.

Timing Board

The Timing printed circuit board contains two time delays necessary for proper operation of the relaying system: one, the 30/0 millisecond timer used for coordination with bus fault and remote breaker tripping; and, two, the 10/150-400 millisecond signal continuing timer used for coordination with the breaker failure timer.

Under normal conditions, transistor Q201, the output of Buffer circuit B4, and the input to the 30/0 timer, is non-conductive thereby preventing a path for base current to turn on transistor Q202. As a result, printed circuit terminal #14 is held at negative (zero volts) representing a "0" output from this timer.

After the local circuit breaker opens, positive 125 volt d-c is applied through the now closed 52b contact to J101 terminal No. 20. When this occurs, transistor Q201 has base drive and immediately becomes conductive. As a result, capacitor C202 starts charging to negative through resistor R207 and the collector-emitter circuit of Q201, and in 30 milliseconds, C202 assumes a low enough potential below positive 20 Vdc to breakdown zender diode Z203 and provide a path for base drive to make transistor Q202 conductive. Therefore, with Q202 conducting, this represents a "1" signal to OR 2 to shift the transmitter from a blocking to an unblocking or trip frequency. Upon breaker reclosing, the 52b contact opens turning transistor Q201 off thus permitting capacitor C102 to rapidly discharge for immediate dropout.

The 10/150-400 millisecond time delay operates similar to the 30/0 MS timer. After a primary pilot trip operation, capacitors C203 and C204 will charge in milliseconds through diode D202, resistor R212 and the collector-emitter circuit of transistor Q203 to a low enough potential to cause breakdown of zener diode Z204 and conduction of transistor Q204. Once Q204 turns on, a "1" signal to OR 2 keys the transmitter to the trip frequency for the duration of the pilot trip signal. After loss of the pilot trip signal, capacitors C203 and C204 will discharge in 150 to 400 milliseconds (adjustable by resistor R214) and turn Q204 off. This 150 to 400 MS dropout time holds the unblocking or trip frequency on to provide coordination with the breaker failure timer. Normal dropout time is factory calibrated at 300 milliseconds.

Channel Interface Board

The channel printed circuit board contains A2 and its associated Buffers B1 and B2 for interface with the TCF Receiver, and OR 2 for interface with the TCF Transmitter.

Under normal conditions and for three-terminal line applications, both J101 terminals 8 (TCF RCVR-1) and 7 (TCF RCVR-2) are held at negative (zero volts) thereby allowing no base drive for transistors Q151 and Q152 thus holding them non-conductive. As a result, transistor Q153 has base drive, so it is normally conducting and represents a "0" output from A1.

When both of the TCF Receivers receive the unblocking or trip frequency from the other terminals, they will produce a positive 20 Vdc potential at J101 terminals 8 and 7. When this occurs, both transistors Q151 and Q152 have base drive and start conducting. In turn, with both Q151 and Q152 on, base drive is removed from transistor Q153 which them stops conducting and represents a "1" output signal from A1. If only one of the TCF Receivers yield a trip output, then transistor Q153 still will receive base drive from the other input transistor in the STU and a "0" signal will be received from A1.

In the case of two-terminal line applications, either J101 terminal 8 or 7 must be connected to J101 terminal 4 to simulate having a constant signal of "1" at one of the A1 inputs. Under this condition, transistor Q153 will still be normally conducting thus representing a "0" output from A1. When the J101 terminal (either 8 or 7) not connected to J101 terminal 4 receives a positive 20 Vdc signal from the TCF, transistor Q153 will lose its base drive and turn off to produce a "1" output from A1.

Under normal conditions, the inputs to OR 2 printed circuit terminals #14, 15 and 16 on the Channel Board are held at negative (0 volts) thereby preventing any base drive from turning on transistors Q154, and thus Q155. When one or more of these printed circuit terminals receive a positive d-c signal, "1", base drive will turn on transistor Q154 which in turn will make transistor Q155 conduct and apply positive 45 Vdc to the TCF transmitter to cause it to shift from the block to the unblock or trip frequency. As can be seen from Fig. 2, in order for the TCF transmitter to be keyed, OR 2 must receive a positive going "1" signal from A2, the 30/0 timer or the 10/150-400 timer.

Arming Board

The Arming printed circuit board contains the logic blocks which combine the information from the protective relays and the channel receiver and in turn provides the proper interfaces for this information to be translated to the Output Board for transient block, arm, transient unblock and pilot trip.

Normally, there is a "0" signal to OR 4 from A1 (printed circuit terminal #12) and from A2 (printed circuit terminal #14) thereby resulting in a "0" signal at printed circuit terminal #9, the output of OR 4. When either or both A1 and A2 yield a "1" output signal to the inputs of OR 4, current is allowed to flow through resistor R287 and diode D264 (for an A1 output) or resistor R288 and diode D265 (for an A2 output). In this case, therefore, a "1" is received from OR 4 to energize the transient block circuitry in the Output Board.

Likewise, both inputs into A3 are normally "0". The input transistors of A3 are Q255 for A1 and Q254 for A2. Normally both Q255 and Q254 have no base drive and, as a result, they are both non-conductive. Therefore, the output transistor of A3, Q256, has base drive and is turned on thus allowing Q254 to conduct and provide a proper interface with the Output Board. If a "1" signal is received from both A1 and A2, then both transistors Q255 and Q254 become conductive thereby removing base drive to Q256 to turn it off. This causes Q257 to stop conducting and allow the 2/0 timer and the transient unblock circuits in the Output Board to function. If either Q255 or Q254 remains non-conductive, then transistor Q257 will stay on and a "0" output will be received from A3.

The Arm circuit is energized from A2 and under normal conditions with a "0" output from A2, there is no base drive from transistor Q258, so it is non-conductive. As a result, with Q258 off, base drive holds transistor Q259 conducting thereby keeping the Output Board "disarmed". As soon as A2 assumes a "1" output state, base drive turns transistor Q258 on and thereby Q259 turns off and arms A6 on the Output Board.

Output Board

The Output Board contains all the logic required for final tripping, transient blocking and transient unblocking. In reference to Fig. 2, a "1" signal from OR 4 represents a transient blocking signal. A "1" output from A3 is a pilot tripping signal in two milliseconds but prior to tripping, it is a transient unblocking signal in the event that transient blocking has already occurred.

The 2/0 millisecond time delay circuit is used to prevent tripping from improper signals of short duration. Normally, printed circuit terminal #6 is held at positive 20 Vdc thereby preventing capacitor C306, associated with the

2/0 MS timer, from charging. Under conditions for tripping, transistor Q257 in A3 (Arming Board) will turn off and allow capacitor C306 to charge to negative through resistors R318 (Output Board) and R279 (Arming Board). After the factory calibrated time (by S1) of two milliseconds, the voltage across C306, which is applied to the base emitter circuit of transistor Q305 in A6, is sufficient to cause Q305 to operate and thereby turn transistor Q306 off providing it is armed.

The 2/0 millisecond timer has no intentional reset time delay. If a tripping condition is indicated for some time less than two (2) milliseconds, such as during a reversal of fault power flow, as soon as transistor Q257 in A3 again conducts, capacitor C306 will rapidly discharge through the collector emitter circuitry of Q257, diode D261 and resistor R318. This rapid resetting of the 2/0 timer prevents possible "notching up" of the charge on C306 during momentary and intermittent interruptions under normal conditions.

The A6 circuit block consists of transistors Q305 and Q306 and the associated components. Under normal conditions, transistor Q305 is non-conducting and Q306 fully conducting. The base of Q306 is held well below its emitter potential by means of the arming circuitry voltage divider consisting of resistors R324, R335, diode D308 and transistor Q259. With this bias, transistor Q306 is held in saturation and is desensitized so that even if a tripping voltage were applied to Q305, transistor Q306 would not turn off. This desensitizing circuit is an arrangement to prevent inadvertent operation of A6 caused by surges on the d-c system. As long as Q306 is conducting, its collector is at a high enough potential above negative d-c so that transistor Q307 in the tripping amplifier cannot turn on.

Upon occurrence of an internal fault, transistor Q259 in the Arming Board turns off thereby removing the desensitizing bias from Q306 by open-circuiting the path of current through diode D308 and resistor R335. This causes A6 to become "armed" and in a ready condition for a tripping operation. After a two (2) millisecond time delay, the potential across capacitor C306 is sufficient to cause Q305 to conduct and thus turn off Q306. When Q306 is no longer conducting, the potential of its collector circuit drops to a relatively low value and allows sufficient voltage to appear across the base-emitter circuit of transistor Q307 in the trip amplifier, causing it to become conductive. In turn, transistors Q308 and Q309 turn on and apply a pilot trip voltage output.

The transient blocking circuit is energized only when there is an output from OR 4. An output from OR 4 consists of a positive potential which immediately turns on transistor Q302 thus dropping its collector potential (at TP 303) to a very low value. Therefore, the positive voltage is removed from the base of transistor Q303 turning it off. When this occurs, capacitor C305 charges in 25 milliseconds to a potential which is sufficient to cause the breakdown of zener diode Z303 and provide a path for base current to turn on transistor Q304. With Q304 on, a conducting path through resistors R324, R323, diode D306 and the collector-emitter circuit of Q304 is provided in order to hold a desensitizing bias on transistor Q306 in A6. Thus, the transient blocking circuitry allows 25 milliseconds after the operation of either a protective relay or the reception of a TCF trip signal for a "1" to be received from A6. If tripping does not occur in this time, as during an external fault, operation of the transient blocking circuit will hold A6 desensitized in order to prevent undesirable operation during transients associated with power reversals on the protected line or at the clearing of an external fault.

If an internal fault occurs before the external fault is cleared, it is desirable to obtain high-speed tripping. The transient unblocking circuitry permits this since transistor Q257 in A3 will turn off and remove the positive 20 Vdc potential on printed circuit terminal #10. This allows capacitor C301 to charge to negative through diode D301, resistor R314 and the collector-emitter circuit of transistor Q304, which has been turned on due to transient blocking. In 25 milliseconds, C301 will charge to a sufficient potential to turn on transistor Q301 and permit base drive for transistor Q303. This will immediately turn on Q303 which allows a path for rapid discharge of capacitor C305. When this occurs, zener diode Z303 will not breakdown, and Q304 will stop conducting thereby interrupting the desensitizing circuit from the base of transistor Q306. Therefore A6 will be able to assume a "1" output and provide tripping after a delay of only 25 milliseconds.

Test Board

The Test Board contains two potentiometers, S1 and S2, used for factory time delay adjustments. Also, six test points are easily accessible from the front of this board for facilitating system tests of the STU Relay.

Potentiometer S1 is the 2/0 millisecond time delay adjustment, and S2 is the 25/0 transient unblocking time delay adjustment. These potentiometers are used only for factory calibration of the STU Relay.

Listed below are the six test points on the Test Board. Test points 1 to 5 are red, and test point 6 is black.

1. Pilot Trip
2. Transient Block
3. Arm - Received Protective Relay
4. Received Channel
5. Transmitter Key
6. Negative DC

CHARACTERISTICS

Input Voltage	45 volts D-C
Current Drain	100 milliamperes maximum
Pilot Trip Output	10 milliamperes at positive 20 Vdc
Min. Operate Time	2 milliseconds
Keying Voltage	Positive 45 volt D-C
Blown A-C Fuse Detection Timer	3 seconds
Ambient Temperature Range	$-20^{\circ}C$ to $+55^{\circ}C$ around chassis

Dimensions	panel height: 8-3/4" or 5 R.U. panel width: 19" panel depth: 6"
Weight	approximately 9 pounds

SETTINGS

Normally, there are no settings to be made on the STU unblock relay. All various time delay circuits are factory adjusted to the stated time in Fig. 2. However, if conditions require, the dropout time of the 10/150-400 millisecond timer may be changed from the factory setting of 300 MS to any value between 150 and 400 MS as explained under the Calibration section.

INSTALLATION

The STU Relay is generally supplied on a relay rack as part of a complete relay system assembly. The location must be free from dust, excessive humidity, vibration, corrosive fumes or heat. The maximum ambient temperature around the chassis must not exceed 55°C.

The outline and drilling plan of the STU Relay is shown in Fig. 8.

ADJUSTMENT AND MAINTENANCE

A. Acceptance Test

The operation of the STU Unblock Relay can be checked by taking voltage measurements at the six (6) test points on the Test Board. Energize the STU Relay with 45 Vdc and measure the positive d-c voltages on test points 1 to 5 with respect to negative d-c, test point 6, under the following conditions:

Note: In reference to Fig. 1, use the timer disable switch (between J101 terminals 12 and 13) closed unless otherwise noted in tests below.

1. Normal Condition.	Test Point 1 - 0 Vdc Test Point 2 - 19 Vdc Test Point 3 - less than 0.5 Vdc Test Point 4 - less than 0.5 Vdc Test Point 5 - 0 Vdc
2. Protective Relay Operation. (Open timer disable switch) (Apply positive 20 Vdc to J101 terminal 30)	Test Point 1 - 0 Vdc Test Point 2 - less than 0.5 Vdc Test Point 3 - 19 Vdc Test Point 4 - less than 0.5 Vdc Test Point 5 - 45 Vdc
3. Channel Receiver Operation. (Apply positive 20 Vdc to J101 terminals 8 and 9)	Test Point 1 - 0 Vdc Test Point 2 - less than 0.5 Vdc Test Point 3 - less than 0.5 Vdc Test Point 4 - 7 Vdc Test Point 5 - 0 Vdc

4. Protective Relay and Channel Operation. (Apply pos. 20 Vdc to J101 terminals 8 and 9. Then apply pos. 20 Vdc to J101, terminal 30)

Test Point 1 - immed. 20 Vdc, in 3 sec. 0 Vdc

Test Point 2 - immed. 19 Vdc, in 3 sec. less than 0.5 Vdc

Test Point 3 - immed. 19 Vdc, in 3 sec. less than 0.5 Vdc

Test Point 4 - immed. 7 Vdc, in 3 sec. 7 Vdc

Test Point 5 - immed. 45 Vdc, in 3 sec. 0 Vdc

B. Recommended Routine Maintenance

Periodic checks of the relaying system are desirable to indicate impending failure so that the equipment can be taken out of service for correction. Any accumulated dust should be removed at regular maintenance intervals.

The proper adjustments to insure correct operation of this relay have been made at the factory and should not be disturbed after receipt by the customer. If the adjustments or if the components or printed circuit boards which affect calibration have been changed, then recalibration per the Calibration section following will have to be made on the circuits in question.

C. Calibration

1. 10/150-400 T.D. (Timing Board)

The dropout of the 10/150-400 millisecond signal continuing timer may be adjusted from 150 to 400 MS to allow for various settings of the breaker failure timer. By comparing the Pilot Trip voltage of the relay with the timer output voltage at printed circuit terminal 16 (Timing Board) under dropout conditions, the time delay between a change of the input voltage and the output voltage can be adjusted from 150 to 400 milliseconds. For more dropout time, potentiometer R214 on the Timing Board should be turned clockwise, and for less time it should be turned counter-clockwise. Factory setting of the dropout time is 300 milliseconds. Pickup time can be calibrated in the same manner except for more time, increase resistor R212 and for less time, decrease R212. Pickup time should be 10 milliseconds. Location of potentiometer R214 and resistor R212 can be seen on the Timing Board component location, Fig. 4.

2. 30/0 T.D. (Timing Board)

The pickup time of the 30/0 millisecond timer can be calibrated by comparing the input voltage to Buffer B4 with the output voltage at printed circuit terminal 14, Timing Board, under pickup conditions. Pickup time should be 30 milliseconds. Increase resistor R207 (Timing Board) for more time or decrease R207 for less time. Location of resistor R207 can be seen in Fig. 4.

3. <u>3000/100 T.D. (P. R. Interface Board)</u>

The 3000/100 millisecond time delay can be calibrated by comparing the time duration for a voltage change between the timer input, the output of Buffer B3, and the timer output, printed circuit terminal 14 (P. R. Interface Bd.) under pickup and dropout conditions. Normal pickup time is 3000 milliseconds. For more pickup time, increase resistor R116 and for less time, decrease R116. Dropout time can be calibrated by using a higher value of resistor R115 for more time or a lower value for less time. Normal dropout calibration time is 100 milliseconds. Location of resistors R115 and R116 can be seen on the Protective Relay Board component location, Fig. 3.

4. <u>2/0 MS Timer (Output Board)</u>

In order to calibrate the 2/0 millisecond time delay, connect a jumper across capacitor C305 on the Output Board. Then compare the voltage at test point TP 255 on the Arming Board with the voltage at test point TP 306 on the Output Board under a trip condition. If the time delay between a change in both voltages is not two milliseconds, turn potentiometer S1 on the Test Board clockwise for more time and counter-clockwise for less time. Location of components and test points may be seen in Figs. 6 and 7. After calibration, remove the jumper from capacitor C305 and insure that the locking clamp on S1 is tight.

5. <u>Transient Unblocking 25/0 Time Delay (Output Board)</u>

In order to calibrate the transient unblocking time delay, the STU Relay must be in a transient block state. After putting the relay in a block state, compare the voltage at test point TP 255, Arming Board, with the voltage at Test Point 1, Test Board. If the time delay between a voltage change at the input (TP 255) and output (TP 1) is not 25 milliseconds, then turn potentiometer S2 (Test Board) clockwise for more time and counter-clockwise for less time. Location of TP 255 can be seen in Fig. 6, Arming Board component location.

6. <u>Transient Blocking 25/0 Time Delay (Output Board)</u>

To calibrate the transient blocking time delay, compare the voltage at test point TP 303 on the Output Board with test point 2, Test Board. Apply a transient block signal and if the time delay between a voltage change at the input (TP 303) and output (Test Point 2) is not 25 milliseconds, then turn potentiometer R316 clockwise for more time and counter-clockwise for less time. Location of the potentiometer R316 and test point TP 303 can be seen in Fig. 7.

D. <u>Electrical Checkpoints - Trouble Shooting</u>

The components of the STU Unblock Relay are operated well within their ratings and normally will give long and trouble-free service. However, if a relay has given indication of trouble in service or during routine checks, the voltages tabulated in Table I should be checked to determine the faulty circuit.

Test point voltages for the P. R. Interface, Timing, Channel, Arming, Output and Test printed circuit boards in the STU Unblock Relay are listed in Table I under various system conditions. The exact values will vary from one relay to another but, in general, will be within ±10% between relays. A Board Extender is helpful in checking test point voltages.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data and identify the part by its designation on the internal schematic drawing Fig. 1, as well as all information in the Electrical Parts List.

TABLE I

ELECTRICAL CHECKPOINTS - TROUBLE SHOOTING VOLTAGES

All test point voltages are positive D-C taken with respect to negative, Test Point No. 6 on the Test Board

TEST POINTS	TEST CONDITIONS: NORMAL STAND-BY	PROTECTIVE RELAY OPER. (3 SEC. TIMER DISABLED)	PROTECTIVE RELAY & CHANNEL RCVR. OPER. (3 SEC. TIMER DISABLED)	PROTECTIVE RELAY & CHANNEL RCVR. OPER. (3 SEC. TIMER USED) (VOLTAGES AFTER 3 SEC)
PROTECTIVE RELAY BD.				
TP 101	12.5 Vdc	less than 0.5	less than 0.5	less than 0.5
TP 102	6.5	6.5	6.5	less than 0.5
TP 103	less than 0.5	less than 0.5	less than 0.5	17
TP 104	6	6	6	less than 0.5
TP 105	less than 0.5	less than 0.5	less than 0.5	20
TP 106	20	20	20	0
TP 107	less than 0.5	less than 0.5	less than 0.5	9
PCT -5	less than 0.5	20	20	6.5
PCT -15	less than 0.5	7	7	less than 0.5
TIMING BD.				
TP 201	20	20	20	20
TP 202	20	20	less than 0.5	20
PCT -14	0	0	0	20
PCT -16	0	0	20	0
CHANNEL BD.				
TP 151	15	15	less than 0.5	less than 0.5
TP 152	15	15	less than 0.5	less than 0.5
TP 153	45	less than 0.5	less than 0.5	45
PCT -10	less than 0.5	less than 0.5	7	7
PCT -18	0	45	45	0

- PCT INDICATES PRINTED CIRCUIT TERMINAL

TABLE I (CONT.)

TEST POINTS	NORMAL STAND-BY	PROTECTIVE RELAY OPER. (3 SEC. TIMER DISABLED)	PROTECTIVE RELAY & CHANNEL RCVR. OPER. (3 SEC. TIMER DISABLED)	PROTECTIVE RELAY & CHANNEL RCVR. OPER. (3 SEC. TIMER USED) (VOLTAGES AFTER 3 SEC.)
		TEST CONDITIONS		
ARMING BD.				
TP 253	10	10	less than 0.5	less than 0.5
TP 254	less than 0.5	less than 0.5	20	less than 0.5
TP 255	20	20	0	20
TP 256	6.5	less than 0.5	less than 0.5	6.5
PCT -1	10	less than 0.5	less than 0.5	10
PCT -19	less than 0.5	19	19	less than 0.5
OUTPUT BD.				
TP 301	20	20	20	20
TP 302	0	0	0	0
TP 303	2	less than 0.5	less than 0.5	less than 0.5
TP 304	2	7.5	2	7.5
TP 305	19	19	5.5	19
TP 306	0	0	13	0
TP 307	20	20	less than 0.5	20
TP 308	0	0	20	0
PCT -14	19	less than 0.5	19	less than 0.5
TEST BD.				
TEST PT. - 1	0	0	20	0
TEST PT. - 2	19	less than 0.5	19	less than 0.5
TEST PT. - 3	less than 0.5	19	19	19
TEST PT. - 4	less than 0.5	less than 0.5	7	7
TEST PT. - 5	0	45	45	0
TEST PT. - 6	0 (REF)	0 (REF)	0 (REF)	0 (REF)

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	PROTECTIVE RELAY INTERFACE BD. (S# 201C050G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
D101-D102	DIODE 1N645A	837A692H03
D103-D105		
D104	DIODE 1N457A	184A855H07
Z101	ZENER DIODE 1N3686B	185A212H06
Z102-Z103	ZENER DIODE 1N957B	186A797H06
Z104	ZENER DIODE 1N3688B	862A288H01
Q101-Q102	TRANSISTOR 2N3417	848A851H02
Q103-Q106		
Q108-Q109		
Q104-Q105	TRANSISTOR 2N697	184A638H18
Q107	TRANSISTOR 2N3645	849A441H01
C101	CAPACITOR 0.047 MFD., 200 VOLTS, ±5%	849A437H04
C102	CAPACITOR 68 MFD., 35 VOLTS, ±20%	187A508H02
C103	CAPACITOR 0.27 MFD., 200 VOLTS, ±10%	188A669H05
R101-R102	RESISTOR 4.7K OHMS, ½ WATT, ±2%	629A531H48
R103	RESISTOR 82K OHMS, ½ WATT, ±2%	629A531H78
R104-R122	RESISTOR 10K OHMS, ½ WATT, ±2%	629A531H56
R105-R123	RESISTOR 6.8K OHMS, ½ WATT, ±2%	629A531H52
R106-R108	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R111-R114		
R131		
R107-R109	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H59
R110-R112		
R113-R117		
R118-R120		
R121-R126		
R127-R130		
R132		
R115	RESISTOR 6.8K OHMS, ½ WATT, ±5%	184A763H47
R116	RESISTOR 56K OHMS, ½ WATT, ±5%	184A763H69
R119-R128	RESISTOR 12K OHMS, ½ WATT, ±5%	184A763H53
R124	RESISTOR 27K OHMS, ½ WATT, ±2%	629A531H66
R125	RESISTOR 150 OHMS, 3 WATT, ±5%	762A679H01
R133	RESISTOR 4.7K OHMS, ½ WATT, ±5%	184A763H43

\- INDICATES TYPICAL VALUE

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	TIMING BD. (S# 201C046G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
D201-D202	DIODE 1N457A	184A855H07
Z201	ZENER DIODE 1N3686B	185A212H06
Z202-Z203 Z204	ZENER DIODE 1N957B	186A797H06
Q201	TRANSISTOR 2N3417	848A851H02
Q202-Q203	TRANSISTOR 2N1132	184A638H20
Q204	TRANSISTOR 2N697	184A638H18
C201	CAPACITOR 0.047 MFD., 200 VOLTS, ±5%	849A437H04
C202	CAPACITOR 4.7 MFD., 35 VOLTS, ±10%	184A661H12
C203-C204	CAPACITOR 6.8 MFD., 35 VOLTS, ±5%	184A661H21
* R201	RESISTOR 47K OHMS, 1 WATT, ±5%	187A643H67
R202	RESISTOR 4.7K OHMS, ½ WATT, ±2%	629A531H48
R203	RESISTOR 82K OHMS, ½ WATT, ±2%	629A531H78
R204	RESISTOR 10K OHMS, ½ WATT, ±2%	629A531H56
R205	RESISTOR 6.8K OHMS, ½ WATT, ±2%	629A531H52
R206	RESISTOR 2.2K OHMS, ½ WATT, ±5%	184A763H35
R207	RESISTOR 15K OHMS, ½ WATT, ±5%	184A763H55
R208-R216	RESISTOR 33K OHMS, ½ WATT, ±5%	184A763H63
R209	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R210-R211 R215	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H51
R212	RESISTOR 1.5K OHMS, ½ WATT, ±5%	184A763H31
R213	RESISTOR 68K OHMS, ½ WATT, ±5%	184A763H71
R214	POTENTIOMETER 50K OHMS	629A430H01
	* CHANNEL BD. (S# 201C013G01)	
D151-D152 D153	DIODE 1N457A	184A855H07
Z151-Z153	ZENER DIODE 1N3686B	185A212H06
Z152-Z154	ZENER DIODE 1N957B	186A797H06
Z155	ZENER DIODE UZ 5875	837A693H04
Z156	ZENER DIODE 1N3688A	862A288H01
Q151-Q152 Q153	TRANSISTOR 2N3417	848A851H02
Q154	TRANSISTOR 2N699	184A638H19
Q155	TRANSISTOR 2N3064	184A638H24
C151-C152	CAPACITOR 0.047 MFD., 200 VOLTS, ±5%	849A437H04
R151-R152 R157-R158	RESISTOR 4.7K OHMS, ½ WATT, ±2%	629A531H48
R153-R159	RESISTOR 82K OHMS, ½ WATT, ±2%	629A531H78
R154-R160	RESISTOR 10K OHMS, ½ WATT, ±2%	629A531H56
R155-R161	RESISTOR 6.8K OHMS, ½ WATT, ±2%	629A531H52
R156-R162	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R163-R164	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H51

ELECTRICAL PARTS LIST

* CIRCUIT SYMBOL	CHANNEL BD. (S# 201C013G01) (CONTINUED) DESCRIPTION	WESTINGHOUSE DESIGNATION
R165-R166 R167 R168	RESISTOR 15K OHMS, 1 WATT, ±5%	187A643H55

CIRCUIT SYMBOL	ARMING BD. (S# 201C022G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
D259-D260 D261-D263 D264-D265	DIODE 1N457A	184A855H07
Q254-Q255 Q256-Q258 Q259	TRANSISTOR 2N3417	848A851H02
Q257	TRANSISTOR 2N3645	849A441H01
R266-R267 R270-R271 R275-R276 R281-R282 R284-R285 R287-R288	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H51
R268-R272 R273-R274 R277-R278 R283	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R279	RESISTOR 27K OHMS, ½ WATT, ±2%	629A531H66

CIRCUIT SYMBOL	OUTPUT BD. (S# 201C024G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
D301-D302 D303-D304 D305-D306 D308	DIODE 1N457A	184A855H07
D307	DIODE 1N645A	837A692H03
Z301-Z303 Z304-Z305	ZENER DIODE 1N957B	186A797H06
Z306	ZENER DIODE 1N3688A	862A288H01
Q301-Q305 Q306-Q307 Q309	TRANSISTOR 2N3645	849A441H01
Q302-Q303 Q304-Q308	TRANSISTOR 2N3417	848A851H02

ELECTRICAL PARTS LIST

C301	CAPACITOR 1.0 MFD., 35 VOLTS, ±10%	837A241H15
C302-C303 C306-C309	CAPACITOR 0.22 MFD., 50 VOLTS, ±10%	762A703H01
C305	CAPACITOR 4.7 MFD., 35 VOLTS, ±10%	184A661H12
C307-C308	CAPACITOR 0.047 MFD.,200 VOLTS, ±5%	849A437H04
C310	CAPACITOR 0.10 MFD.,200 VOLTS, ±10%	188A669H03
C311	CAPACITOR 1.5 MFD., 35 VOLTS, ±10%	187A508H09
R301-R303 R304-R306 R310-R311 R315-R320 R323-R324 R326-R330 R335	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H51
R302	RESISTOR 120K OHMS, ½ WATT, ±5%	184A763H77
R305	RESISTOR 47 OHMS, ½ WATT, ±5%	187A290H17
R307-R314 R319-R321 R325	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R309-R317	RESISTOR 1K OHMS, ½ WATT, ±5%	184A763H27
R312	RESISTOR 470 OHMS, ½ WATT, ±5%	184A763H19
R313	RESISTOR 470K OHMS, ½ WATT, ±5%	184A763H91
R316	POTENTIOMETER 15K OHMS	629A430H08
R318-R322 R328	RESISTOR 4.7K OHMS, ½ WATT, ±5%	184A763H43
R327	RESISTOR 6.8K OHMS, ½ WATT, ±5%	184A763H47
R329	RESISTOR 18K OHMS, ½ WATT, ±5%	184A763H57
R331	RESISTOR 10K OHMS, ½ WATT, ±2%	629A531H56
R332	RESISTOR 6.8K OHMS, ½ WATT, ±2%	629A531H52
R333	RESISTOR 27K OHMS, ½ WATT, ±2%	629A531H66
R334	RESISTOR 150 OHMS, 3 WATT, ±5%	762A679H01

CIRCUIT SYMBOL	TEST BD. (S# 899C711G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
S1	POTENTIOMETER 1K OHMS	185A086H28
S2	POTENTIOMETER 50K OHMS	185A086H22

CIRCUIT SYMBOL	CHASSIS MOUNTED COMPONENTS DESCRIPTION	WESTINGHOUSE DESIGNATION
Z1	ZENER DIODE 1N2984B	762A631H01
R1	RESISTOR 300 OHMS, 25 WATT, ±5%	1202847

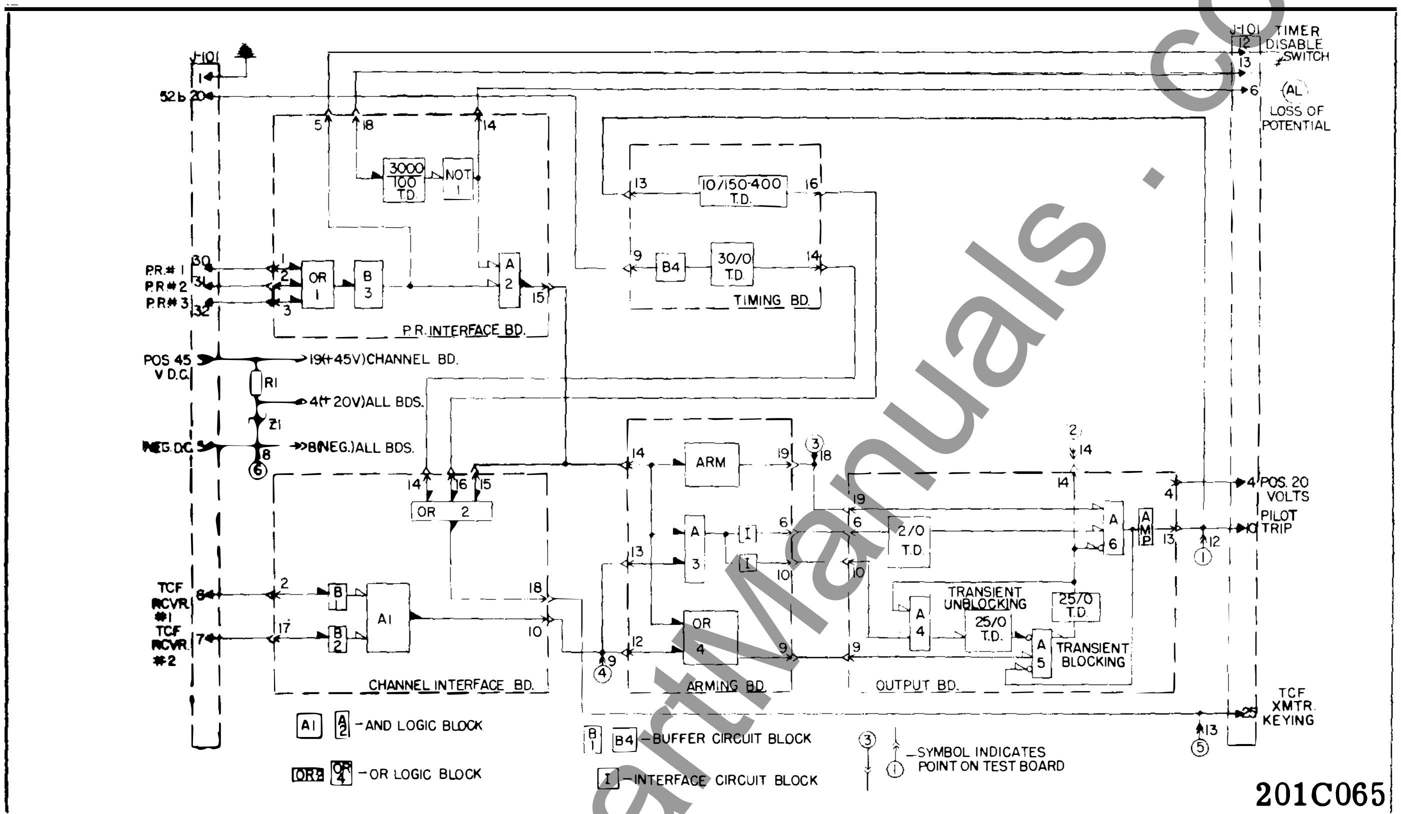


Fig. 2 Logic Block Diagram for the Type STU Relay

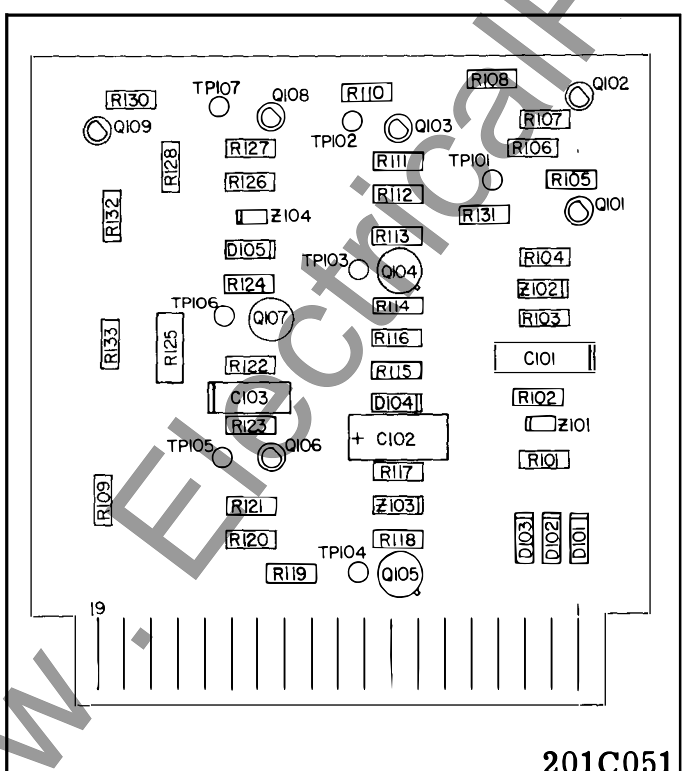


Fig. 3 Component Location of the Protective Relay Board for the Type STU Relay.

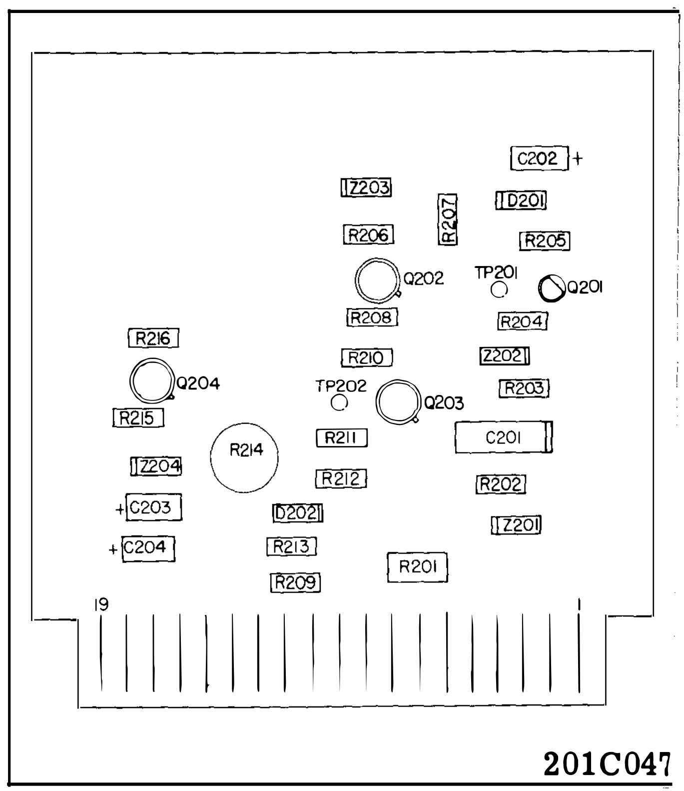
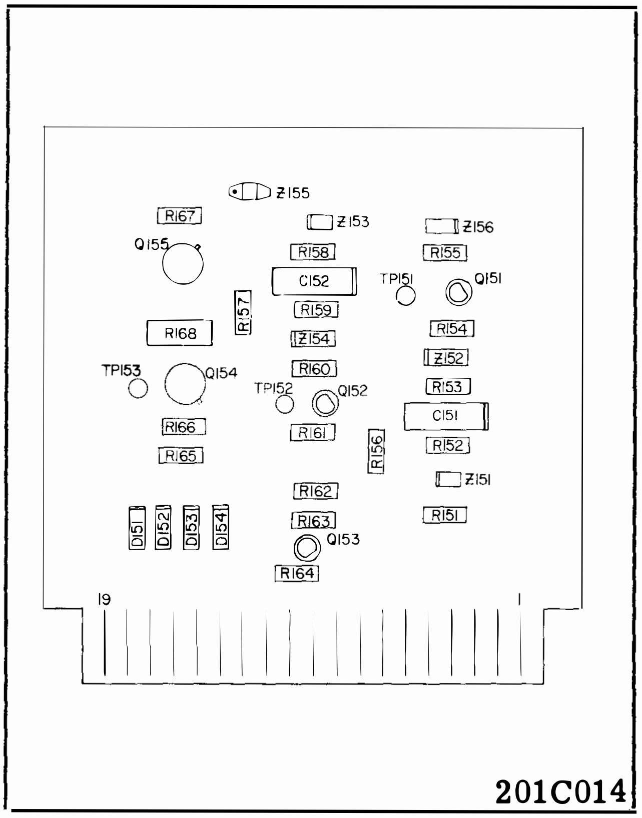


Fig. 4 Component Location of the Timing Board for the Type STU Relay.



* Fig. 5 Component Location of the Channel Board for the Type STU Relay.

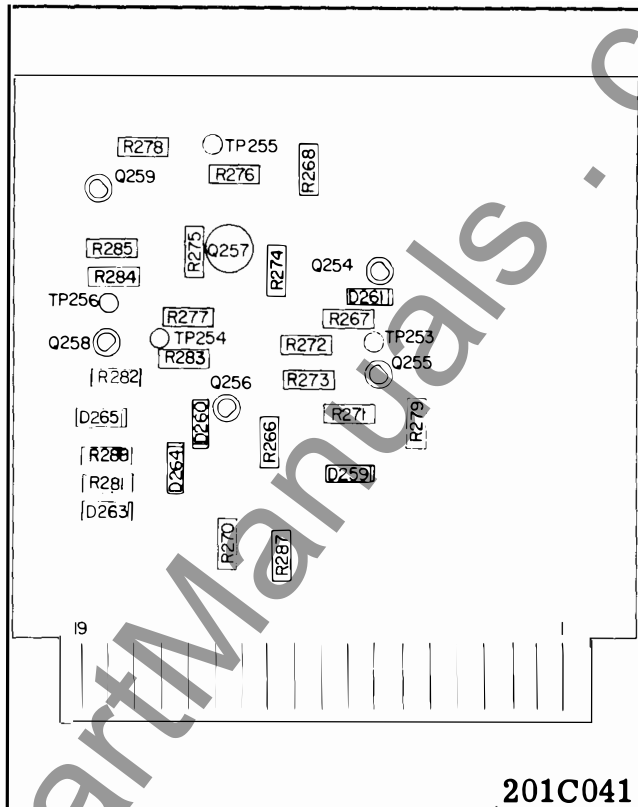


Fig. 6 Component Location of the Arming Board for the Type STU Relay.

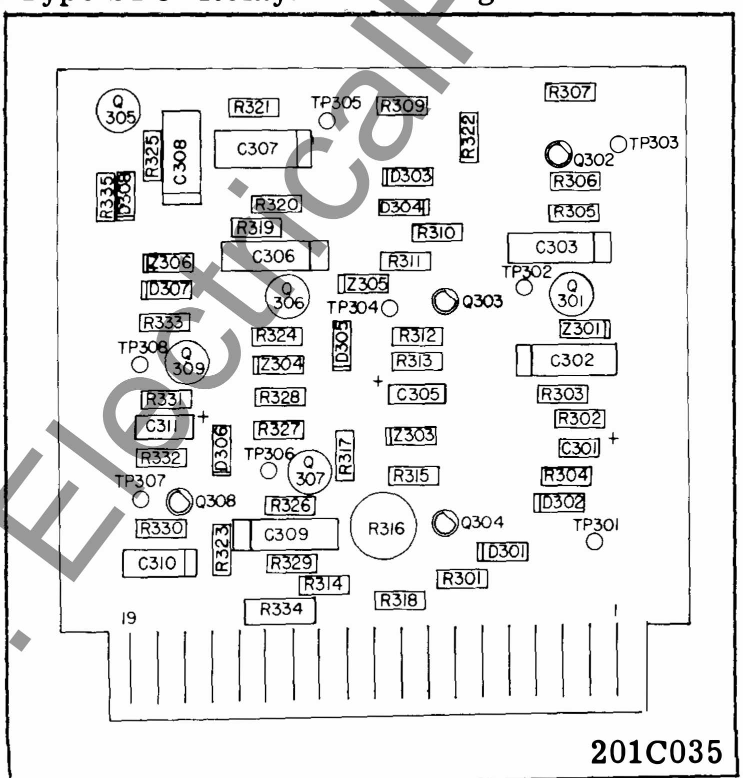


Fig. 7 Component Location of the Output Board for the Type STU Relay.

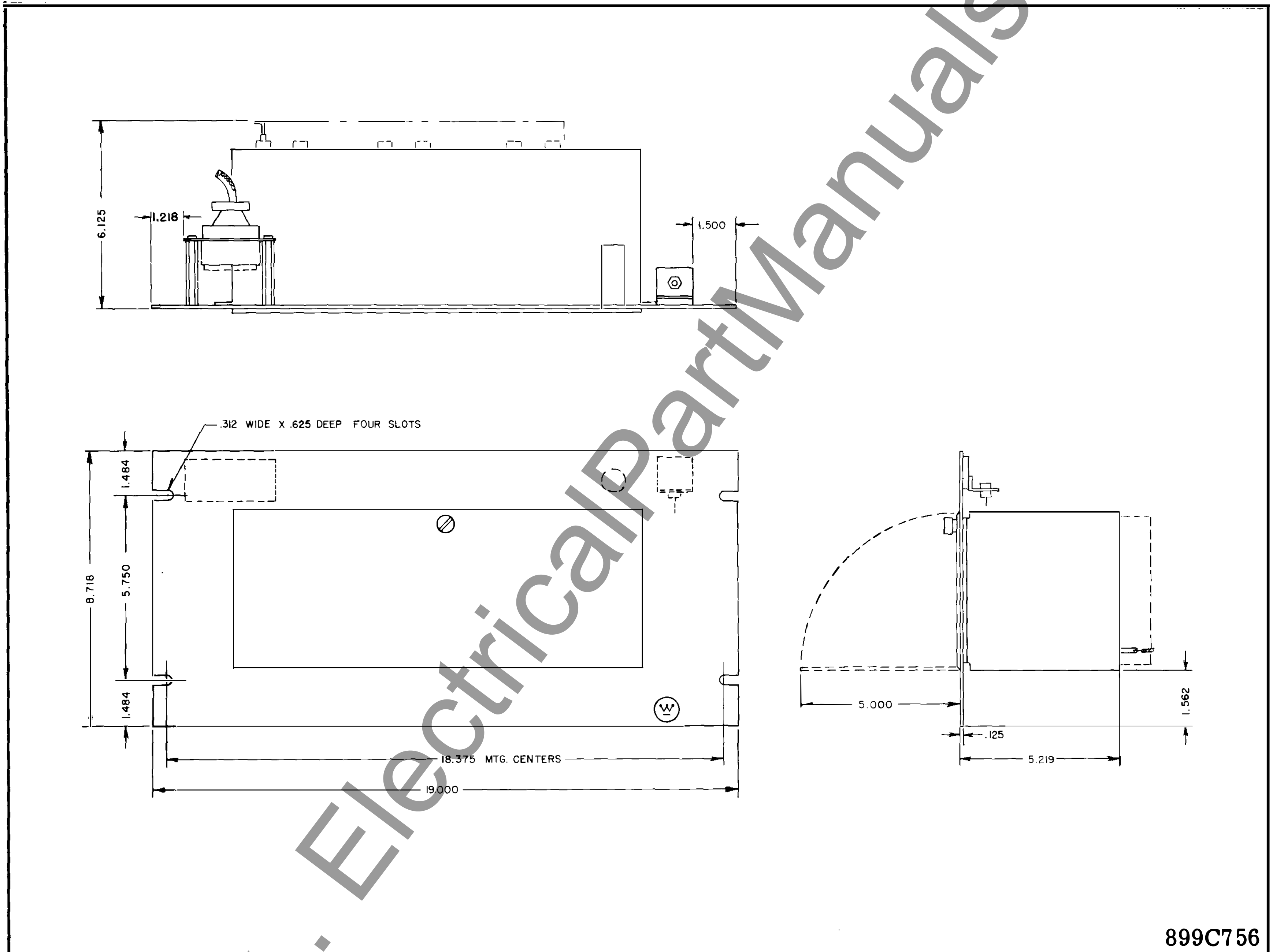


Fig. 8 Outline and Drilling Plan for the STU Relay.

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