BASIC SYSTEMS DRIVES (BSD)
TENSION SEQUENCER - BASIC

I. INTRODUCTION

This printed circuit card is from the series of cards designed for the BSD MASTER CONTROLLER functions. However, it is also applied in the Reel Controller subsystem to sequence the current regulated thyristor power supply and the Reference Summer/Rate Detector Card S#1781A13 G01. The logic associated with the current and tension regulated drives has been pre-engineered and implemented by means of solid state logic devices on various printed circuit cards. Though the basic logic is committed on this board, some flexibility has been provided to allow modification of the basic interlocked functions. I.L. 16-800-290 provides the necessary information on the equivalent relay logic standards used in describing the circuits of this sequencer card.

Figure 1 is a picture of the Tension Sequencer-Basic. A front view locating all components by schematic identification is shown on the last page of the instruction leaflet.

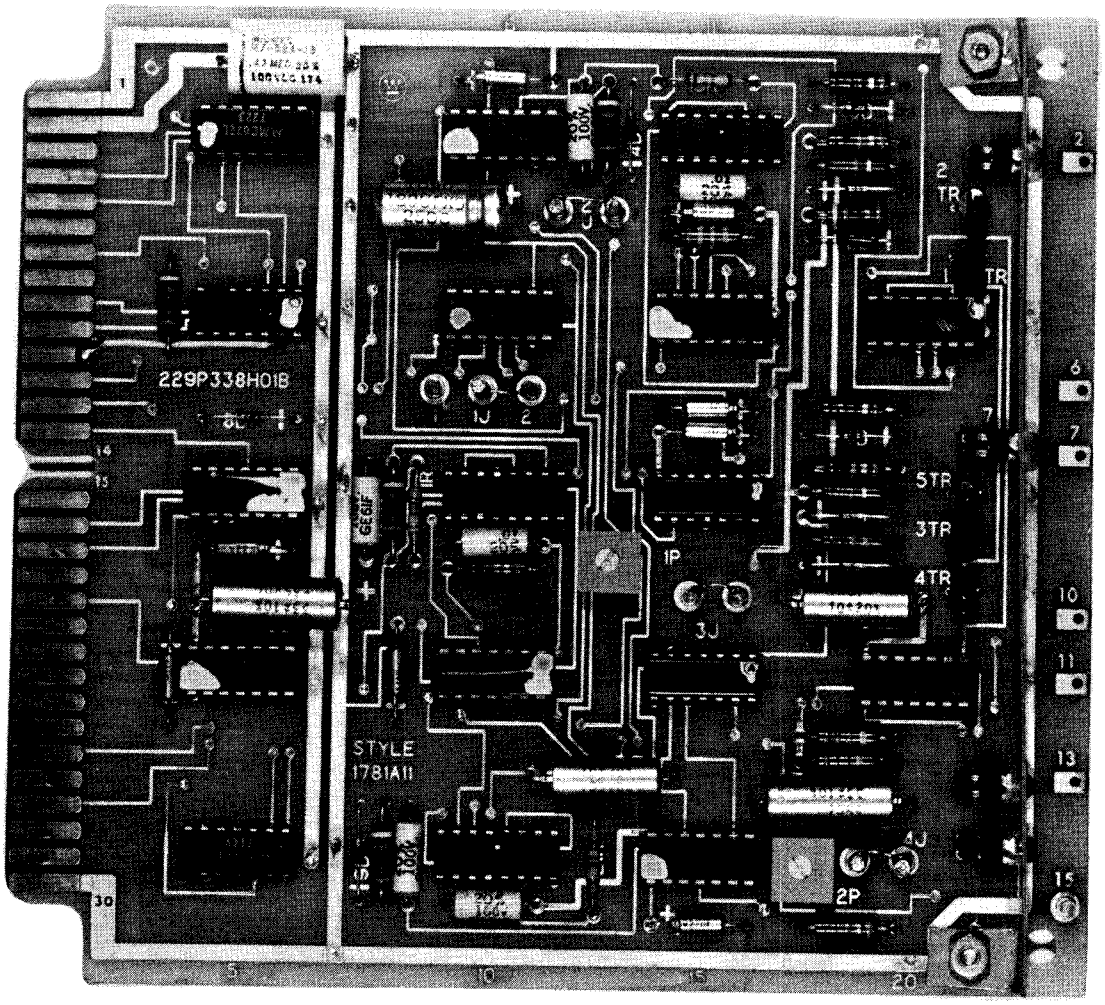
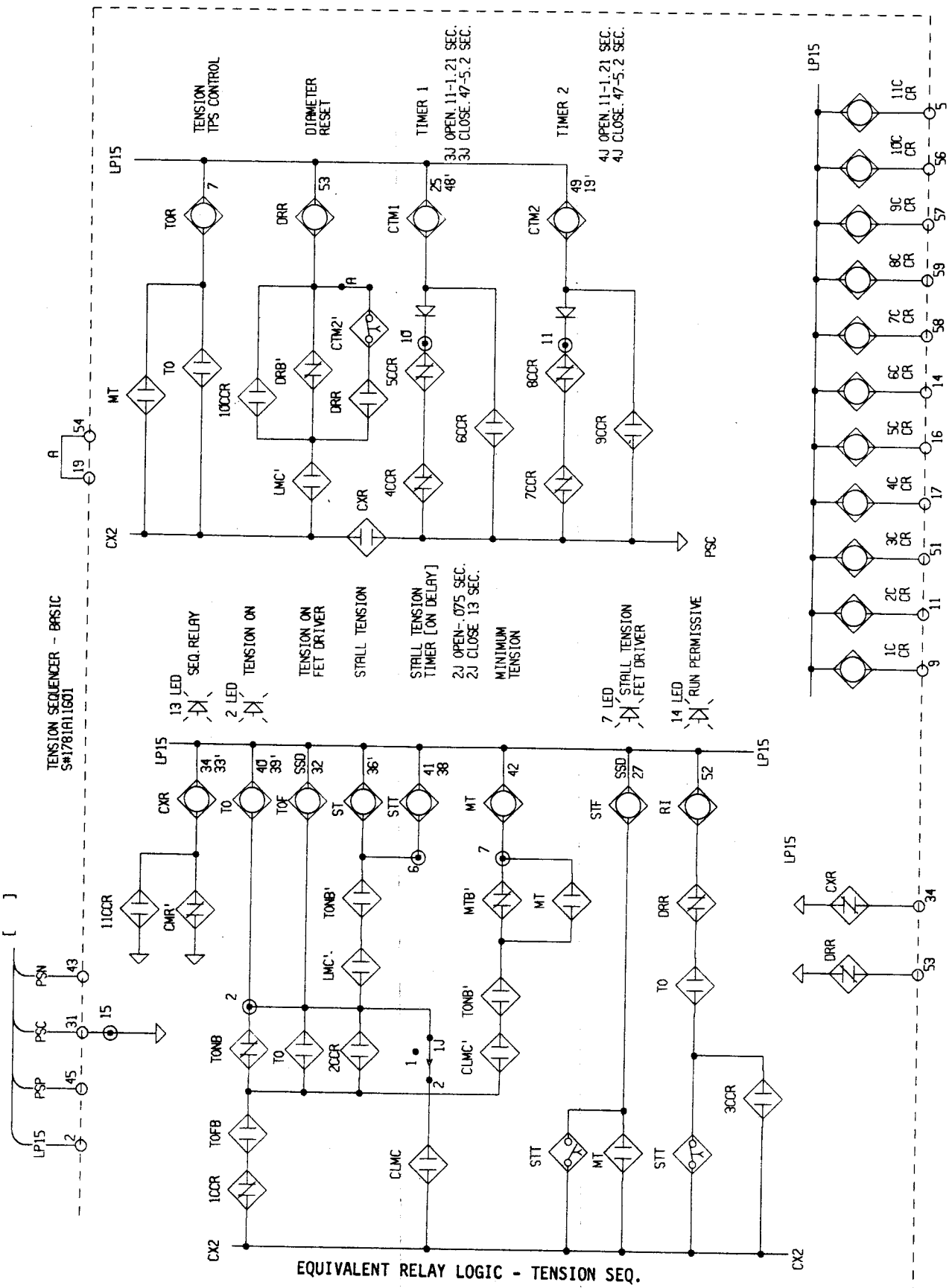
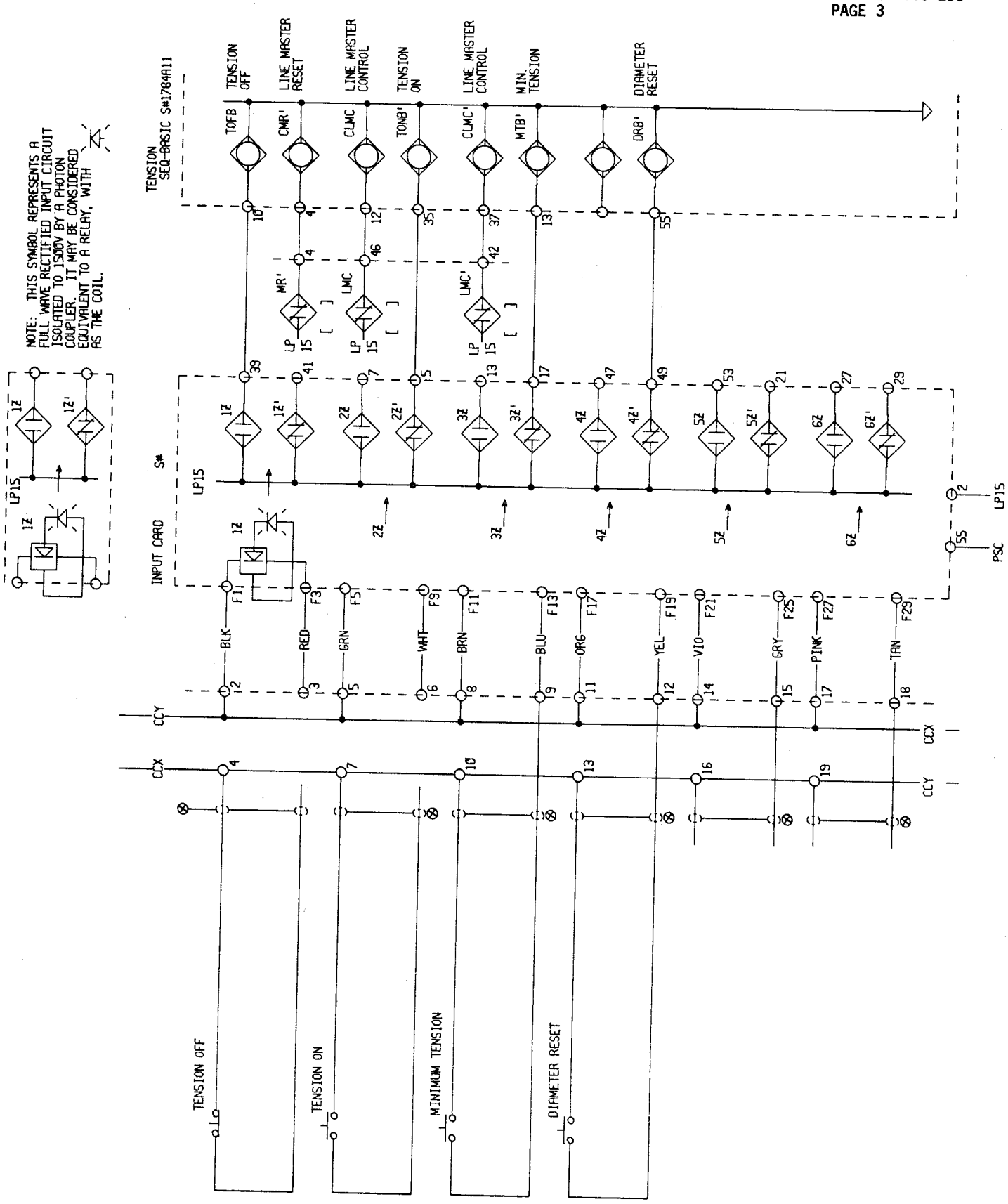


FIGURE 1



EQUIVALENT RELAY LOGIC - TENSION SEQ.

FIGURE 2A



TENSION SEQ. INPUT CIRCUITS

FIGURE 2B

II. DESCRIPTION OF OPERATION

A. Introduction

As a part of a static logic system, this card has to operate in conjunction with other pc cards for a complete functional arrangement. A static Input Card, S#1640A40, is required to provide an interface function between the external pushbuttons, switches, etc., operating at 115V AC and the logic signals required by the Tension Sequencer card. The output signals from this card are used for sequencing various analog controller cards, such as the Reference Summer/Rate Detector and for an external relay interface card, such as a Static Switch Driver S#1606A04.

B. Circuit Functionalization

Figure 2a is a part of a typical static ladder diagram showing the various functions in the manner that they have been pre-engineered. The following list should clarify the abbreviated terminology used.

MR	Master Reset
LMC	Line Master Control
TONB	Tension On Pushbutton
TOFB	Tension Off Pushbutton
MTB	Minimum Tension Pushbutton
DRB	Diameter Reset Pushbutton

The various input signals to this card are represented by static relays whose contacts are shown in the ladder diagram. Those inputs which have been pre-engineered into the system are designated by an alphabetic abbreviation, such as TONB. Those inputs which have been provided for flexibility have a numeric designation, such as 1CCR, 2CCR, etc.

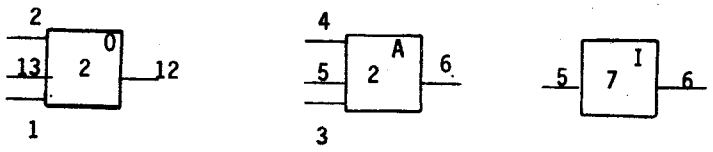
Typical input signals from the static Input Card are shown interfacing with static relays in Figure 2b. Some of the static relays have a primed designation, such as TONB' and some are unprimed, such as TOFB. For those relays that have unprimed designations, the input signal to the relay is +15V when 115V AC is applied to the corresponding input terminals of the Input Board and is 0V when the AC voltage is removed. For those relays that have primed designations, the input signal is +15V when no AC voltage is applied to the corresponding input terminals and is 0V when AC voltage is applied.

Note on Figures 2a and 2b the different reference voltages for the input static relays. In Figure 2a the relays are reference to +15V so that a logic 1 de-energizes the static relay and a logic 0 energizes the static relay. In Figure 2b, the reverse is true because the relays are referenced to PSC. A logic 1 energizes the static relay and a logic 0 de-energizes the static relay.

There are two types of output signals available from this card. These signals are logic signals (0V or +15V) and static switch driver signals (the collector of a non-conducting transistor or -24V). The type of output available is identified by the relay designation. No F suffix implies logic outputs; an F suffix implies the output is an SSD signal. For logic outputs, a signal and its complement may be available. For example, the CXR relay has both outputs available. Pin 34 is the CXR signal and pin 33 is the complement CXR'. These two terminal numbers are identified in Figure 2a as pin 34, pin 33' in physical association with the CXR static relay.

In checking the operation of the static ladder diagram, the condition of the various relays has to be determined. In the TO circuit, the TONB' and TOFB relays are normally energized. Energizing of TO requires initially an energized CXR relay. If the TONB' relay is de-energized, the TO relay will energize and seal-in contacts will hold the relay energized. De-energizing of TO requires that TOFB be de-energized. Contacts of 1CCR and 2CCR are part of the TO circuit; but if they are not used, they don't influence the operation described above. The numerically designated relays are not a part of the standard sequence procedure and their use has to be designed into the logic. Contacts of LMC can be used to bypass external pushbuttons until the line (system) comes to a stop.

The schematic diagram shows the logic required to produce the various functions. From the standpoint of the various pc terminals, the levels required on the logic diagram and on the schematic are consistent. That is, a zero on the schematic should correspond to a zero on the logic diagram, etc. For the logic signal levels, a zero can be a voltage between 0 and +1.5V and a one can be a voltage between +13.5V and +15V. The schematic has logic blocks which are identified typically as follows:



The numeric designation within the block identifies the location of the IC. The alphabetic designation in the upper right hand corner describes the function of the block and hence the inputs required. The designations are O for an OR function, A for an AND function and I for an INVERT function.

All of the logic elements are NAND gates and the alphabetic designation will assist in working through the logic. For a block that has an O designation, one of the inputs must be a zero to satisfy the function. For a block that has an A designation, all of the inputs must be one to satisfy the function. An inverter block simply inverts the input signal.

There are various methods of applying tension which have been engineered into the system. These are described as follows:

Tension can be applied to a selected operational level in an exponential manner. Tension will be maintained at this level until either the line is started or until a 13 second time interval elapses. If the line has not been started within this interval, a permissive interlock to the master controller is removed and the line cannot be started unless the Tension On pushbutton is again depressed. The TO relay remains energized after the timer runs out, but it is necessary to reset the On Delay (STT) in order to re-energize the RI relay.

Tension can be applied to a selected minimum operational level in an exponential manner. When the TO relay is energized, tension attempts to increase to its operational level; however, after a 75msec. time period, the tension reference is transferred to a minimum level. For this mode of operation, the timing period of STT must be changed from 13 secs to 75 ms. In addition, relay 3CCR must be maintained in the energized state in order to bypass the contacts of STT in the RI circuitry. Once tension has been applied, the line can be started at any time and the tension signal will transfer to the required operational level.

The use of the LMC contacts in the TO circuitry is a function of the application. In line operation, 1J should be position 2 in order to bypass the external pushbutton while the line is running. In other applications, 1J should be in position 1.

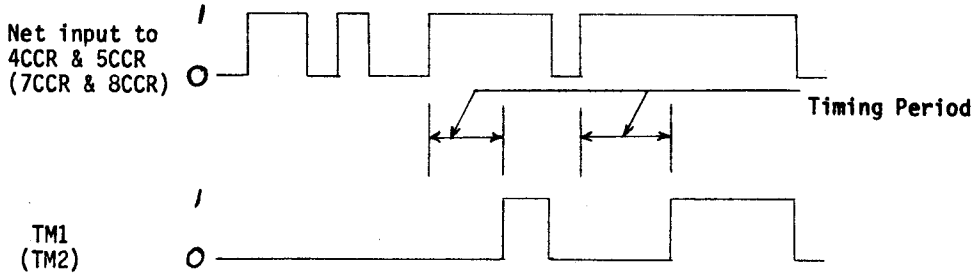
The jumpers that are used on this board are normally soldered into fixed positions. They have to be removed or repositioned to change operating status. 1J is normally in position 2 for line operation. 2J is normally on the board to set the time interval of STT at 13 secs. This jumper has to be removed to change the timing interval to 75 msecs.

The simplified diagram in Figure 2a includes both standard and optional features associated with the Tension Sequencer-Basic. The various options shown include MT, STF, DRR, TM1 & TM2. Although TM1 and TM2 have specific functions relative to the overall function of the ladder diagram, their inputs have been uncommitted in order to provide maximum flexibility for optional use in a system.

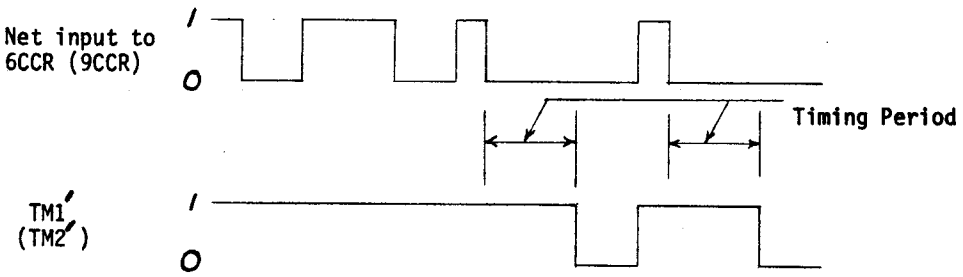
TM1 and TM2 can be used for either ON or OFF delays. Two timing ranges are available: 0.47 to 5.2 secs. if the appropriate jumper is wired (normal); 0.11 to 1.21 secs if the appropriate jumper is removed. To use TM1 as an ON delay, no input should be applied to 6CCR. Either 4CCR or 5CCR or both can be used to trigger the timer. If both inputs to the relay change to the one state, or if one input changes to the one state with the other input left open, TM1 energizes. There are two output signals TM1 and TM1′. TM1 will change from a zero to a one after the timing period has passed. TM1′ will change from a one to a zero after the timing period has passed. Both outputs will return to the initialized state (TM1 = 0 and TM1′ = 1) when either 4CCR or 5CCR energizes (applying a zero to the corresponding input terminal). To use TM1 as an OFF delay, either 4CCR or 5CCR should be energized by connecting the corres-

ponding input terminal to PSC. When 6CCR energizes, the timer is initiated and the output signal TM1' will be representative of the OFF delay signal. It will remain in the one state until the timer has elapsed following which the output will be zero. The timers are resettable and will reset if the used input does not last until the timer has cycled.

ON DELAY TIMING



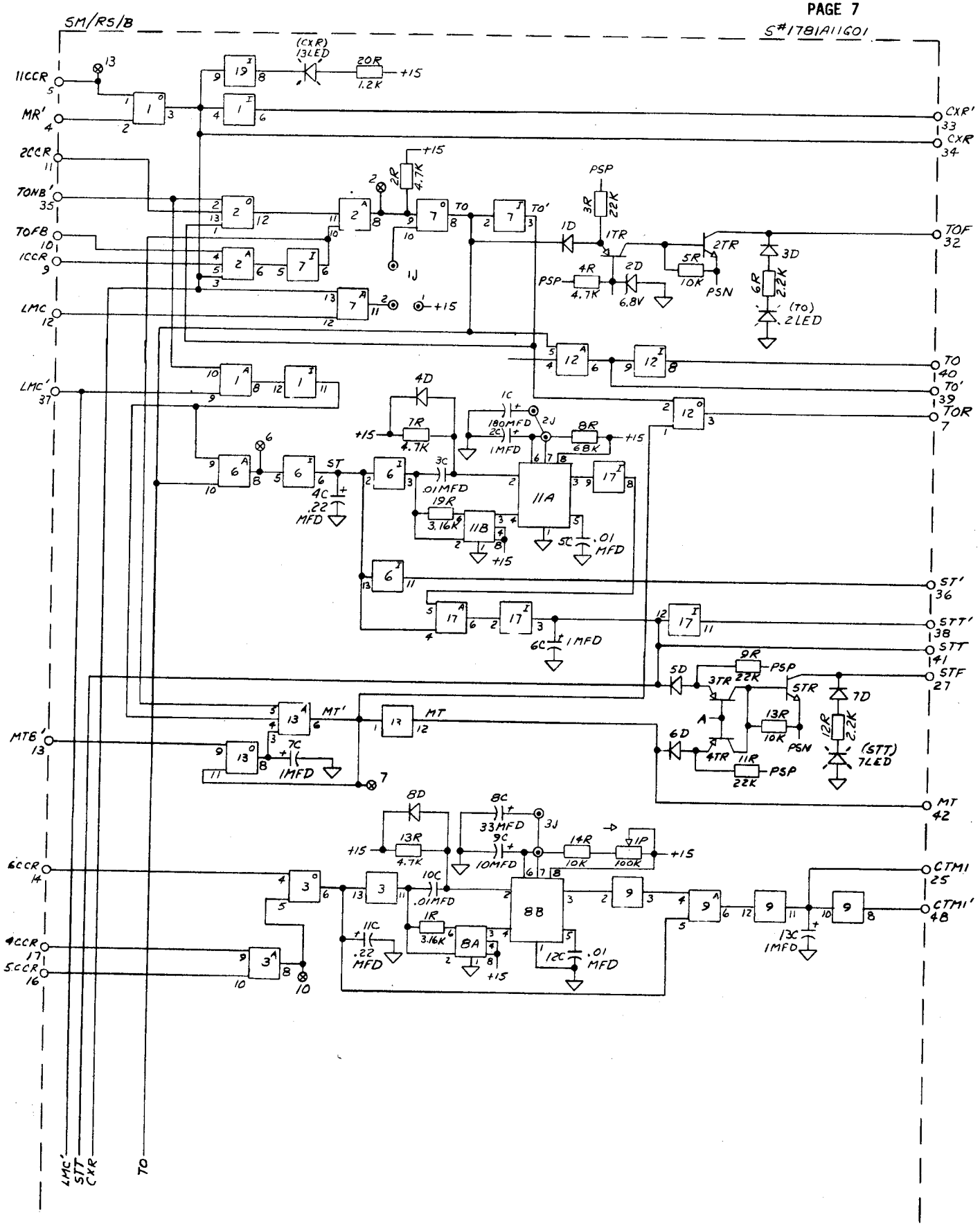
OFF DELAY TIMING

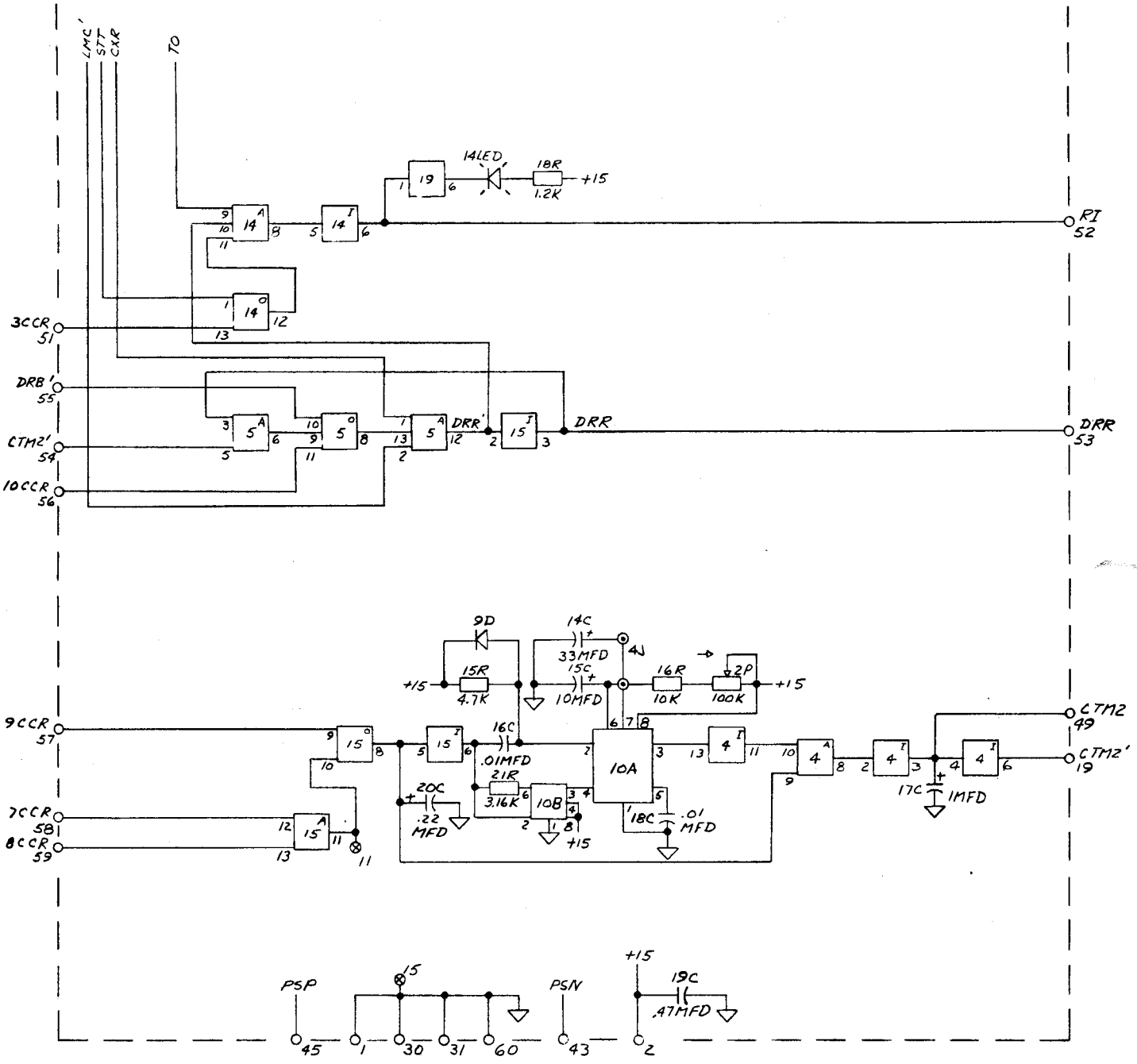


TYPICAL TIMING DIAGRAMS

On the schematic diagram and the block diagram there are test points which are designated in the following fashion - ⊗ 2. On the front edge of the board, there is an identification strip with the numeric designations 1 through 15. These numbers locate both the LED's and the test points. The test point can be used for monitoring the status of a particular signal and it can be used for energizing a particular function by connecting the appropriate test point to PSC (test point 15).

An unused input pin on the logic circuitry corresponds to a 1. If the unused inputs are measured with a meter, the readings obtained will not be consistent with what has been specified for the one level.


SM/RS/B
S#1781A11601
11CCR
MR'
2CCR
TONB'
TOFB
1CCR
LMC
LMC'
MTB'
6CCR
4CCR
5CCR
(CXR) 13LED
20R 1.2K
+15
CXR' 33
CXR 34
TOF 32
TO 40
TO' 39
TOR 7
ST' 36
STT' 38
STT 41
STF 27
MT 42
CTMI 25
CTMI' 48
PSP
3R 22K
1D
1TR
2TR
3D
4R 4.7K
2D 6.8V
5R 10K
PSN
6R 2.2K
(TO) 2LED
2R 4.7K
1J
4D
7R 4.7K
1C 180MFD 2C 1MFD
2J
8R 68K
3C .01MFD
19R 3.16K
11A
11B
5C .01 MFD
4C .22 MFD
ST
6C 1MFD
5D
9R 22K
3TR
5TR
7D
13R 10K
12R 2.2K
6D
4TR
11R 22K
(STT) 7LED
MT'
7C 1MFD
8D
8C 33MFD
3J
13R 4.7K
9C 10MFD
14R 10K
1P 100K
10C .01MFD
88
1R 3.16K
8A
11C .22 MFD
12C .01 MFD
13C 1MFD
LMC'
STT
CXR
TO


LMC'
STT
CXR
TO
14LED
19
1BR
1.2K
+15
RI
52
3CCR
51
DRB'
55
CTM2'
54
10CCR
56
DRR'
DRR
DRR
53
9D
14C
33MFD
15R
4.7K
15C
10MFD
16R
10K
2P
100K
+15
9CCR
57
16C
.01MFD
21R
3.16K
10A
CTM2
49
CTM2'
19
7CCR
58
8CCR
59
20C
.22
MFD
10B
1BC
.01
MFD
17C
1MFD
PSP
PSN
15
19C
.47MFD
45
1
30
31
60
43
2

III. CHARACTERISTICS AND RATINGS

Power Supplies:

PSP	+24V	±1.5V	@	6 ma
PSN	-24V	±1.5V	@	23 ma
+15	+15V	±0.5V	@	165 ma

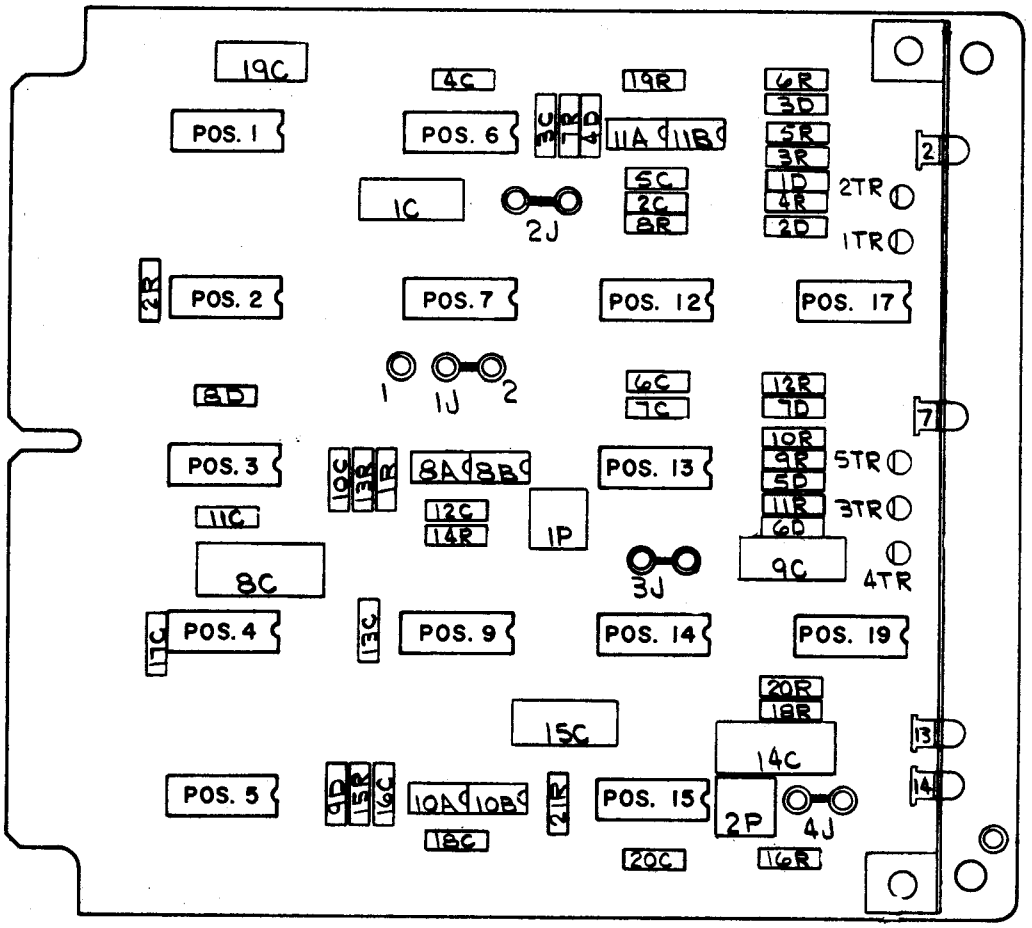
Output Capcity:

Output Terminal	33	34	40	39	7	36	38	41
Load Capacity (HTL Logics)	10	5	10	9	10	10	10	6
Output Terminal	42	25	48	52	50	53	49	19
Load Capacity (HTL Logics)	8	9	10	8	9	9	9	10

Allowable Operating Temperature : $0^{o}C$ to $55^{o}C$

Timer Adjustments:

STT	2J	on	13 sec.	
	2J	off	75 msecs.	
TM1	3J	on	0.47 to 5.2 secs	1P
	3J	off	0.11 to 1.21 secs	
TM2	4J	on	0.47 to 5.2 secs	2P
	4J	off	0.11 to 1.21 secs	


19C
4C
19R
6R
3D
POS. 1
POS. 6
U3
U1
U4
11A
11B
5R
3R
2
1C
2J
5C
2C
8R
1D
4R
2D
2TR
1TR
2R
POS. 2
POS. 7
POS. 12
POS. 17
1
1J
2
6C
7C
12R
7D
8D
7
10R
9R
5D
11R
6D
5TR
3TR
4TR
POS. 3
10C
13R
1R
8A
8B
POS. 13
12C
14R
1P
11C
8C
3J
9C
17C
POS. 4
13C
POS. 9
POS. 14
POS. 19
20R
18R
15C
14C
13
14
POS. 5
9D
15R
16C
10A
10B
21R
POS. 15
2P
4J
18C
20C
16R